

1. Description

1.1. Project

Project Name	QSRC_STM32
Board Name	QSRC_STM32
Generated with:	STM32CubeMX 4.19.0
Date	04/01/2017

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
12	PA2	I/O	USART2_TX	
13	PA3	I/O	USART2_RX	
14	PA4 *	I/O	GPIO_Output	
23	VSS	Power		
24	VDD	Power		
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
35	VSS	Power		
36	VDD	Power		
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function



5. IPs and Middleware Configuration

5.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

5.2. TIM2

Clock Source : Internal Clock

5.2.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1600 *
Counter Mode	Down *
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.3. TIM3

mode: Clock Source

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1600 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.4. USART1

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.5. USART2

Mode: Asynchronous

5.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction
Over Sampling

Receive and Transmit
16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	High *	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	n/a	Low	
	PA4	GPIO_Output	Output Push Pull	n/a	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode: Normal
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	QSRC_STM32
Project Folder	D:\e\praca\QSRC_STM32
Toolchain / IDE	Other Toolchains (GPDSC)
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes