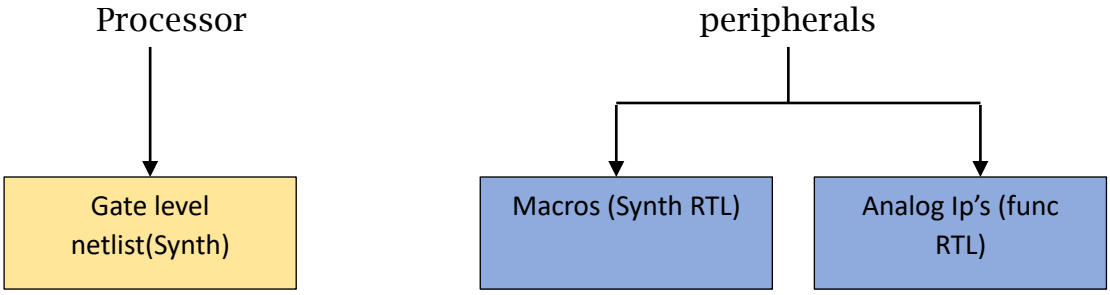
RISC-V REFERENCE SOC TAPEOUT PROGRAM

WEEK – 0

Module 1 : Getting started with Digital VLSI SOC Design and Planning

Testing specification (RISC V GCC)
Writing Verilog code according to specs use key words which are synthesisable
Soc Design Flow start

Splits into two parts:



Analog Ip's are replaced by Mosfet while GLS, Macros need to be synthesisable
Soc Integration (GPIO's)

RTL To GDSII Starts
Floorplanning, Placement, cts, routing

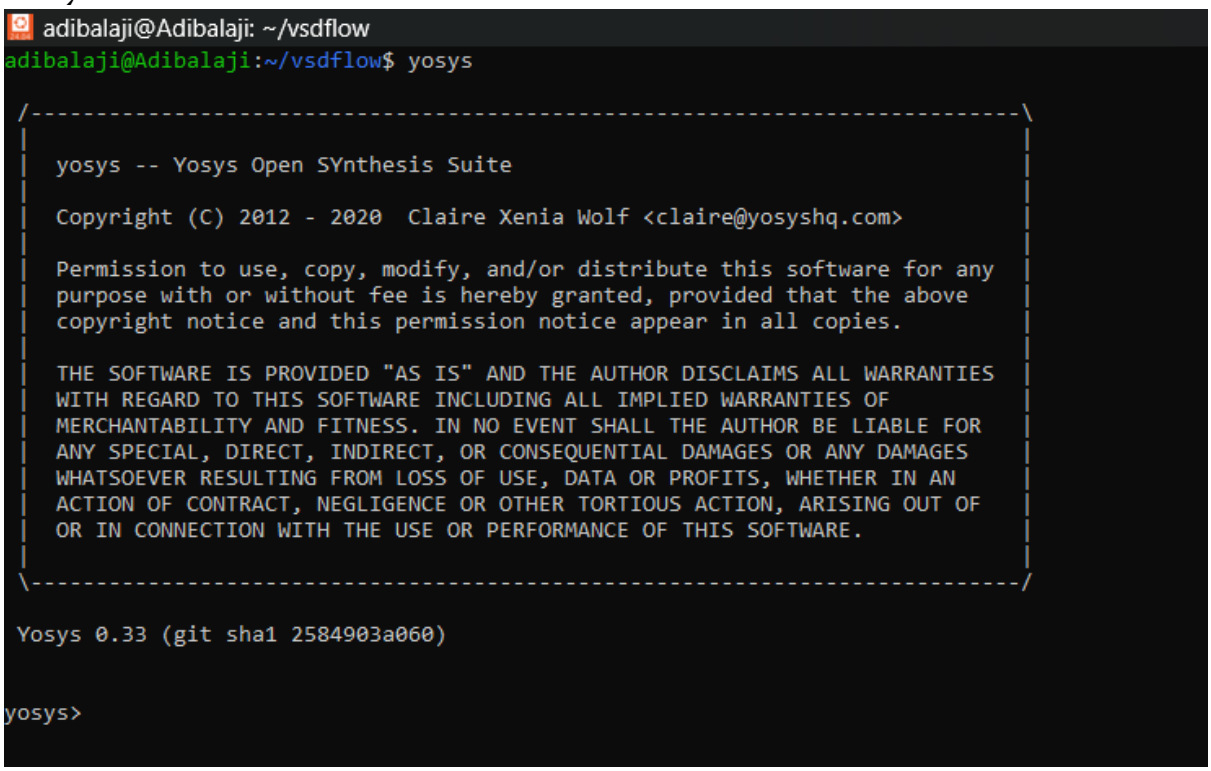
Create GDSII file only metal layer presents
We do some Checks like DRC/LVS/Antenna

After completion of tapeout(Sending to industry) we get a chip now we can design a board on chip to make sure our chip design or chip application is purposefully done

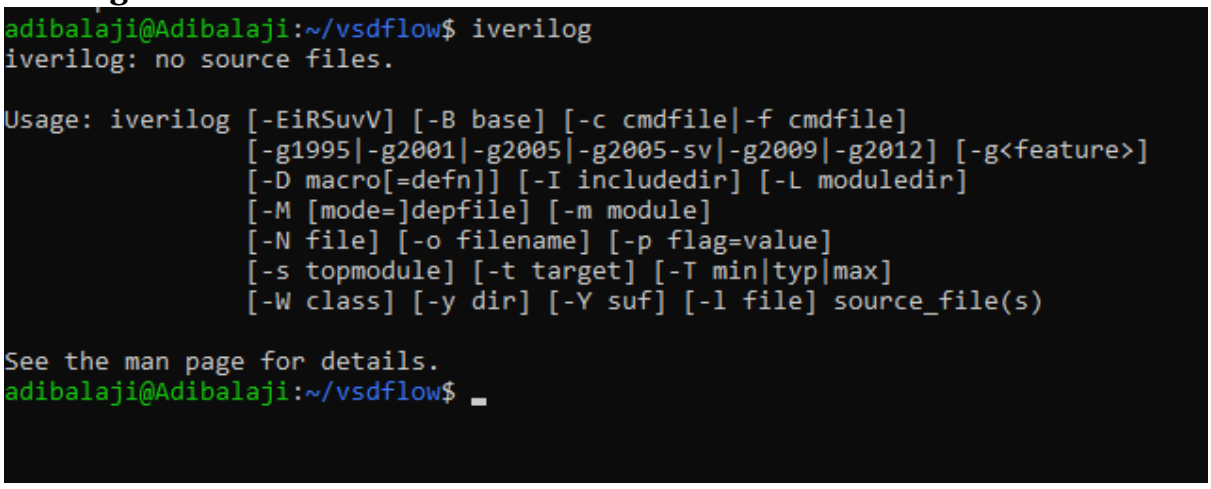
Q: Difference Between Processor & Controller?
Ans: when processor club's with ip's, macros this is called controller

Module 2 : Installation Tools

Yosys Installation



Iverilog Installation



GTKWave Installation