CIRRUS LOGIC®

CL-GD5446

Preliminary Data Book

FEATURES

- **High-throughput PCI bus interface optimized for video playback**
  - — Large write buffer allows sustained zero-wait-state bursts
  - — Independent memory apertures for BitBLT and CPU/video allow concurrent operations for optimized video playback
  - — Byte-swapping for PowerPC™ support
  - — PCI v2.1-compliant
- **Advanced 64-bit BitBLT engine for Windows® 95**
  - — Transparent source data BitBLT for DirectDraw™
  - — Color expansion for all graphics modes
  - — Large data buffers for fast screen-to-screen BitBLTs
  - — Double-buffered, memory-mapped registers with AutoStart™
  - — Optimized color 8 × 8 PatCopy
  - — Accelerated Packed-24 modes
- **64-bit DRAM interface optimized for EDO DRAM**
  - — 80-MHz MCLK offers up to 320 Mbytes/sec. peak bandwidth
  - — Supports new 128K × 16, 128K × 32 DRAM
- **V-Port™, GPIO, I²C bus interfaces for video decoders**
  - — Video capture, closed-caption capture applications
  - — GPIO permits video decoders with single load on PCI bus
  - — Automatic double buffering prevents video 'tearing'
  - — Glueless interface to the CL-PX4072
  - — Interface to MPEG and other video decoders
- **Hardware window for video display**
  - — Multiformat frame buffer
  - — Supports YUV-16 true color video with 8-bit graphics
  - — YUV 4:2:2, AccuPak™, RGB-8, RGB-16 video formats
  - — Unique YUV planar assist mode
  - — Independent interpolated X and Y zooming
  - — Occlusion support with color- or chroma-key
- **PC97-compliant (Revision B)**

(cont.)

64-bit VisualMedia™ Accelerator

OVERVIEW

The CL-GD5446 delivers high-performance graphics and TV-quality, full-motion, full-screen video playback in an integrated, single-chip device. The CL-GD5446 VisualMedia™ accelerator, integrated into a cost-effective personal computer, plays CD-ROM video clips and disk-based video files (including MPEG titles), in full screen at up to 30 frames per second with fully synchronized sound. At the same time, the CL-GD5446 delivers exceptional system throughput with minimal impact to system operation. Transparent BitBLT and page-flipping features provide outstanding DirectDraw™ and games performance.

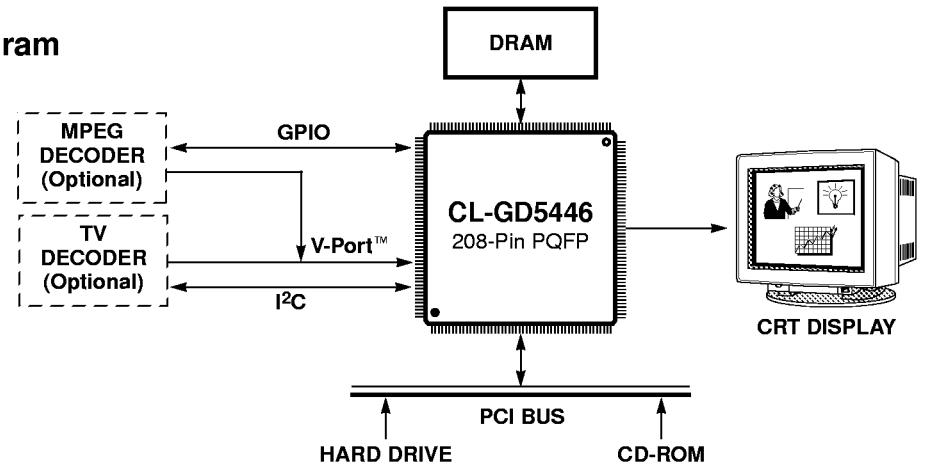
The CL-GD5446 provides a glueless connection to most of the popular video decoder devices from Cirrus Logic as well as other vendors. This provides broad flexibility to support live TV-in-a-window, closed captioning, hardware MPEG, and video conferencing, extending baseline system functions with enhanced features to meet the requirements of a wide range of applications.

The CL-GD5446 can support YUV 4:2:2 video playback in an arbitrarily sized window on 1024 × 768, 256-color graphics with a frame buffer of only 1 Mbyte. This capability can help place PCs using the CL-GD5446 at a very favorable price-performance point.

The CL-GD5446 supports pixel resolutions of up to 1280 × 1024, and 16.8 million colors at resolutions of up to 1024 × 768.

(cont.)

System Block Diagram



FEATURES (cont.)

- **Product differentiation for video-playback applications**
  - — Home PC television tuner: 'TV-in-a-window'
  - — Video clip capture
  - — Home video editing
  - — Video mail/video message
  - — Personal video conferencing
  - — MPEG-1, MPEG-2 applications
  - — Closed-caption applications
- **Cirrus Logic provides enabling software drivers**
  - — Windows® 95, Windows® 3.x, NT™, OS/2®, and AutoCAD®
  - — DirectDraw™ and DCI
  - — VPM™ (video port manager)

OVERVIEW (cont.)

The CL-GD5446 features an integrated dual-frequency synthesizer with on-chip oscillator and filters, as well as a triple 8-bit palette DAC with on-chip current reference. Green-PC power-management features help make systems based on the CL-GD5446 compliant with the Energy Star Program.

The CL-GD5446 is software- and pin-compatible with the industry-standard Alpine family of VGA controllers from Cirrus Logic. It comes with the same Cirrus Logic quality software, applications support, and documentation.

Revision B of the CL-GD5446 is PC97-compliant.

Cirrus Logic also provides TV decoder application software — TVTap™ — for the CL-GD5446/'PX407X designs.

ADVANTAGES

Unique Features	Benefits
Outstanding VisualMedia™ Acceleration	
■ High-throughput PCI bus interface	❒ Minimizes host bus bottleneck for VisualMedia™ playback.
■ Advanced 64-bit BitBLT engine with transparent BitBLT and page-flip support	❒ Supports Fast Windows® 95, DirectDraw™, and games.
■ Optimized EDO DRAM interface	❒ 64-bit and 80-MHz MCLK offer best performance for mainstream DRAMs.
■ 128K × 16/32-bit DRAM options	❒ Allows 3- and 1-Mbyte (64-bit) options.
Superior TV-Like-Quality Video Performance	
■ Hardware video window	❒ Allows independent graphics and video streams to be displayed on-screen.
■ X and Y linear interpolated scaling	❒ Minimizes aliasing and allows best video display regardless of screen size.
■ YUV planar assist, AccuPak™ encoding	❒ Technology to obtain best performance while minimizing video-quality degradation.
■ Multiformat frame buffer	❒ Allows true-color video with 256-color graphics.
■ Color key, chroma key	❒ Allows graphics over video in video playback and video capture modes.
Foundation for Differentiation	
■ Video capture V-Port™	❒ Allows video decoder interface and eliminates separate frame buffer for lower system cost.
■ General-purpose I/O bus	❒ Allows single load, glueless, generic I/O interfacing to industry-standard video decoders.
■ VPM™	❒ Video port API for Windows® v3.x and Windows® 95 easing peripheral application software development.
■ I^2C interface	❒ Allows low-cost control interface for applications such as TV decoders.
Compatibility	
■ Compatible with VGA and VESA® standards	❒ Compatible with installed base of systems and software.
■ Drivers supplied at various resolutions for Windows® 3.1, Windows NT™, AutoCAD®, OS/2®, and other popular applications	❒ Provides a 'ready-to-go' solution minimizing the need for additional driver development.

SOFTWARE SUPPORT

Cirrus Logic provides an extensive — and expanding — range of software drivers to enhance the resolution and performance of many popular software packages. Note that the CL-GD5446 VGA graphics portion of a system *does not* require software drivers to run applications in standard-resolution modes.

Cirrus Logic software drivers for the CL-GD5446 include:

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® / Intel® DCI (display control interface), DirectDraw™, VPM™ Provider	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
Microsoft® Windows® v3.x Microsoft® Windows® 95	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
Microsoft® Windows NT™ v3.5, v3.51, v4.0	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	16 and 256
	640 × 480, 800 × 600, 1024 × 768, 1152 × 864, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
OS/2® v2.11, v3.0	640 × 480, 800 × 600, 1024 × 768,1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
AutoCAD® v12.0, v13.0 Autoshade® v2.0 with Renderman 3D Studio™ v1.0, v2.0, v3.0, v4.0	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768	32,768
	640 × 480, 800 × 600, 1024 × 768	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million

[a] All monitor types do not support all resolutions; 640 × 480 drivers will run on PS/2®-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **Relocatable, 32 Kbytes with PCI bus support**
- **VBE (VESA® BIOS Extensions) support in ROM**
- **Support for DPMS (display power management signaling) in ROM**
- **VESA® monitor timing-compliant**
- **DDC1/2B support**

UTILITIES

- **Graphics and video diagnostics test**
- **Windows® NT™ and DOS utilities**
- **Video mode configuration utility — CLMODE**
- **Set resolution in Windows® utility — WINMODE**
- **Configurable system integration for OEMs — OEMSI**

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Revision History

The following are the differences between the December 1995 and November 1996 versions of this data book:

- Information pertaining to the Revision B device has been added

CONVENTIONS

Abbreviations

Symbol	Units of measure
°C	degree Celsius
Hz	hertz (cycles per second)
Kbyte	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbyte	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
µF	microfarad
µs	microsecond (1,000 nanoseconds)
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
pV	picovolt

The use of 'tbd' indicates values that are 'to be determined', 'n/a' designates 'not available', and 'n/c' indicates a pin that is a 'no connect'.

Numeric Naming

Hexadecimal numbers are represented with all letters in upper case and a lower-case 'h' is appended to them (for example, '14h', '3A7h', and 'C000h' are hexadecimal numbers). Binary numbers are represented with a lower-case 'b' appended. Numbers not indicated by a 'b' or an 'h' are decimal.

Acronyms

Acronym	Definition
AC	alternating current
ALU	arithmetic logic unit
ATE	automatic test equipment
BIOS	basic input/output system
BitBLT, BLT	bit boundary block transfer
bpp	bits per pixel
CAD	computer-aided design
CAS	column address strobe
CGA	color graphics adapter

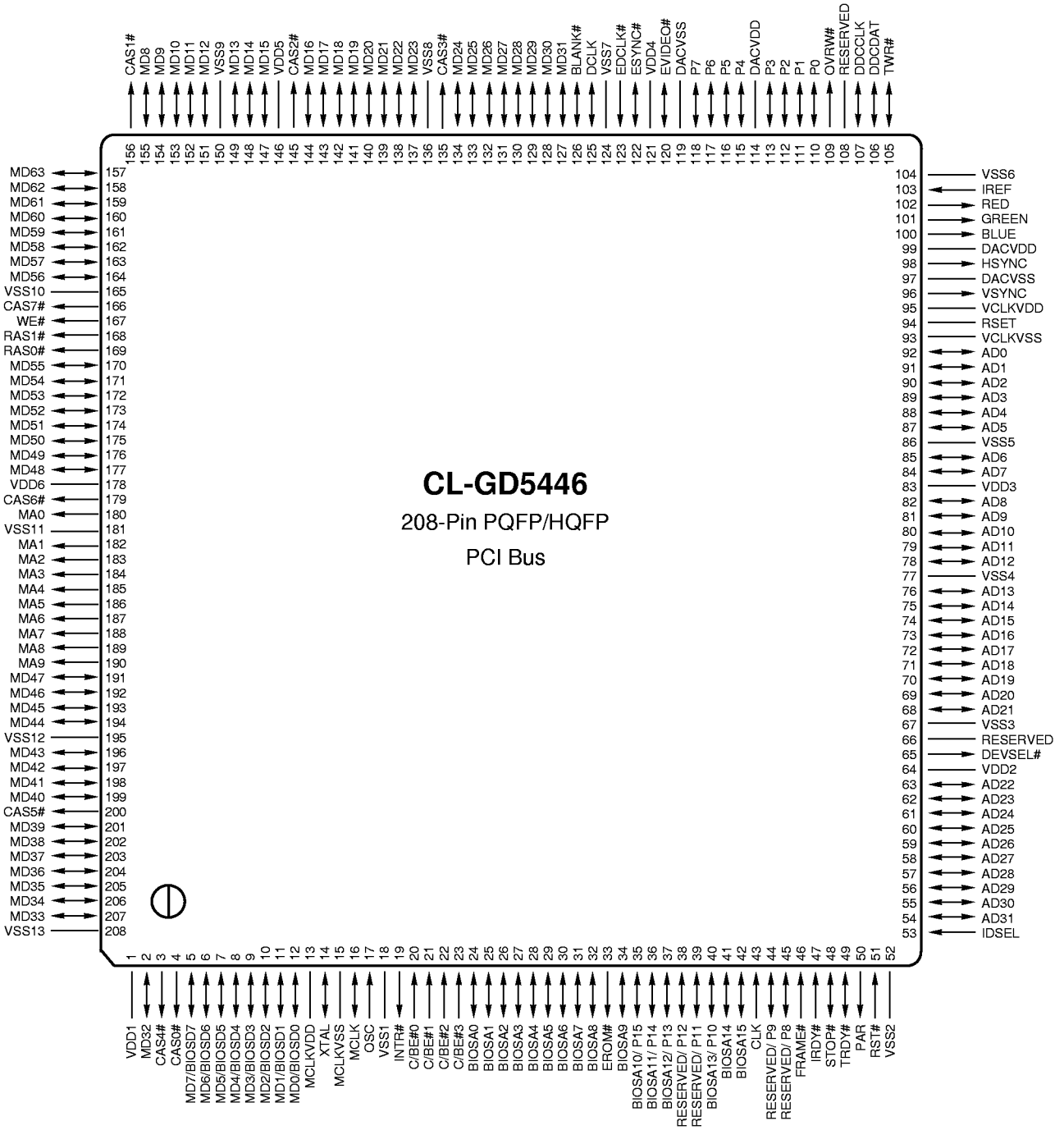
Acronym	Definition
CLUT	color lookup table
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
CRT	cathode ray tube
CRTC	CRT controller
DAC	digital-to-analog converter
DC	direct current
DDA	digital differential algorithm

Acronym	Definition
DDC	display data channel
DMI	desktop management signaling
DPMS	display power management signaling
DRAM	dynamic random access memory
dword	doubleword
EEPROM	electrically erasable/programmable read-only memory
EGA	enhanced graphics adapter
EPROM	electrically programmable read-only memory
EVAFC	extended VESA® advanced feature connector
FIFO	first in/first out
GPIO	general-purpose IO
GSC	graphics system controller
GUI	graphical user interface
HDR	Hidden DAC register
HRQ	host read queue
HSYNC/VSYNC	horizontal/vertical synchronization
HWQ	host write queue
IC	integrated circuit
I/O	input/output
LBI	local bus interface
LSB	least-significant bit
LUT	lookup table
MA	memory arbiter
MC	memory controller
MCC	monochrome-to-color converter
MD	memory data
MMI/O	memory-mapped I/O
MSB	most-significant bit
OFU	operand fetch unit
OSU	operand storage unit

Acronym	Definition
PCI	peripheral component interconnect
PFS	programmable frequency synthesizer
PLL	phase-locked loop
PQFP	plastic quad-flat pack
qword	two dwords
RAC	Rambus® access channel
RAM	random-access memory
RAS	row address strobe
RDRAM	Rambus® dynamic random-access memory
RGB	red, green, and blue
RIF	Rambus® interface
ROPs	raster operations
RSU	result storage unit
R/W	read/write
SC	serial clock
SG	signature generator
SGRAM	synchronous graphics RAM
SRAM	static random-access memory
TSR	terminate and stay resident
TTL	transistor-transistor logic
VBE	VESA BIOS extensions
VBI	vertical blanking interval
VDD	virtual device driver
VESA®	Video Electronics Standards Association
VGA	video graphics array
VL	VESA® local
VPM	video port manager
VRAM	video random-access memory
WE	transparency write enable

1. PIN INFORMATION

The CL-GD5446 VGA GUI controller is available in a 208-pin PQFP (plastic quad flat pack) or HQFP (high-performance quad flat pack) for the PCI bus only.



1.1 Pin Summary

The following abbreviations are used for pin types in the following tables: (I) indicates input; (O) indicates output; (O-Z) indicates tristate output; (OC) indicates open-collector output; (BIO) indicates bidirectional I/O; (I/O) indicates input or output depending on how the device is configured and programmed.

Table 1-1. Host Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	PCI	GPIO[b] Redefinition	Pixel Bus[c] Redefinition
53	I					IDSEL		
51	I					RST#		
46	I					FRAME#		
47	I					IRDY#		
43	I					CLK		
49	BIO		–3	8	240	TRDY#		
48	BIO		–3	8	240	STOP#		
50	O		–3	8	240	PAR		
65	O		–3	4	200	DEVSEL#		
19	OC		(OC)	24	200	INTR#		
54	BIO		–3	12	240	AD31		
55	BIO		–3	12	240	AD30		
56	BIO		–3	12	240	AD29		
57	BIO		–3	12	240	AD28		
58	BIO		–3	12	240	AD27		
59	BIO		–3	12	240	AD26		
60	BIO		–3	12	240	AD25		
61	BIO		–3	12	240	AD24		
62	BIO		–3	12	240	AD23		
63	BIO		–3	12	240	AD22		
68	BIO		–3	12	240	AD21		
69	BIO		–3	12	240	AD20		
70	BIO		–3	12	240	AD19		
71	BIO		–3	12	240	AD18		
72	BIO		–3	12	240	AD17		
73	BIO		–3	12	240	AD16		

Table 1-1. Host Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	PCI	GPIO[b] Redefinition	Pixel Bus[c] Redefinition
74	BIO		–3	12	240	AD15		
75	BIO		–3	12	240	AD14		
76	BIO		–3	12	240	AD13		
78	BIO		–3	12	240	AD12		
79	BIO		–3	12	240	AD11		
80	BIO		–3	12	240	AD10		
81	BIO		–3	12	240	AD9		
82	BIO		–3	12	240	AD8		
84	BIO		–3	12	240	AD7		
85	BIO		–3	12	240	AD6		
87	BIO		–3	12	240	AD5		
88	BIO		–3	12	240	AD4		
89	BIO		–3	12	240	AD3		
90	BIO		–3	12	240	AD2		
91	BIO		–3	12	240	AD1		
92	BIO		–3	12	240	AD0		
23	I					C/BE#3		
22	I					C/BE#2		
21	I					C/BE#1		
20	I					C/BE#0		
42	I/O		–3	8	50	BIOSA15	GPA1	
41	I/O		–3	8	50	BIOSA14	GPA0	
40	I/O		–3	8	50	BIOSA13	GPD10	P10
37	I/O		–3	8	50	BIOSA12	GPD13	P13
36	I/O		–3	8	50	BIOSA11	GPD14	P14
35	I/O		–3	8	50	BIOSA10	GPD15	P15
34	I/O		–3	8	50	BIOSA9	GPIOWR#	
32	I/O		–3	8	50	BIOSA8	GPIORD#	
31	I/O		–3	8	50	BIOSA7	GPD7	
30	I/O		–3	8	50	BIOSA6	GPD6	

Table 1-1. Host Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	PCI	GPIO[b] Redefinition	Pixel Bus[c] Redefinition
29	I/O		–3	8	50	BIOSA5	GPD5	
28	I/O		–3	8	50	BIOSA4	GPD4	
27	I/O		–3	8	50	BIOSA3	GPD3	
26	I/O		–3	8	50	BIOSA2	GPD2	
25	I/O		–3	8	50	BIOSA1	GPD1	
24	I/O		–3	8	50	BIOSA0	GPD0	
66	I/O		–3	8	50	Reserved	GPRDY/DT	
45	I/O		–3	8	50	Reserved	GPD8	P8
44	I/O		–3	8	50	Reserved	GPD9	P9
39	I/O		–3	8	50	Reserved	GPD11	P11
38	I/O		–3	8	50	Reserved	GPD12	P12

[a] Indicates nominal 250-kΩ pull-up resistor.

[b] See Appendix B11 for additional information on the general-purpose I/O port.

[c] See the definition of register GR18[6].

Table 1-2. Video Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name	V-Port™ Redefinition
96	O-Z		–12	24	50	VSYNC	
98	O-Z		–12	24	50	HSYNC	
126	I/O		–12	12	50	BLANK#	HREF Input
35	I/O		–3	8	50	P15[b]	PIXD15
36	I/O		–3	8	50	P14[b]	PIXD14
37	I/O		–3	8	50	P13[b]	PIXD13
38	I/O		–3	8	50	P12[b]	PIXD12
39	I/O		–3	8	50	P11[b]	PIXD11
40	I/O		–3	8	50	P10[b]	PIXD10
44	I/O		–3	8	50	P9[b]	PIXD9
45	I/O		–3	8	50	P8[b]	PIXD8
118	I/O		–12	12	50	P7	PIXD7
117	I/O		–12	12	50	P6	PIXD6

Table 1-2. Video Interface *(cont.)*

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name	V-Port™ Redefinition
116	I/O		–12	12	50	P5	PIXD5
115	I/O		–12	12	50	P4	PIXD4
113	I/O		–12	12	50	P3	PIXD3
112	I/O		–12	12	50	P2	PIXD2
111	I/O		–12	12	50	P1	PIXD1
110	I/O		–12	12	50	P0	PIXD0
125	I/O		–12	12	50	DCLK	PIXCLK Input
122	I/O	●	–12	12		ESYNC#	(Prog. Output 1)
120	I/O	●	–12	12		EVIDEO#	VACT Input
123	I	●				EDCLK#	VREF Input
102	Analog Out					RED	
101	Analog Out					GREEN	
100	Analog Out					BLUE	
103	Analog In					IREF	
94	Analog In					RSET	

[a] ● indicates the presence of an internal 250-kΩ ±50% pull-up resistor.

[b] P[15:8] are redefined PCI pins. See the definition of register GR18[6].

Table 1-3. Display Memory Interface

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
168	O		–12	12	50	RAS1#
169	O		–12	12	50	RAS0#
166	O		–12	12	50	CAS7#
179	O		–12	12	50	CAS6#
200	O		–12	12	50	CAS5#
3	O		–12	12	50	CAS4#
135	O		–12	12	50	CAS3#
145	O		–12	12	50	CAS2#
156	O		–12	12	50	CAS1#
4	O		–12	12	50	CAS0#

Table 1-3. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
167	O		–12	12	150	WE#
190	O		–12	12	150	MA9
189	O		–12	12	150	MA8 [b]
188	O		–12	12	150	MA7
187	O		–12	12	150	MA6
186	O		–12	12	150	MA5
185	O		–12	12	150	MA4
184	O		–12	12	150	MA3
183	O		–12	12	150	MA2
182	O		–12	12	150	MA1
180	O		–12	12	150	MA0 [c]
157	I/O	●	–8	8	50	MD63
158	I/O	●	–8	8	50	MD62
159	I/O	●	–8	8	50	MD61
160	I/O	●	–8	8	50	MD60
161	I/O	●	–8	8	50	MD59
162	I/O	●	–8	8	50	MD58
163	I/O	●	–8	8	50	MD57
164	I/O	●	–8	8	50	MD56
170	I/O	●	–8	8	50	MD55
171	I/O	●	–8	8	50	MD54
172	I/O	●	–8	8	50	MD53
173	I/O	●	–8	8	50	MD52
174	I/O	●	–8	8	50	MD51
175	I/O	●	–8	8	50	MD50
176	I/O	●	–8	8	50	MD49
177	I/O	●	–8	8	50	MD48
191	I/O	●	–8	8	50	MD47
192	I/O	●	–8	8	50	MD46
193	I/O	●	–8	8	50	MD45
194	I/O	●	–8	8	50	MD44

Table 1-3. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
196	I/O	●	–8	8	50	MD43
197	I/O	●	–8	8	50	MD42
198	I/O	●	–8	8	50	MD41
199	I/O	●	–8	8	50	MD40
201	I/O	●	–8	8	50	MD39
202	I/O	●	–8	8	50	MD38
203	I/O	●	–8	8	50	MD37
204	I/O	●	–8	8	50	MD36
205	I/O	●	–8	8	50	MD35
206	I/O	●	–8	8	50	MD34
207	I/O	●	–8	8	50	MD33
2	I/O	●	–8	8	50	MD32
127	I/O	●	–8	8	50	MD31
128	I/O	●	–8	8	50	MD30
129	I/O	●	–8	8	50	MD29
130	I/O	●	–8	8	50	MD28
131	I/O	●	–8	8	50	MD27
132	I/O	●	–8	8	50	MD26
133	I/O	●	–8	8	50	MD25
134	I/O	●	–8	8	50	MD24
137	I/O	●	–8	8	50	MD23
138	I/O	●	–8	8	50	MD22
139	I/O	●	–8	8	50	MD21
140	I/O	●	–8	8	50	MD20
141	I/O	●	–8	8	50	MD19
142	I/O	●	–8	8	50	MD18
143	I/O	●	–8	8	50	MD17
144	I/O	●	–8	8	50	MD16
147	I/O	●	–8	8	50	MD15
148	I/O	●	–8	8	50	MD14
149	I/O	●	–8	8	50	MD13

Table 1-3. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
151	I/O	●	–8	8	50	MD12
152	I/O	●	–8	8	50	MD11
153	I/O	●	–8	8	50	MD10
154	I/O	●	–8	8	50	MD9
155	I/O	●	–8	8	50	MD8
5	I/O	●	–8	8	50	MD7/BIOSD7[d]
6	I/O	●	–8	8	50	MD6/BIOSD6[d]
7	I/O	●	–8	8	50	MD5/BIOSD5[d]
8	I/O	●	–8	8	50	MD4/BIOSD4[d]
9	I/O	●	–8	8	50	MD3/BIOSD3[d]
10	I/O	●	–8	8	50	MD2/BIOSD2[d]
11	I/O	●	–8	8	50	MD1/BIOSD1[d]
12	I/O	●	–8	8	50	MD0/BIOSD0[d]

[a] ● indicates the presence of an internal 250-kΩ ±50% pull-up resistor.
[b] MA8 is connected to Memory Address 0 for asymmetric DRAMs.
[c] MA0 is connected to Memory Address 8 for asymmetric DRAMs.
[d] MD[7:0] are also used as the BIOS Data Input pins.

Table 1-4. General-Purpose I/O[a] Port

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Name	Redefined As
35	I/O	–3	8	50	BIOSA10	GPD15
36	I/O	–3	8	50	BIOSA11	GPD14
37	I/O	–3	8	50	BIOSA12	GPD13
38	I/O	–3	8	50	Reserved	GPD12
39	I/O	–3	8	50	Reserved	GPD11
40	I/O	–3	8	50	BIOSA13	GPD10
44	I/O	–3	8	50	Reserved	GPD9
45	I/O	–3	8	50	Reserved	GPD8
31	I/O	–3	8	50	BIOSA7	GPD7
30	I/O	–3	8	50	BIOSA6	GPD6
29	I/O	–3	8	50	BIOSA5	GPD5
28	I/O	–3	8	50	BIOSA4	GPD4

Table 1-4. General-Purpose I/O[a] Port

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Name	Redefined As
27	I/O	–3	8	50	BIOSA3	GPD3
26	I/O	–3	8	50	BIOSA2	GPD2
25	I/O	–3	8	50	BIOSA1	GPD1
24	I/O	–3	8	50	BIOSA0	GPD0
14	I/O	–3	8	50	XTAL	GPA6
42	I/O	–3	8	50	BIOSA15	GPA5/GPA1
41	I/O	–3	8	50	BIOSA14	GPA4/GPA0
109	O	–3	8	50	OVRW#	GPA3
105	I/O	–3	8	50	TWR#	GPA2
108	O	–3	8	50	Reserved	GPCS#
32	I/O	–3	8	50	BIOSA8	GPIORD#
34	I/O	–3	8	50	BIOSA9	GPIOWR#
66	I/O	–3	8	50	Reserved	GPRDY/DT

[a] The pins in this table are redefined to be used for the General-Purpose I/O port. See Appendix B11.

Table 1-5. V-Port™[a]

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Name	Redefined As
35	I/O	–3	8	50	BIOSA10	PIXD15
36	I/O	–3	8	50	BIOSA11	PIXD14
37	I/O	–3	8	50	BIOSA12	PIXD13
38	I/O	–3	8	50	Reserved	PIXD12
39	I/O	–3	8	50	Reserved	PIXD11
40	I/O	–3	8	50	BIOSA13	PIXD10
44	I/O	–3	8	50	Reserved	PIXD9
45	I/O	–3	8	50	Reserved	PIXD8
118	I/O	–12	12	50	P7	PIXD7
117	I/O	–12	12	50	P6	PIXD6
116	I/O	–12	12	50	P5	PIXD5
115	I/O	–12	12	50	P4	PIXD4
113	I/O	–12	12	50	P3	PIXD3
112	I/O	–12	12	50	P2	PIXD2

Table 1-5. V-Port™[a]

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Name	Redefined As
111	I/O	–12	12	50	P1	PIXD1
110	I/O	–12	12	50	P0	PIXD0
120	I/O	–12	12	50	EVIDEO#	VACT
123	I				EDCLK#	VREF
125	I/O	–12	12	50	DCLK	PIXCLK
126	I/O	–12	12	50	BLANK#	HREF

[a] The pins in this table are redefined to be used for the V-Port.

Table 1-6. Miscellaneous Pins

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name	GPIO[b] Redefinition
107	I/O		–12	12	35	DDCCLK	
106	I/O		–12	12	35	DDCDAT	
33	O		–12	12	35	EROM#	
109	O		–12	12	35	OVRW#	GPA3
105	I	●				TWR#	GPA2
108	–					Reserved	GPCS#

[a] ● indicates the presence of an internal 250-kΩ ±50% pull-up resistor.

[b] These pins are also used for the General-Purpose I/O port. See Appendix B11.

Table 1-7. Clock Synthesizer Interface

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
17	I				OSC
14	O				XTAL
16	I/O	–12	12	20	MCLK[a]

[a] Pin 16 is also used as Programmable Output 0.

Table 1-8. Power and Ground

Pin Number	Pin Type	Name	Note
178	Power	VDD6	Digital
146	Power	VDD5	Digital
121	Power	VDD4	Digital
83	Power	VDD3	Digital
64	Power	VDD2	Digital
1	Power	VDD1	Digital
208	Ground	VSS13	Digital
195	Ground	VSS12	Digital
181	Ground	VSS11	Digital
165	Ground	VSS10	Digital
150	Ground	VSS9	Digital
136	Ground	VSS8	Digital
124	Ground	VSS7	Digital
104	Ground	VSS6	Digital
86	Ground	VSS5	Digital
77	Ground	VSS4	Digital
67	Ground	VSS3	Digital
52	Ground	VSS2	Digital
18	Ground	VSS1	Digital
95	Power	VCLKVDD	VCLK
93	Ground	VCLKVSS	VCLK
13	Power	MCLKVDD	MCLK
15	Ground	MCLKVSS	MCLK
114	Power	DACVDD	DAC
99	Power	DACVDD	DAC
119	Ground	DACVSS	DAC
97	Ground	DACVSS	DAC

Table 1-9. Pins with Multiple Uses (Ordered by Pin Number)

Pin Number	PCI Name[a]	GPIO[b]	V-Port™[c]	VESA®	VMI[d] Interface	Memory Bus	Programmable I/O	Other
5	BIOSD7	–	–	–	–	MD7	–	–
6	BIOSD6	–	–	–	–	MD6	–	–
7	BIOSD5	–	–	–	–	MD5	–	–
8	BIOSD4	–	–	–	–	MD4	–	–
9	BIOSD3	–	–	–	–	MD3	–	–
10	BIOSD2	–	–	–	–	MD2	–	–
11	BIOSD1	–	–	–	–	MD1	–	–
12	BIOSD0	–	–	–	–	MD0	–	–
14	–	GPA6	–	–	–	–	–	XTAL
16	–	–	–	–	–	–	Prog. Out 0	MCLK
24	BIOSA0	GPD0	–	–	HD[0]	–	–	–
25	BIOSA1	GPD1	–	–	HD[1]	–	–	–
26	BIOSA2	GPD2	–	–	HD[2]	–	–	–
27	BIOSA3	GPD3	–	–	HD[3]	–	–	–
28	BIOSA4	GPD4	–	–	HD[4]	–	–	–
29	BIOSA5	GPD5	–	–	HD[5]	–	–	–
30	BIOSA6	GPD6	–	–	HD[6]	–	–	–
31	BIOSA7	GPD7	–	–	HD[7]	–	–	–
32	BIOSA8	GPIORD#	–	–	RD#	–	–	–
34	BIOSA9	GPIOWR#	–	–	WR#	–	–	–
35	BIOSA10	GPD15	PIXD15	P15	–	–	–	–
36	BIOSA11	GPD14	PIXD14	P14	–	–	–	–
37	BIOSA12	GPD13	PIXD13	P13	–	–	–	–
38	–	GPD12	PIXD12	P12	–	–	–	–
39	–	GPD11	PIXD11	P11	–	–	–	–
40	BIOSA13	GPD10	PIXD10	P10	–	–	–	–
41	BIOSA14	GPA0	–	–	HA[0]	–	–	–
42	BIOSA15	GPA1	–	–	HA[1]	–	–	–
44	–	GPD9	PIXD9	P9	–	–	–	–
45	–	GPD8	PIXD8	P8	–	–	–	–

Table 1-9. Pins with Multiple Uses (Ordered by Pin Number) *(cont.)*

Pin Number	PCI Name[a]	GPIO[b]	V-Port™[c]	VESA®	VMI[d] Interface	Memory Bus	Programmable I/O	Other
66	–	GPDRY/DT	–	–	GPRDY	–	–	–
105	–	GPA2	–	–	HA[2]	–	–	TWR#
108	–	GPCS#	–	–	CS#	–	–	–
109	–	GPA3	–	–	HA[3]	–	–	OVRW#
110	–	–	PIXD0	P0	–	–	–	–
111	–	–	PIXD1	P1	–	–	–	–
112	–	–	PIXD2	P2	–	–	–	–
113	–	–	PIXD3	P3	–	–	–	–
115	–	–	PIXD4	P4	–	–	–	–
116	–	–	PIXD5	P5	–	–	–	–
117	–	–	PIXD6	P6	–	–	–	–
118	–	–	PIXD7	P7	–	–	–	–
120	–	–	VACT	EVIDEO#	–	–	–	–
122	–	–	–	ESYNC#	–	–	Prog. Out 1	–
123	–	–	VREF	EDCLK#	–	–	–	–
125	–	–	PIXCLK	DCLK	–	–	–	–
126	–	–	HREF	BLANK#	–	–	–	–

[a] These functions are enabled when the BIOS is enabled in PCI30.
[b] GPIO is configured with CF8, CF4, CF3 (Revision A only).
[c] These pins are configured for V-Port in CR50[4] and CR50[1:0].
[d] These are the pin names on the VMI interface for reference only.

2. FUNCTIONAL DESCRIPTION

2.1 General

The CL-GD5446 offers a VGA solution that is totally compatible with the IBM VGA standard. The CL-GD5446 includes a VGA core, 64-bit BitBLT engine, video capture and display, and on-board frequency synthesizers and palette DAC. A complete VGA motherboard solution can be implemented by using two 256K × 16 DRAMs with the CL-GD5446.

Figure 2-1 presents a functional block diagram of the CL-GD5446, showing the connections to the host, display memory, V-Port, and monitor.

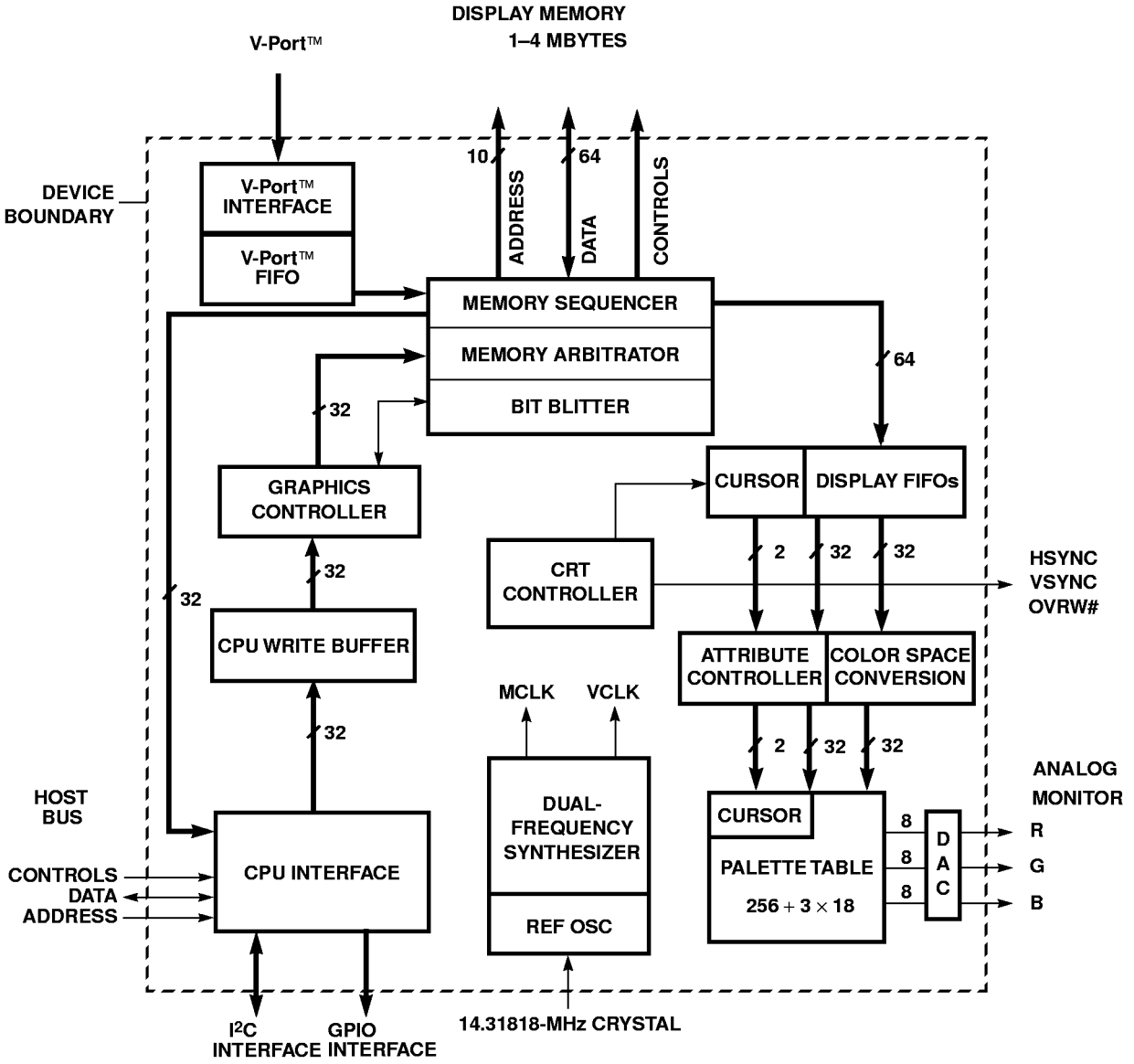


Figure 2-1. CL-GD5446 Functional Block Diagram

2.2 Functional Blocks

The following sections describe functional blocks that are integrated into the CL-GD5446.

2.2.1 CPU Interface

The CL-GD5446 connects directly to the PCI bus with no glue logic. The CL-GD5446 decodes the entire 32-bit address so that no address mirroring occurs. The CL-GD5446 interface executes 32-bit I/O and memory accesses at a speed of up to 33 MHz. The CL-GD5446 also supports memory burst cycles. The CL-GD5446 can support an additional peripheral device while remaining fully compliant with the PCI single-load specification. The CL-GD5446 is PCI 2.1-compliant.

Revision B of the CL-GD5446 has two 16-Mbyte windows into the frame buffer for compliance with PC97.

2.2.2 CPU Write Buffer

The CL-GD5446 has a multi-level 32-bit CPU write buffer which dramatically increases GUI acceleration and enhances CPU performance. The CPU write buffer contains a queue of CPU write accesses to display memory or the BitBLT engine that have not been executed because frame buffer bandwidth has not yet been available. Maintaining a queue allows the CL-GD5446 to generate TRDY# to complete the bus cycle as soon as it has recorded the address and data, and then to execute the operation when display memory cycles are available.

2.2.3 Graphics Controller

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and miscellaneous operations. These operations are typically performed in the graphics controller for VGA-compatible applications; newer applications take advantage of the BitBLT engine.

2.2.4 BitBLT Engine

The CL-GD5446 has a 64-bit BitBLT engine that supports color expansion with or without transparency for all graphics pixel sizes as well as transparency without color expansion for 8- and 16-bpp graphics formats.

The Control registers for the BitBLT engine are memory-mapped and double-buffered. Memory-mapping the Control registers allows the fastest possible parameter transfer. Double-Buffered Control registers and the AutoStart feature provide the greatest possible degree of parallelism between the host and the BitBLT engine.

2.2.5 Memory Arbitrator

The memory arbitrator allocates bandwidth to the four functions that compete for the frame buffer bandwidth: DRAM refresh, screen refresh, V-Port writes, and CPU and BitBLT access.

DRAM refresh is handled invisibly by allocating a selectable number of CAS#-before-RAS# refresh cycles at the beginning of each scanline. Screen refresh, V-Port writes, and CPU/BitBLT access are allocated cycles according to the FIFO control parameters. Priority is given to screen refresh and V-Port writes.

2.2.6 Memory Sequencer

The memory sequencer generates timing for display memory. The CL-GD5446 can be configured to generate timing optimized for EDO (extended data output) DRAMS with MCLK programmable up to 80 MHz. The control signals from the CL-GD5446 to the DRAM are RAS#, CAS#, WE#, and the multiplexed address bus. The sequencer generates CAS#-before-RAS# refresh cycles, random read and random early write cycles, Fast-Page mode read and early write cycles, and EDO read cycles. The memory sequencer can generate addresses for symmetric or asymmetric DRAMs.

2.2.7 CRT Controller

The CRT controller generates all the timing required by the monitor including HSYNC, HSYNC, and BLANK#. The sync signals have programmable polarity and can be forced static for monitor power management. The CL-GD5446 BIOS supports all standard VGA modes, as well as extended resolutions up to 1280 × 1024. The CL-GD5446 supports a hardware video window for video playback.

2.2.8 Display FIFOs

The display FIFOs allow data from the frame buffer to be fetched before it is actually needed for screen refresh. This allows the fetches to be executed as EDO Fast-Page mode read cycles rather than random read cycles, greatly increasing the available memory bandwidth. The CL-GD5446 has two display FIFOs, allowing information from two independent sources streams to be mixed together in the display pipeline. This is necessary for occlusion support and also for Y-interpolation.

2.2.9 Attribute Controller

The attribute controller formats the display for the screen (primarily text modes). Display color selection, text blinking, and underlining are performed by the attribute controller. Alternate font selection also occurs in the attribute controller.

2.2.10 V-Port™

The CL-GD5446 V-Port writes realtime or recorded video from a decoder to the frame buffer, typically for display in the video window. Video can be converted to AccuPak™ or can be decimated vertically and horizontally. When video is being captured for display in the window, the capture and display buffers can be automatically swapped as each frame is captured. This prevents the display of partial frames with a minimum of host intervention.

The CL-GD5446 has an independent capture FIFO. This allows video capture to occur at the same time interpolated Y-zooming or occlusion is being used.

Luminance-only capture is available for TeleText and closed caption with suitable software.

The V-Port hardware interface uses the same pins as the VGA pass-through connector. It can be configured for an 8- or 16-bit pixel bus and for either active sense of HREF.

2.2.11 Hardware Video Window

The CL-GD5446 features a programmable hardware window for the simultaneous display of graphics and video. The graphics and video formats can have different color spaces and even pixel sizes. The display of 8-bpp palettized graphics with YUV 4:2:2 graphics is a typical application.

The video can be independently zoomed in the horizontal and vertical directions up to 4×. Horizontal zooming is always done with interpolation of 'in-between' pixels. Vertical zooming can be done with scanline replication. Scanline interpolation can be used for vertical zooming at 2× or greater (subject to frame buffer bandwidth limitations).

Occlusion support allows the graphics and video streams to be mixed on a pixel-by-pixel basis. Color key matching of the graphics source or chroma key matching of the video source can be used to determine which pixels are replaced. Occlusion is supported for 8- and 16-bpp graphics. Occlusion and Y-zoom with interpolation are mutually exclusive.

2.2.12 Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts an 8-bit color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

Alternatively, the CL-GD5446 can be configured for 8-, 15-, 16-, or 24-bit direct color RGB pixels. This allows 256, 32K, 64K, or 16M simultaneous colors to be displayed on the screen.

The CL-GD5446 also supports YUV 4:2:2 and AccuPak formats within the video window.

The palette DAC supports a Power-Down mode which temporarily turns off clocks to the palette and power to the DAC to conserve power.

2.2.13 Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the memory sequencer and display clocks from a single reference frequency. The frequency of each clock is independently programmable. The maximum memory sequencer clock and display clock are 80 MHz and 135 MHz, respectively. The reference frequency of 14.31818 MHz can be generated on-chip using an inexpensive 2-pin crystal or it can be supplied from an external TTL source.

2.2.14 VESA®/VGA Pass-Through Connector

The CL-GD5446 can connect directly to a VESA connector for input or output. The device supports the three enable/disable inputs; the Pixel bus can drive the connector directly.

2.2.15 General-Purpose I/O Port

The CL-GD5446 can support an additional peripheral device on its adapter card. Address decoding and data buffering allow the additional device while maintaining the PCI 'single-load' specification.

2.2.16 I²C Interface

The CL-GD5446 has a built-in two pin interface that can be used to control peripheral devices such as TV tuners. This interface can also be used for DDC2B monitor identification.

2.3 Performance

The CL-GD5446 is designed with the following performance-enhancing features:

- 64-bit display memory data bus for faster access to display memory
- Memory-mapped, double-buffered BitBLT registers with autostart maximizes host/BLT overlap
- Transparent source BitBLT for increased BLT functionality
- DRAM timing configurable for EDO operations for faster access to display memory
- 80-MHz MCLK provides 320-Mbyte/second peak frame-buffer bandwidth
- Burst host bus performance and a CPU write buffer that allows faster CPU access for writes to display memory
- Increased throughput with PCI local bus interface with Burst mode
- 32-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 16- or 32-bit CPU interface to I/O registers for faster host access
- Multi-level, 32-bit system memory write cache
- 32-bit internal data inputs for internal DAC
- Two display FIFOs to minimize memory contention
- Video capture decimation to reduce the memory bandwidth requirements
- YUV planar assist and AccuPak™ reduce codec CPU processing, increasing host bus and memory bus transfer rates
- 32 × 32 and 64 × 64 hardware cursor to improve Microsoft® Windows® performance

2.4 Compatibility

The CL-GD5446 includes all registers and data paths required for VGA controllers, and is upward-compatible with the CL-GD542X family.

The CL-GD5446 supports extensions to VGA, including 1024 × 768 × 16M interlaced, 1024 × 768 × 64K interlaced and non-interlaced, and 1280 × 1024 × 256 interlaced and non-interlaced modes.

Production Revision B of the CL-GD5446 is compliant with PC97.

2.5 Board Testability

The CL-GD5446 device is testable, even when installed on a printed circuit board. By using Pin-Scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace, is detected (see Appendix B7, "Pin Scan" in the *CL-GD5446 Technical Reference Manual*).The signature generator allows the entire system, including the display memory, to be tested at speed (see Appendix B6, "Signature Generator" in the *CL-GD5446 Technical Reference Manual*). The CL-GD5446 enhanced signature generator test allows the BitBLT engine, the V-Port, as well as the frame buffer to be tested.

3. CONFIGURATION TABLES

3.1 Graphics Modes

Table 3-1. IBM® Standard VGA Display Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
6	6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
E	E	16/256K	80 × 25	8 × 14	640 × 200	Graphics	25	31.5	70
F	F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12	12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	35.8	43.3	85
13	13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70

NOTE: The EGA-compatible text modes (which use an 8 × 14 font) and graphics modes 10 and F use a 16-dot high font, with the bottom two lines truncated, in the absence of TSRFONT (8 × 14 font TSR). This creates some errors when displaying characters with descenders, but does not restrict operation of programs using these modes. In text modes using the 8 × 14 font, the characters 'g', 'j', 'p', 'q', 'y', and 'ÿ' are truncated using a middle- and bottom-line algorithm to avoid truncation of descenders. For compatibility with some DOS applications using the 8 × 14 font, the TSRFONT utility should be used. Applications such as DOSSHELL, in Graphics 25 or 34 line display modes, require the TSRFONT utility to be loaded.

Table 3-2. Cirrus Logic Extended Display Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	56.25	53.7	85
5D†	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	36	43.3	85
60†	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	94.5	68.3	85
64	111	64K	–	–	640 × 480	Graphics	25	31.5	60
64	111	64K	–	–	640 × 480	Graphics	31.5	37.9	72
64	111	64K	–	–	640 × 480	Graphics	31.5	37.5	75
64	111	64K	–	–	640 × 480	Graphics	36	43.3	85

Table 3-2. Cirrus Logic Extended Display Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
65	114	64K	–	–	800 × 600	Graphics	36	35.2	56
65	114	64K	–	–	800 × 600	Graphics	40	37.8	60
65	114	64K	–	–	800 × 600	Graphics	50	48.1	72
65	114	64K	–	–	800 × 600	Graphics	49.5	46.9	75
65	114	64K	–	–	800 × 600	Graphics	56.25	53.7	85
66	110	32K‡	–	–	640 × 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.9	72
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.5	75
66	110	32K‡	–	–	640 × 480	Graphics	36	43.3	85
67	113	32K‡	–	–	800 × 600	Graphics	36	35.2	56
67	113	32K‡	–	–	800 × 600	Graphics	40	37.8	60
67	113	32K‡	–	–	800 × 600	Graphics	50	48.1	72
67	113	32K‡	–	–	800 × 600	Graphics	49.5	46.9	75
67	113	32K‡	–	–	800 × 600	Graphics	56.25	53.7	85
68†	116	32K‡	–	–	1024 × 768	Graphics	44.9	35.5	43i†
68	116	32K‡	–	–	1024 × 768	Graphics	65	48.3	60
68	116	32K‡	–	–	1024 × 768	Graphics	75	56	70
68	116	32K‡	–	–	1024 × 768	Graphics	78.7	60	75
68	116	32K‡	–	–	1024 × 768	Graphics	94.5	68.3	85
6C†	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D†	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	108	65	60
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	135	80	75
71	112	16M	–	–	640 × 480	Graphics	25	31.5	60
71	112	16M	–	–	640 × 480	Graphics	31.5	37.9	72
71	112	16M	–	–	640 × 480	Graphics	31.5	37.5	75
71	112	16M	–	–	640 × 480	Graphics	36	43.3	85
74†	117	64K	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74	117	64K	–	–	1024 × 768	Graphics	65	48.3	60

Table 3-2. Cirrus Logic Extended Display Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
74	117	64K	–	–	1024 × 768	Graphics	75	56	70
74	117	64K	–	–	1024 × 768	Graphics	78.7	60	75
74	117	64K	–	–	1024 × 768	Graphics	94.5	68.3	85
75†	11A	64K	–	–	1280 × 1024	Graphics	75	48	43i†
78	115	16M	–	–	800 × 600	Graphics	36	35.2	56
78	115	16M	–	–	800 × 600	Graphics	40	37.8	60
78	115	16M	–	–	800 × 600	Graphics	50	48.1	72
78	115	16M	–	–	800 × 600	Graphics	49.5	46.9	75
78	115	16M	–	–	800 × 600	Graphics	56.25	53.7	85
79	118	16M	–	–	1024 × 768	Graphics	44.9	35.5	43i†
79	118	16M	–	–	1024 × 768	Graphics	65	48.3	60
79	118	16M	–	–	1024 × 768	Graphics	75	56	70
79	118	16M	–	–	1024 × 768	Graphics	78.7	60	75
79	118	16M	–	–	1024 × 768	Graphics	94.5	68.3	85
7B	–	256/256K	–	–	1600 × 1200	Graphics	135	62.5	48i†
7C	–	256/256K	144 × 54	8 × 16	1152 × 864	Graphics	94.5	63.9	70
7C	–	256/256K	144 × 54	8 × 16	1152 × 864	Graphics	108	67.5	75

NOTES:

1) '‡' character indicates 32K Direct-Color/256-Color Mixed mode.
2) †' character indicates Interlaced mode.
3) Some modes and some refresh rates are not supported by the CL-GD5446. Refer to the CL-GD5446 Software Release Kit for the list of display modes supported by the CL-GD5446 BIOS. Also see the inside front cover of this manual.
4) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected is automatically used.
5) The CL-GD5446 can support 132-column text modes, not included in the BIOS.

3.2 Configuration Register, CF

When RESET (system power-on reset) is active, the CL-GD5446 samples the levels on several of the Display Memory Data (MD[63:48]) pins. These levels are latched into a write-only Configuration register (CF1). This register controls some fundamental operating modes of the CL-GD5446.

The levels on the Memory Data bus default to a logic '1' during power-on reset because of internal 250-kΩ pull-up resistors. A logic '0' is achieved by installing an external 6.8-kΩ pull-down resistor on the memory data line corresponding to the appropriate bit in the Configuration register. Refer to Appendix B5, "Configuration Notes", in this manual. Table 3-3 summarizes the Configuration register.

Table 3-3. Configuration Register Bits

Memory Data Bit	Pin Number	CF Bits	Level	Description
MD63	157	15	0 1	Enable Pin-Scan test Disable Pin-Scan test
MD62	158	14	0 1	PCI3C[8] = 1 (interrupt claimed) PCI3C[8] = 0 (interrupt not claimed)
MD61	159	13	–	Reserved
MD60	160	12	–	Used with CF5 to define MCLK
MD59	161	11	0 1	Asymmetric DRAM (RAS*/CAS* addressing) Symmetric DRAM (RAS*/CAS* addressing)
MD58	162	10	–	Pull-down resistor required (CAS steering)
MD57	163	9	0 1	7-MCLK RAS* cycle 6-MCLK RAS* cycle
MD56	164	8	–	Used with CF4 to define GPIO, VGA register relocation Revision A only. See Appendix A2 for Revision B silicon.
MD55	170	7	–	Reserved
MD54	171	6	0 1	Feature Connector pins (P[7:0], BLANK#, DCLK) disabled Feature Connector pins normal operation
MD53	172	5	–	Used with CF12 to define MCLK
MD52	173	4	–	Used with CF8 to define GPIO, VGA register relocation Revision A only. See Appendix A2 for Revision B silicon.
MD51	174	3	0 1	Enable PCI14 for GPIO, VGA register relocation Disable PCI14 (no GPIO, VGA register relocation)
MD50, MD49, MD48	141, 142, 143	2, 1, 0	000 001 010 011 100 110 111	Reserved Reserved Reserved Reserved PCI bus Reserved (VESA VL-Bus, reference only) Reserved

4. VGA REGISTER PORT MAP

Table 4-1. VGA Register Port Map

Address	Port	VESA® VL-Bus™ Note[a]
94	POS 102 Access Control (3C3 sleep)	✔
102	POS102 register	✔
3B4	CRT Controller Index (R/W — monochrome)	
3B5	CRT Controller Data (R/W — monochrome)	
3BA	Feature Control (W), Input Status Register 1 (R — monochrome)	
3C0	Attribute Controller Index/Data (Write)	
3C1	Attribute Controller Index/Data (Read)	
3C2	Miscellaneous Output (W), Input Status Register 0 (R)	
3C3	Motherboard Sleep	
3C4	Sequencer Index (R/W)	
3C5	Sequencer Data (R/W)	
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register (R/W)	
3C7	Pixel Address Read Mode (W), DAC State (R)	
3C8	Pixel Mask Write Mode (R/W)	
3C9	Pixel Data (R/W)	
3CA	Feature Control Readback (R)	
3CC	Miscellaneous Output Readback (R)	
3CE	Graphics Controller Index (R/W)	
3CF	Graphics Controller Data (R/W)	
3D4	CRT Controller Index (R/W — color)	
3D5	CRT Controller Data (R/W — color)	
3DA	Feature Control (W), Input Status Register 1 (R — color)	
46E8	Adapter Sleep	✔

[a] These registers are available only when the CL-GD5446 is configured for VESA VL-Bus. The CL-GD5446 is not available for VESA VL-Bus.

5. REGISTER MAP

All CL-GD5446 registers are listed in Table 5-1. Page numbers in the Page column refer to the register description chapters later in this manual. The registers that have a (V) in the I/O port column are for the VESA VL-Bus and are listed for reference only. Registers at I/O port 3Dxh are at 3Bxh when the CL-GD5446 is programmed for Monochrome mode (MISC[0] = 0).

Table 5-1. CL-GD5446 Registers

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
MISC	Miscellaneous Output (write only)	3C2h	–	–	4-9
	Miscellaneous Output (read only)	3CCh	–	–	4-9
FC	Feature Control (write only)	3DAh	–	–	4-11
	Feature Control (read only)	3CAh	–	–	4-11
FEAT	Input Status Register 0	3C2h	–	–	4-12
STAT	Input Status Register 1	3DAh	–	–	4-13
–	Pixel Mask	3C6h	–	–	4-14
–	Palette Address (Read mode) (write only)	3C7h	–	–	4-15
–	DAC State (read only)	3C7h	–	–	4-16
–	Palette Address (Write mode)	3C8h	–	–	4-17
–	Palette Data	3C9h	–	–	4-18
HDR	Hidden DAC Register	3C6h	–	–	8-52
PCI00	PCI Device/Vendor ID	00h	–	–	7-3
PCI04	PCI Status/Command	04h	–	–	7-4
PCI08	PCI Class Code	08h	–	–	7-5
PCI10	PCI Display Memory Base Address	10h	–	–	7-6
PCI14	PCI Relocatable I/O and GPIO Base Address (Revision A)	14h	–	–	7-7
PCI14	PCI VGA/BitBLT Register Base Address (Revision B)	14h	–	–	7-8
PCI18	PCI GPIO Base Address (Revision B)	18h	–	–	7-9
PCI2C	PCI Subsystem/Subsystem Vendor ID (Revision B)	2Ch	–	–	7-10
PCI30	PCI Expansion ROM Base Address	30h	–	–	7-11
PCI3C	PCI Interrupt Line	3Ch	–	–	7-12
ARX	Attribute Controller Index	3C0h/3C1h	–	–	4-72
AR0–ARF	Attribute Controller Palette	3C0h/3C1h	00h–0Fh	–	4-73
AR10	Attribute Controller Mode	3C0h/3C1h	10h	–	4-74

Table 5-1. CL-GD5446 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
AR11	Overscan (Border) Color	3C0h/3C1h	11h	–	4-76
AR12	Color Plane Enable	3C0h/3C1h	12h	–	4-77
AR13	Pixel Panning	3C0h/3C1h	13h	–	4-78
AR14	Color Select	3C0h/3C1h	14h	–	4-79
CRX	CRTC Index	3D4h	–	–	4-26
CR0	CRTC Horizontal Total	3D5h	00h	–	4-29
CR1	CRTC Horizontal Display End	3D5h	01h	–	4-30
CR2	CRTC Horizontal Blanking Start	3D5h	02h	–	4-31
CR3	CRTC Horizontal Blanking End	3D5h	03h	–	4-32
CR4	CRTC Horizontal Sync Start	3D5h	04h	–	4-34
CR5	CRTC Horizontal Sync End	3D5h	05h	–	4-35
CR6	CRTC Vertical Total	3D5h	06h	–	4-37
CR7	CRTC Overflow	3D5h	07h	–	4-38
CR8	CRTC Screen A Preset Row-Scan	3D5h	08h	–	4-39
CR9	CRTC Character Cell Height	3D5h	09h	–	4-40
CRA	CRTC Text Cursor Start	3D5h	0Ah	–	4-41
CRB	CRTC Text Cursor End	3D5h	0Bh	–	4-42
CRC	CRTC Screen Start Address High	3D5h	0Ch	–	4-43
CRD	CRTC Screen Start Address Low	3D5h	0Dh	–	4-44
CRE	CRTC Text Cursor Location High	3D5h	0Eh	–	4-45
CRF	CRTC Text Cursor Location Low	3D5h	0Fh	–	4-46
CR10	CRTC Vertical Sync Start	3D5h	10h	–	4-47
CR11	CRTC Vertical Sync End	3D5h	11h	–	4-48
CR12	CRTC Vertical Display End	3D5h	12h	–	4-50
CR13	CRTC Offset (Pitch)	3D5h	13h	–	4-51
CR14	CRTC Underline Row Scanline	3D5h	14h	–	4-52
CR15	CRTC Vertical Blank Start	3D5h	15h	–	4-53
CR16	CRTC Vertical Blank End	3D5h	16h	–	4-54
CR17	CRTC Mode Control	3D5h	17h	–	4-55
CR18	CRTC Line Compare	3D5h	18h	–	4-57
CR19	Interlace End	3D5h	19h	–	8-41
CR1A	Miscellaneous Control	3D5h	1Ah	–	8-42

Table 5-1. CL-GD5446 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR1B	Extended Display Controls	3D5h	1Bh	–	8-44
CR1C	Sync Adjust and GENLOCK	3D5h	1Ch	–	8-46
CR1D	Overlay Extended Control	3D5h	1Dh	–	8-48
CR22	Graphics Data Latches Readback (read only)	3D5h	22h	–	4-58
CR24	Attribute Controller Toggle Readback (read only)	3D5h	24h	–	4-59
CR25	Part Status (read only)	3D5h	25h	–	8-50
CR26	Attribute Controller Index Readback (read only)	3D5h	26h	–	4-60
CR27	ID (read only)	3D5h	27h	–	8-51
CR31	Video Window Horizontal Zoom Control	3D5h	31h	–	6-4
CR32	Video Window Vertical Zoom Control	3D5h	32h	–	6-5
CR33	Video Window Horizontal Region 1 Size	3D5h	33h	–	6-6
CR34	Video Window Region 2 Width	3D5h	34h	–	6-7
CR35	Video Window Region 2 Source Data Size	3D5h	35h	–	6-8
CR36	Video Window Horizontal Overflow	3D5h	36h	–	6-9
CR37	Video Window Vertical Start	3D5h	37h	–	6-10
CR38	Video Window Vertical End	3D5h	38h	–	6-11
CR39	Video Window Vertical Overflow	3D5h	39h	–	6-12
CR3A	Video Buffer 1 Start Address Byte 0	3D5h	3Ah	–	6-13
CR3B	Video Buffer 1 Start Address Byte 1	3D5h	3Bh	–	6-13
CR3C	Video Buffer 1 Start Address Byte 2	3D5h	3Ch	–	6-14
CR3D	Video Buffer Address Offset	3D5h	3Dh	–	6-15
CR3E	Video Window Master Control	3D5h	3Eh	–	6-16
CR3F	Miscellaneous Video Control	3D5h	3Fh	–	6-18
CR50	Video Capture Control	3D5h	50h	–	6-20
CR51	Video Capture Data Format	3D5h	51h	–	6-22
CR52	Video Capture Horizontal Data Reduction	3D5h	52h	–	6-23
CR53	Video Capture Vertical Data Reduction	3D5h	53h	–	6-24
CR54	Video Capture Horizontal Delay	3D5h	54h	–	6-25
CR56	Video Capture Vertical Delay	3D5h	56h	–	6-26
CR57	Video Capture Maximum Height	3D5h	57h	–	6-27
CR58	Video Capture Miscellaneous Control	3D5h	58h	–	6-28
CR59	Video Buffer 2 Start Address Byte 0	3D5h	59h	–	6-29

Table 5-1. CL-GD5446 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
CR5A	Video Buffer 2 Start Address Byte 1	3D5h	5Ah	–	6-29
CR5B	Video Window Brightness Adjust	3D5h	5Bh	–	6-30
CR5C	Luminance-Only Capture Control	3D5h	5Ch	–	6-31
CR5D	Video Window Pixel Alignment	3D5h	5Dh	–	6-32
CR5E	Double-Buffer Control	3D5h	5Eh	–	6-33
GRX	Graphics Controller Index	3CEh	–	–	4-61
GR0	Set/Reset / Background Color Byte 0	3CFh	00h	00	4-62
GR1	Set/Reset Enable / Foreground Color Byte 0	3CFh	01h	04	4-63
GR2	Graphics Controller Color Compare	3CFh	02h	–	4-64
GR3	Graphics Controller Data Rotate	3CFh	03h	–	4-65
GR4	Graphics Controller Read Map Select	3CFh	04h	–	4-66
GR5	Graphics Controller Mode	3CFh	05h	–	4-67
GR6	Graphics Controller Miscellaneous	3CFh	06h	–	4-69
GR7	Graphics Controller Color Don't Care	3CFh	07h	–	4-70
GR8	Graphics Controller Bit Mask	3CFh	08h	–	4-71
GR9	Offset Register 0	3CFh	09h	–	8-26
GRA	Offset Register 1	3CFh	0Ah	–	8-28
GRB	Graphics Controller Mode Extensions	3CFh	0Bh	–	8-29
GRC	Color Key/Chroma Key Compare	3CFh	0Ch	–	8-31
GRD	Color Key/Mask/Chroma Key	3CFh	0Dh	–	8-32
GRE	Power Management	3CFh	0Eh	–	8-33
GR10	Background Color Byte 1	3CFh	10h	01	5-3
GR11	Foreground Color Byte 1	3CFh	11h	05	5-3
GR12	Background Color Byte 2	3CFh	12h	02	5-3
GR13	Foreground Color Byte 2	3CFh	13h	06	5-3
GR14	Background Color Byte 3	3CFh	14h	03	5-3
GR15	Foreground Color Byte 3	3CFh	15h	07	5-3
GR16	Active Display Line Readback Byte 0	3CFh	16h	–	8-35
GR17	Active Display Line Readback Byte 1	3CFh	17h	–	8-36
GR18	Extended DRAM Control	3CFh	18h	–	8-37
GR19	GPIO Port Configuration	3CFh	19h	–	8-39
GR1A	Scratch Pad 4	3CFh	1Ah	–	8-40

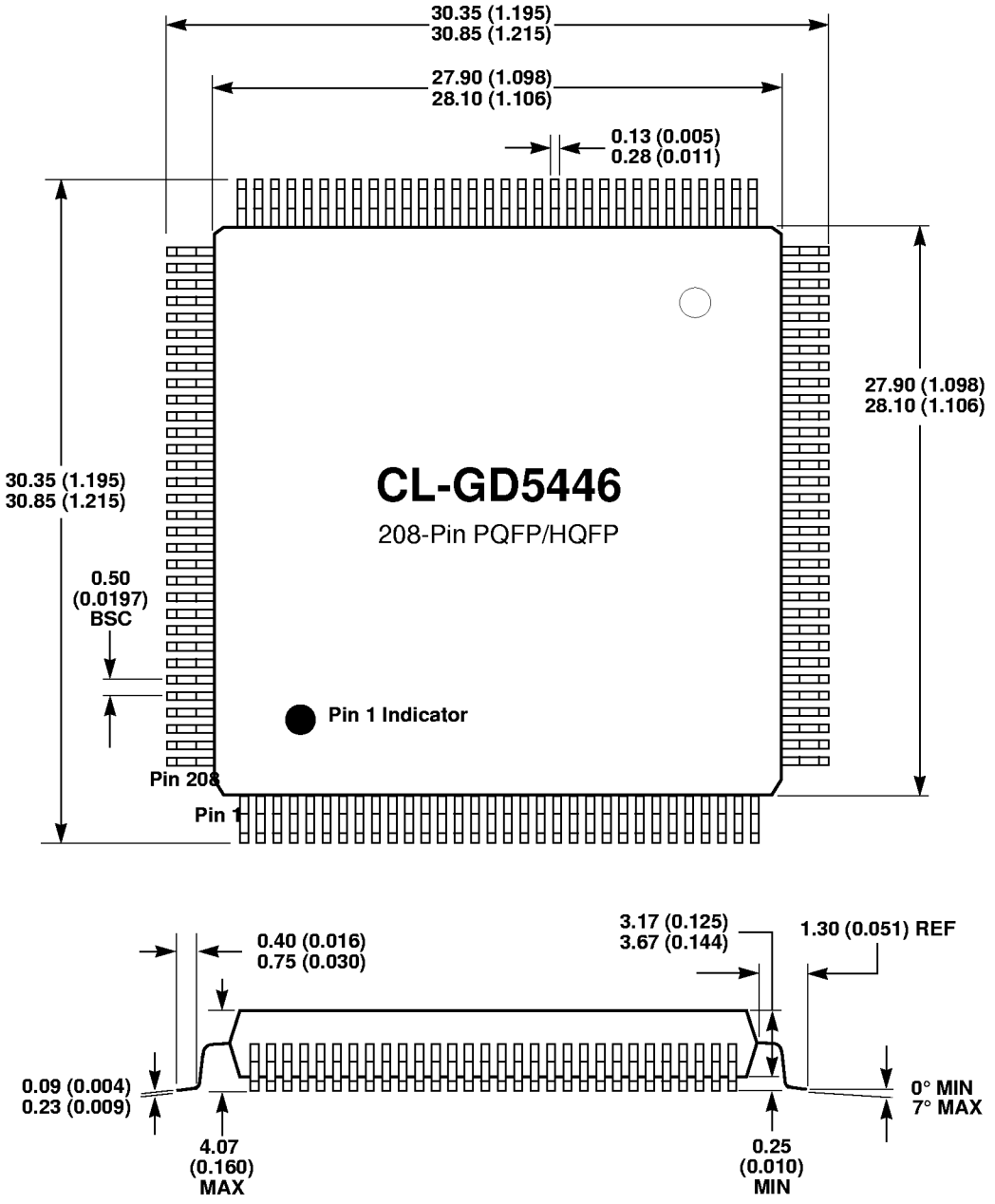
Table 5-1. CL-GD5446 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
GR1B	Scratch Pad 5	3CFh	1Bh	–	8-40
GR1C	Chroma Key – U Minimum/Green Minimum	3CFh	1Ch	–	6-35
GR1D	Chroma Key – U Maximum/Green Maximum	3CFh	1Dh	–	6-35
GR1E	Chroma Key – V Minimum/Blue Minimum	3CFh	1Eh	–	6-35
GR1F	Chroma Key – V Maximum/Blue Maximum	3CFh	1Fh	–	6-35
GR20	BLT Width Byte 0	3CFh	20h	08	5-4
GR21	BLT Width Byte 1	3CFh	21h	09	5-4
GR22	BLT Height Byte 0	3CFh	22h	0A	5-5
GR23	BLT Height Byte 1	3CFh	23h	0B	5-5
GR24	BLT Destination Pitch Byte 0	3CFh	24h	0C	5-6
GR25	BLT Destination Pitch Byte 1	3CFh	25h	0D	5-6
GR26	BLT Source Pitch Byte 0	3CFh	26h	0E	5-7
GR27	BLT Source Pitch Byte 1	3CFh	27h	0F	5-7
GR28	BLT Destination Start Byte 0	3CFh	28h	10	5-8
GR29	BLT Destination Start Byte 1	3CFh	29h	11	5-8
GR2A	BLT Destination Start Byte 2	3CFh	2Ah	12	5-8
GR2C	BLT Source Start Byte 0	3CFh	2Ch	14	5-9
GR2D	BLT Source Start Byte 1	3CFh	2Dh	15	5-9
GR2E	BLT Source Start Byte 2	3CFh	2Eh	16	5-9
GR2F	BLT Destination Left-Side Clipping	3CFh	2Fh	17	5-10
GR30	BLT Mode	3CFh	30h	18	5-11
GR31	BLT Start/Status	3CFh	31h	40	5-13
GR32	BLT ROP (Raster Operation)	3CFh	32h	1A	5-15
GR33	BLT Mode Extensions	3CFh	33h	1B	5-17
GR34	Transparent BLT Key Color Byte 0	3CFh	34h	1C	5-18
GR35	Transparent BLT Key Color Byte 1	3CFh	35h	1D	5-18
SRX	Sequencer Index	3C4h	–	–	4-19
SR0	Sequencer Reset	3C5h	00h	–	4-20
SR1	Sequencer Clocking Mode	3C5h	01h	–	4-21
SR2	Sequencer Plane Mask	3C5h	02h	–	4-22
SR3	Sequencer Character Map Select	3C5h	03h	–	4-23
SR4	Sequencer Memory Mode	3C5h	04h	–	4-25

Table 5-1. CL-GD5446 Registers *(cont.)*

Abbreviation	Register Name	I/O Port	Index	MMI/O	Page
SR6	Key	3C5h	06h	–	8-4
SR7	Extended Sequencer Mode	3C5h	07h	–	8-5
SR8	DDC2B/EEPROM Control	3C5h	08h	–	8-7
SR9	Scratch Pad 0	3C5h	09h	–	8-9
SRA	Scratch Pad 1	3C5h	0Ah	–	8-9
SRB	VCLK0 Numerator	3C5h	0Bh	–	8-10
SRC	VCLK1 Numerator	3C5h	0Ch	–	8-10
SRD	VCLK2 Numerator	3C5h	0Dh	–	8-10
SRE	VCLK3 Numerator	3C5h	0Eh	–	8-10
SRF	DRAM Control	3C5h	0Fh	–	8-11
SR10	Graphics Cursor X Position	3C5h	10h	–	8-13
SR11	Graphics Cursor Y Position	3C5h	11h	–	8-14
SR12	Graphics Cursor Attributes	3C5h	12h	–	8-15
SR13	Graphics Cursor Pattern Address Offset	3C5h	13h	–	8-16
SR14	Scratch Pad 2	3C5h	14h	–	8-17
SR15	Scratch Pad 3	3C5h	15h	–	8-17
SR16	Display FIFO Threshold Control	3C5h	16h	–	8-18
SR17	Configuration Readback and Extended Control	3C5h	17h	–	8-19
SR18	Signature Generator Control	3C5h	18h	–	8-20
SR19	Signature Generator Result Low Byte	3C5h	19h	–	8-22
SR1A	Signature Generator Result High Byte	3C5h	1Ah	–	8-23
SR1B	VCLK0 Denominator and Post Scalar	3C5h	1Bh	–	8-24
SR1C	VCLK1 Denominator and Post Scalar	3C5h	1Ch	–	8-24
SR1D	VCLK2 Denominator and Post Scalar	3C5h	1Dh	–	8-24
SR1E	VCLK3 Denominator and Post Scalar	3C5h	1Eh	–	8-24
SR1F	MCLK Select	3C5h	1Fh	–	8-25
POS94	POS102 Access Control	94h (V)	–	–	4-5
POS102	POS102	102h (V)	–	–	4-6
VSSM	3C3 (Planar) Sleep Address	3C3h (V)	–	–	4-7
VSSM	46E8 (Adapter) Sleep Address	46E8h (V)	–	–	4-8

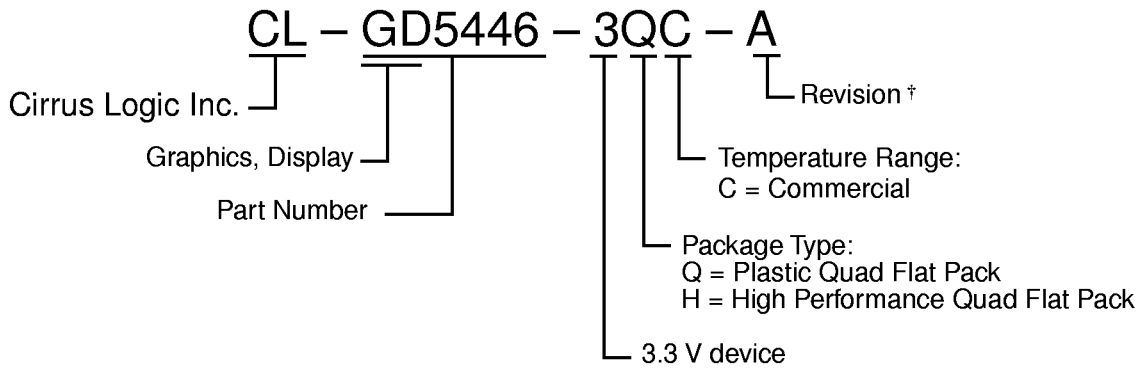
6. PACKAGE SPECIFICATIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) HQFP is a high-performance QFP with an exposed or unexposed heat sink.

7. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic. for up-to-date information on revisions.