

ELECH490 - Digital architectures and design

Labs presentation

Organisation

- **Please register to a lab serie on the UV if it is not the case yet**
- Only come to the lab sessions of the serie you are registered to
- You can work individually or per group

Organisation

4 lab sessions followed by a group project

- Lab 1 - Combinatorial circuits
- Lab 2 - Conditional assignments, Registers & Counters
- Lab 3 - State machines
- Lab 4 – Introduction to the project: the Basys3 Board

You will receive one FPGA board /group of 2 students at the beginning of Lab 4

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Lab schedule

	Lab 1	Lab 2	Lab 3	Lab 4
Series 1	03/11 from 8:00 to 12:00	15/11 from 14:00 to 18:00	22/11 from 14:00 to 18:00	29/11 from 14:00 to 18:00
Series 2	09/11 from 14:00 to 18:00	16/11 from 14:00 to 18:00	23/11 from 14:00 to 18:00	30/11 from 14:00 to 18:00

Vivado



Installation guide on the UV

Getting started with exercise 1

1) Create a new project



Getting started with exercise 1

2) Choose the location of your project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:


☒ Create project subdirectory

Project will be created at: C:/Users/amelii/Documents/Teaching/ELECH409/lab1

Getting started with exercise 1

3) Select the RTL project type

Project Type
Specify the type of project to create.



☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

☐ **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

Getting started with exercise 1

4) Add the lc.vhd and lc_tb.vhd sources files

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
	1	lc.vhd	xil_defaultlib	Simulation only	C:/Users/amelii/Documents/Teaching/ELEC
	2	lc_tb.vhd	xil_defaultlib	Simulation only	C:/Users/amelii/Documents/Teaching/ELEC

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

Getting started with exercise 1

5) Select the Basys3 board

Default Part
Choose a default Xilinx part or board for your project.

Parts **Boards**

[Reset All Filters](#)

Vendor: All Name: All Board Rev: Latest

Search: Q- basys (1 match)

Display Name	Preview	Vendor	File Version	Part
Basys3		digilentinc.com	1.2	xc7a35tcpg236-1

Getting started with exercise 1

6) Create your project



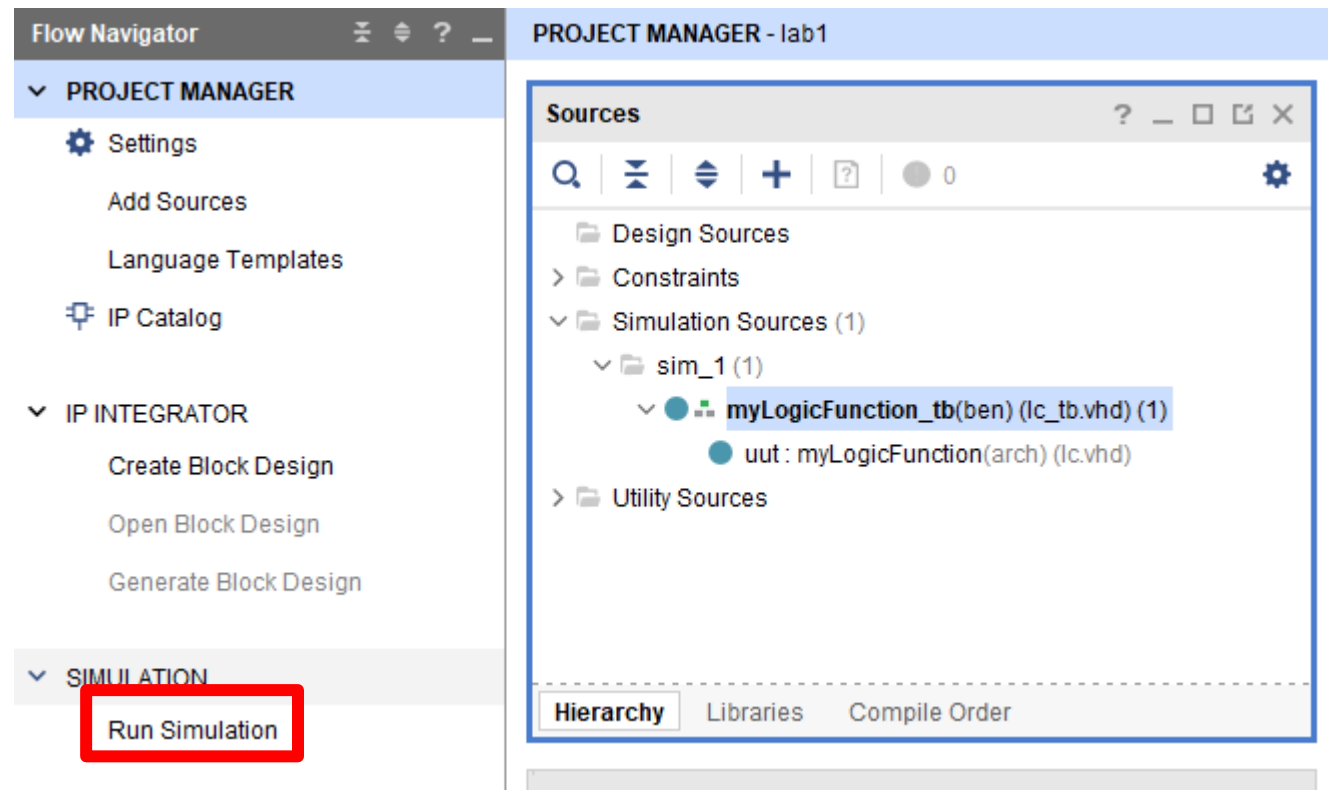
New Project Summary

- i** A new RTL project named 'lab1' will be created.
- i** 2 source files will be added.
- w** No constraints files will be added. Use Add Sources to add them later.
- i** The default part and product family for the new project:
 - Default Board: Basys3
 - Default Part: xc7a35tcpg236-1
 - Product: Artix-7
 - Family: Artix-7
 - Package: cpg236
 - Speed Grade: -1

To create the project, click Finish

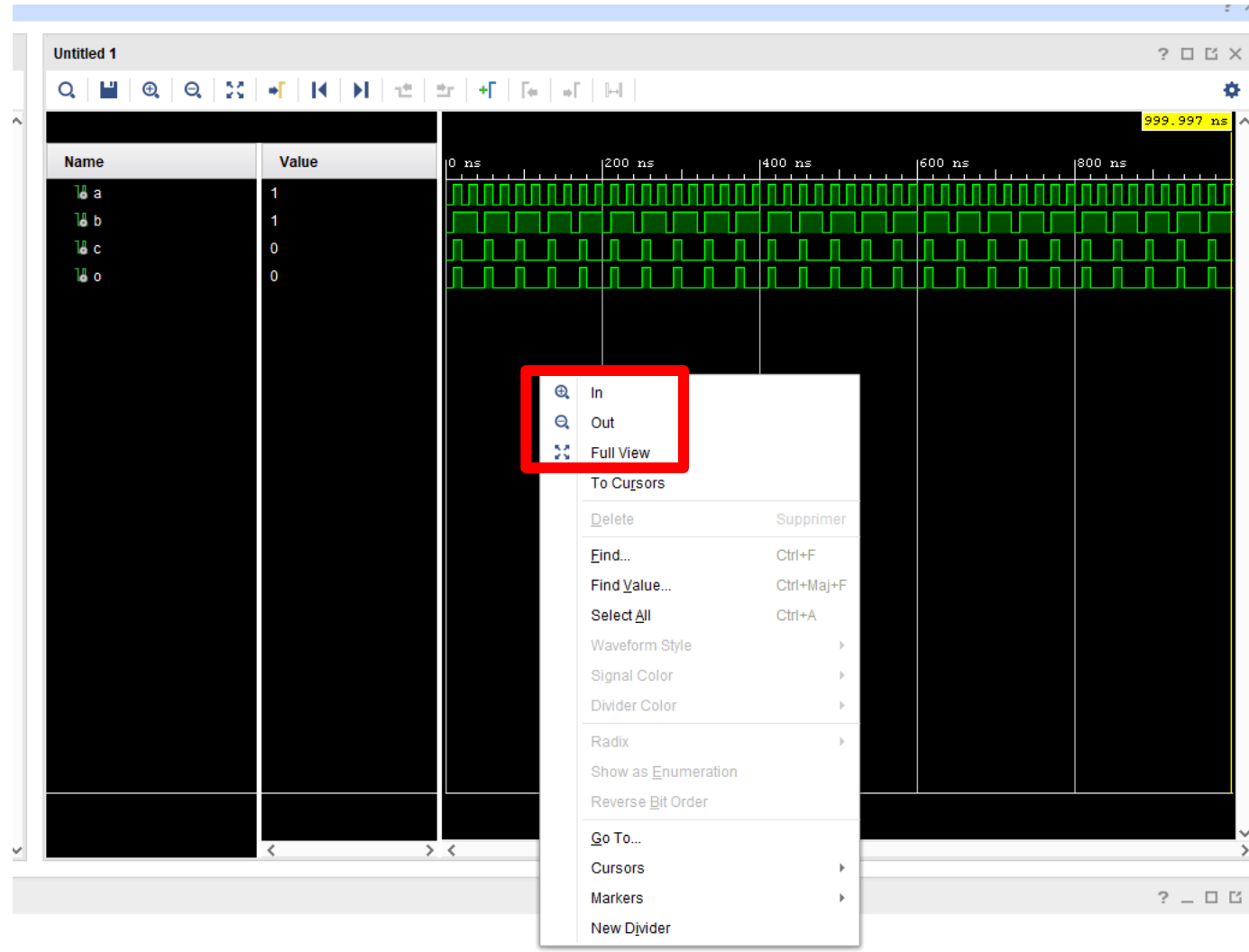
Getting started with exercise 1

7) Select *Run Simulation* then *Run Behavioural Simulation*



Getting started with exercise 1

8) Observe the waves



Do you have any questions?