Lab03 – State machines

1 Very simple Moore state machine

Using the template of the Moore state machine given in the lectures (lecture 4, slide 16 to 23), implement a simple Moore state machine with only two states: `ON` and `OFF`. Signal `switch` enables state transition from `ON` to `OFF` and from `OFF` to `ON`.

For the specifications above:

- Write the VHDL model of the state-machine above
- Write the VHDL of the test-benches
- Simulate designs and validate their operation using waveforms

Discuss the following:

- How many state bits you should expect using normal encoding?
- How many bits you should expect using one-hot encoding?

2 Moore state machine

Using the template of the Moore state machine given in the lectures, implement a two-bit up counter with synchronous enable `EN` & reset `RST`. When `EN` is set to 1, on every rising edge the counter counts up. Once the maximum number is reached, the next rising edge will put the counter to 0. Reset puts the counter in the initial state with output 0.

For the specifications above:

- Write the VHDL model of the state-machine above
- Write the VHDL of the test-benches
- Simulate designs and validate their operation using waveforms

3 More complex state machine

Using the previous state machine as a starting point, modify the model to allow up/down counter. Use signal `UP` to control the counting direction (when set to 1 the counter counts up, and down otherwise).

For the specifications above:

- Write the VHDL model of the state-machine above and draw the state diagram
- Write the VHDL of the test-benches
- Simulate designs and validate their operation using waveforms