ELECH490 - Digital architectures and design

Labs presentation

Organisation

- **Please register to a lab serie on the UV if it is not the case yet**
- Only come to the lab sessions of the serie you are registered to
- You can work individually or per group

Organisation

4 lab sessions followed by a group project

- Lab 1 - Combinatorial circuits
- Lab 2 - Conditional assignments, Registers & Counters
- Lab 3 - State machines
- Lab 4 – Introduction to the project: the Basys3 Board

You will receive one FPGA board /group of 2 students at the beginning of Lab 4

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Lab schedule

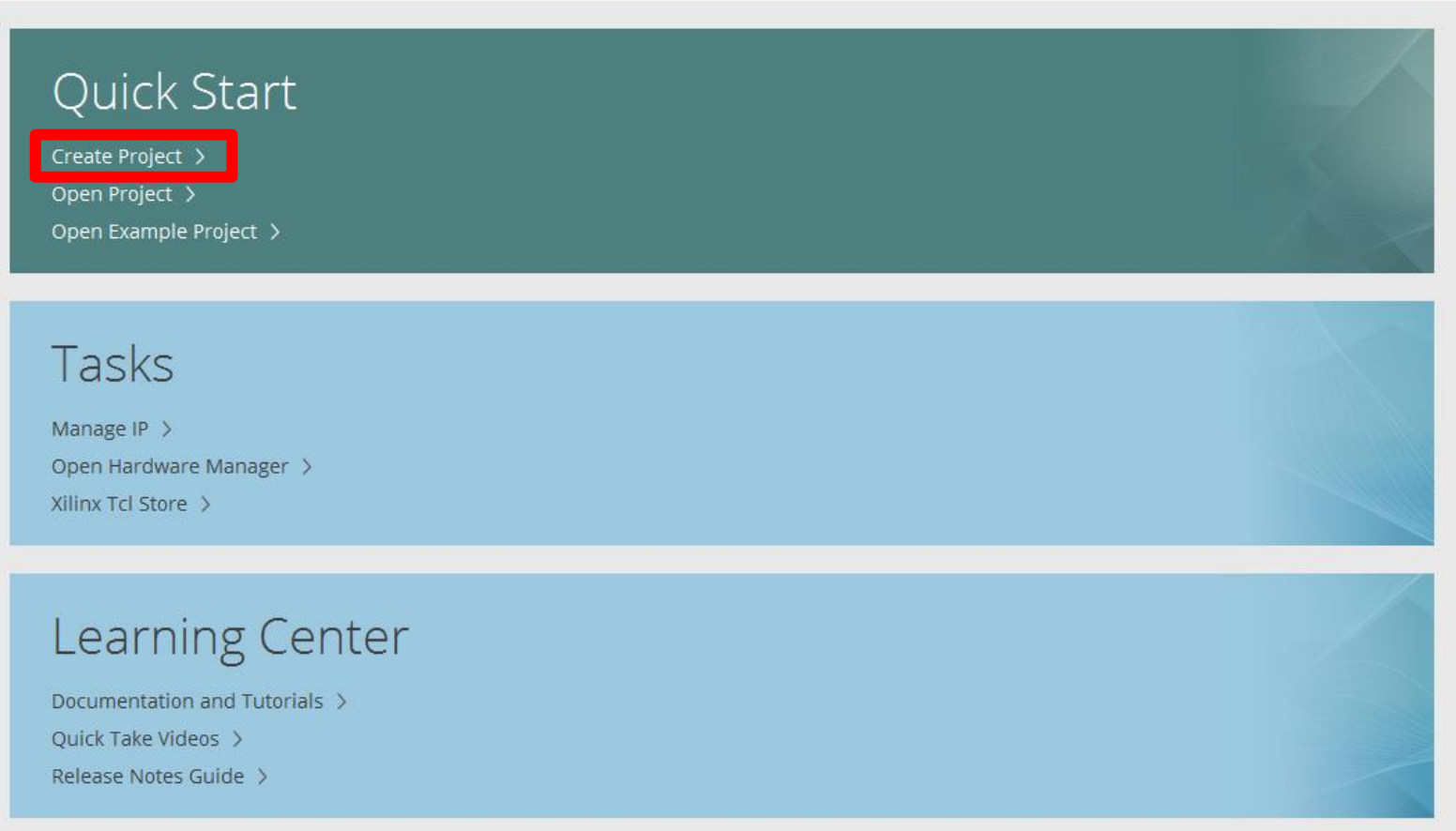
	Lab 1	**Lab 2**	**Lab 3**	**Lab 4**
Series 1	**03/11** from 8:00 to 12:00	**15/11** from 14:00 to 18:00	**22/11** from 14:00 to 18:00	**29/11** from 14:00 to 18:00
Series 2	**09/11** from 14:00 to 18:00	**16/11** from 14:00 to 18:00	**23/11** from 14:00 to 18:00	**30/11** from 14:00 to 18:00

Vivado

Installation guide on the UV

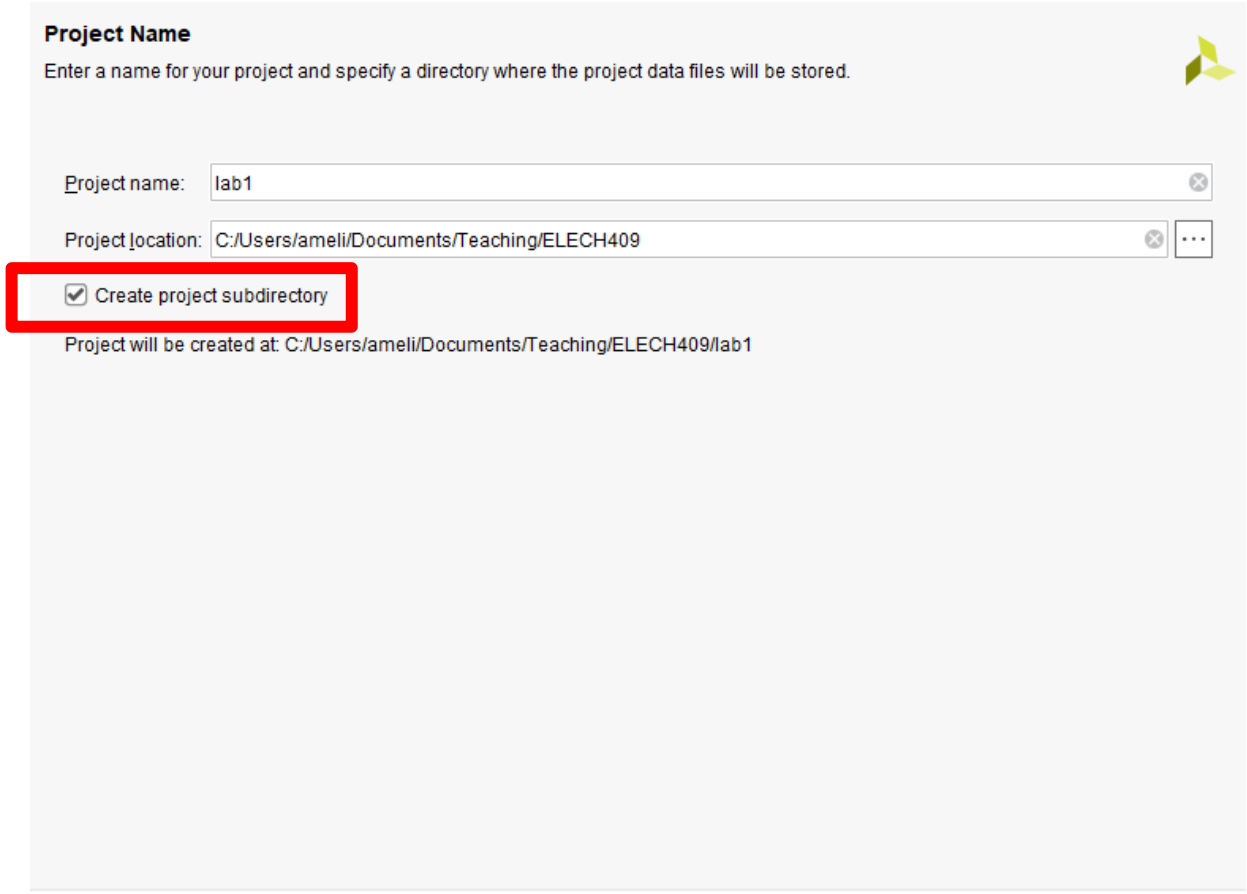
Getting started with exercise 1

1) Create a new project



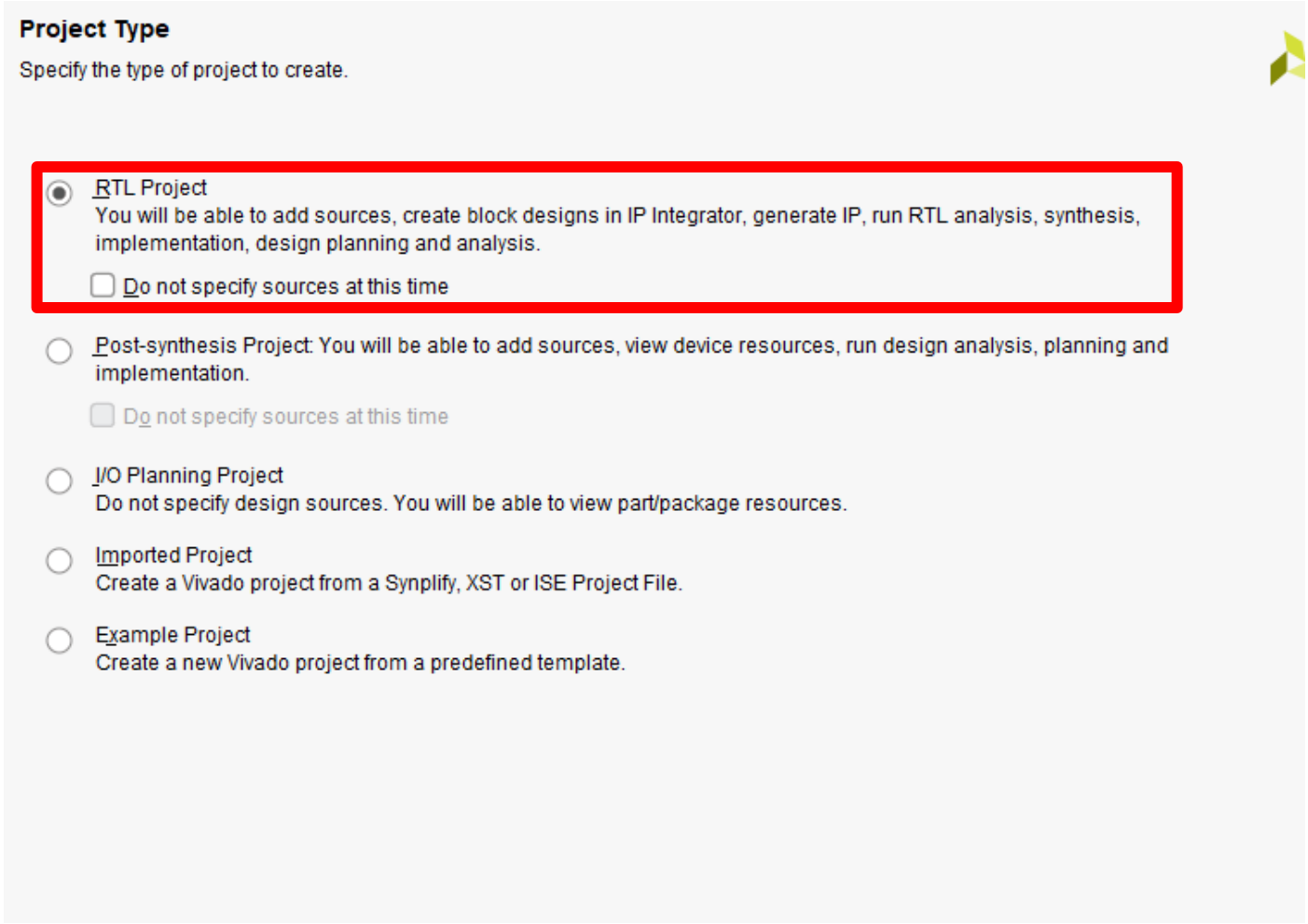
Getting started with exercise 1

2) Choose the location of your project



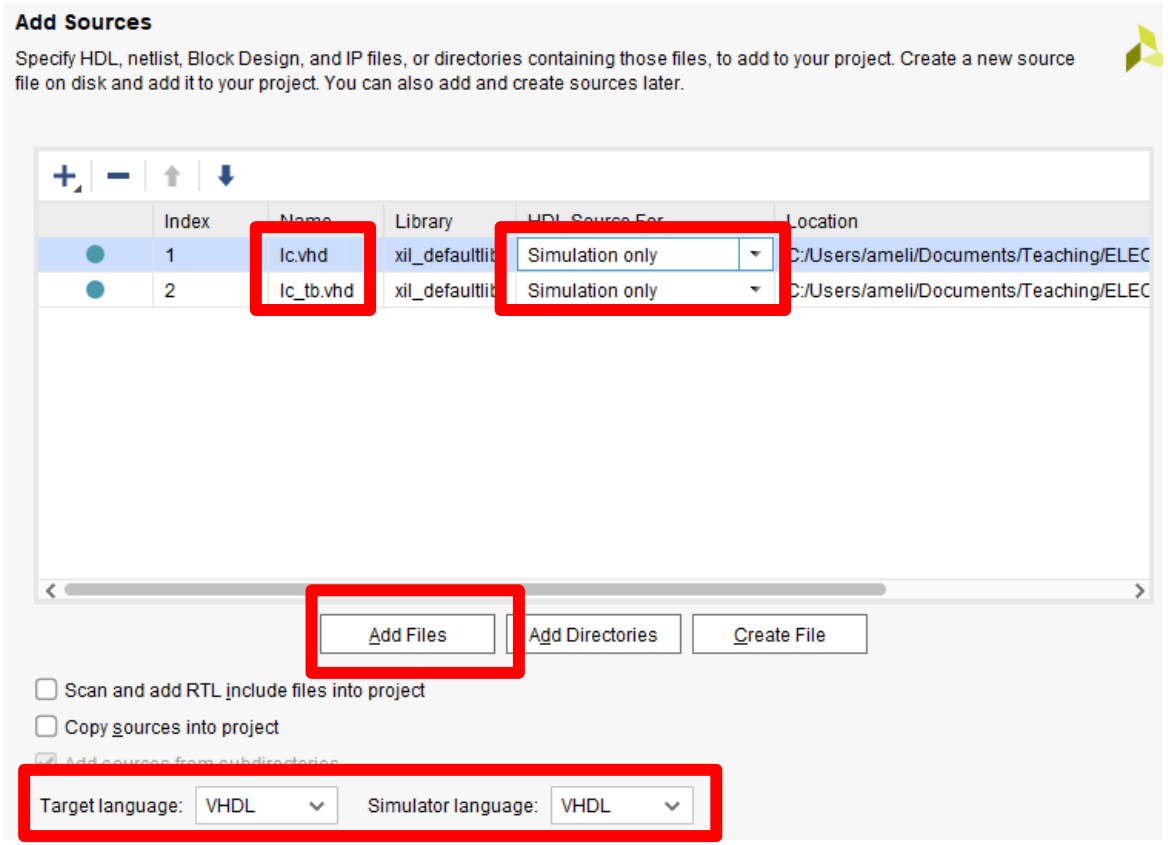
Getting started with exercise 1

3) Select the RTL project type



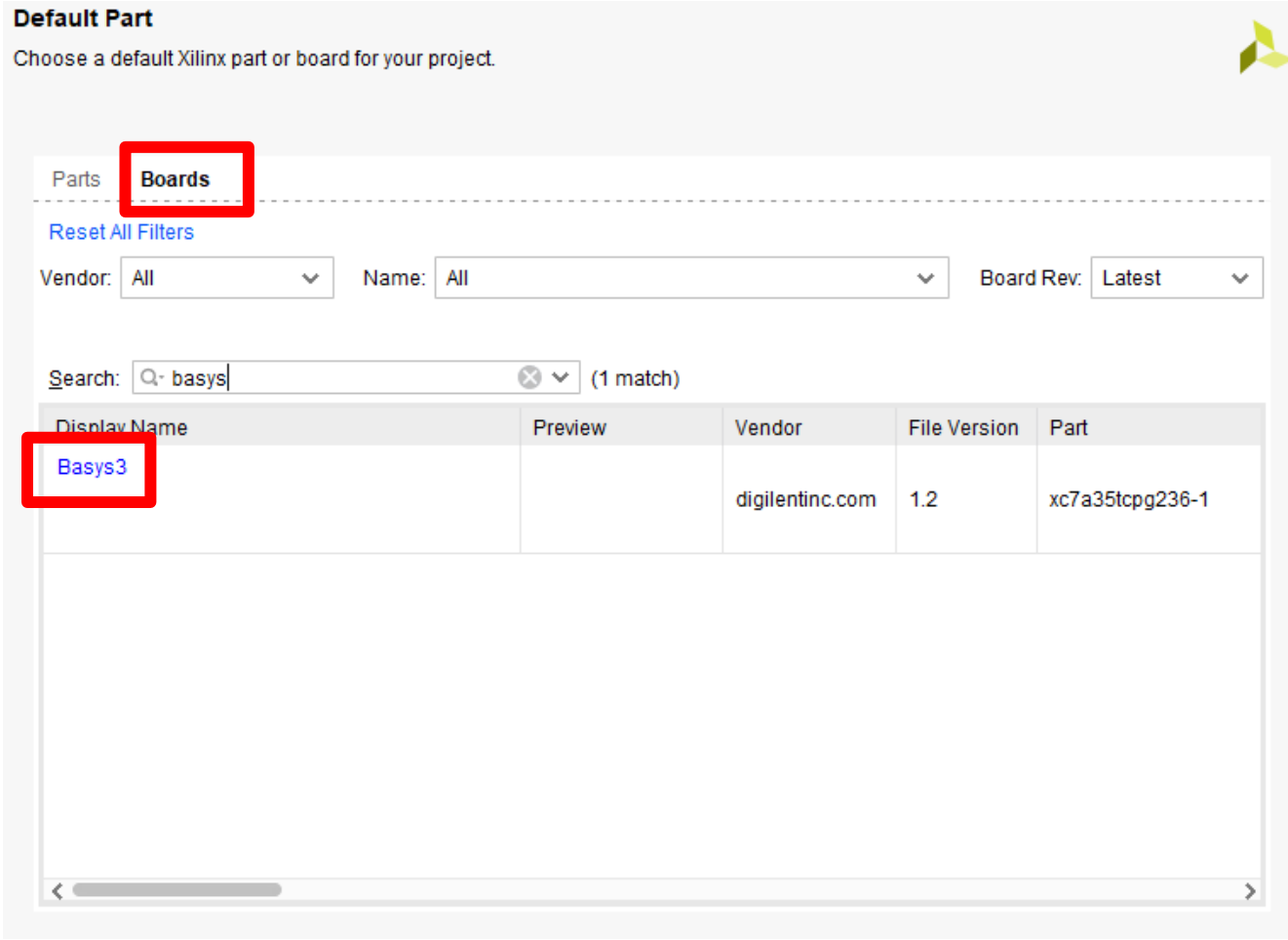
Getting started with exercise 1

4) Add the lc.vhd and lc_tb.vhd sources files



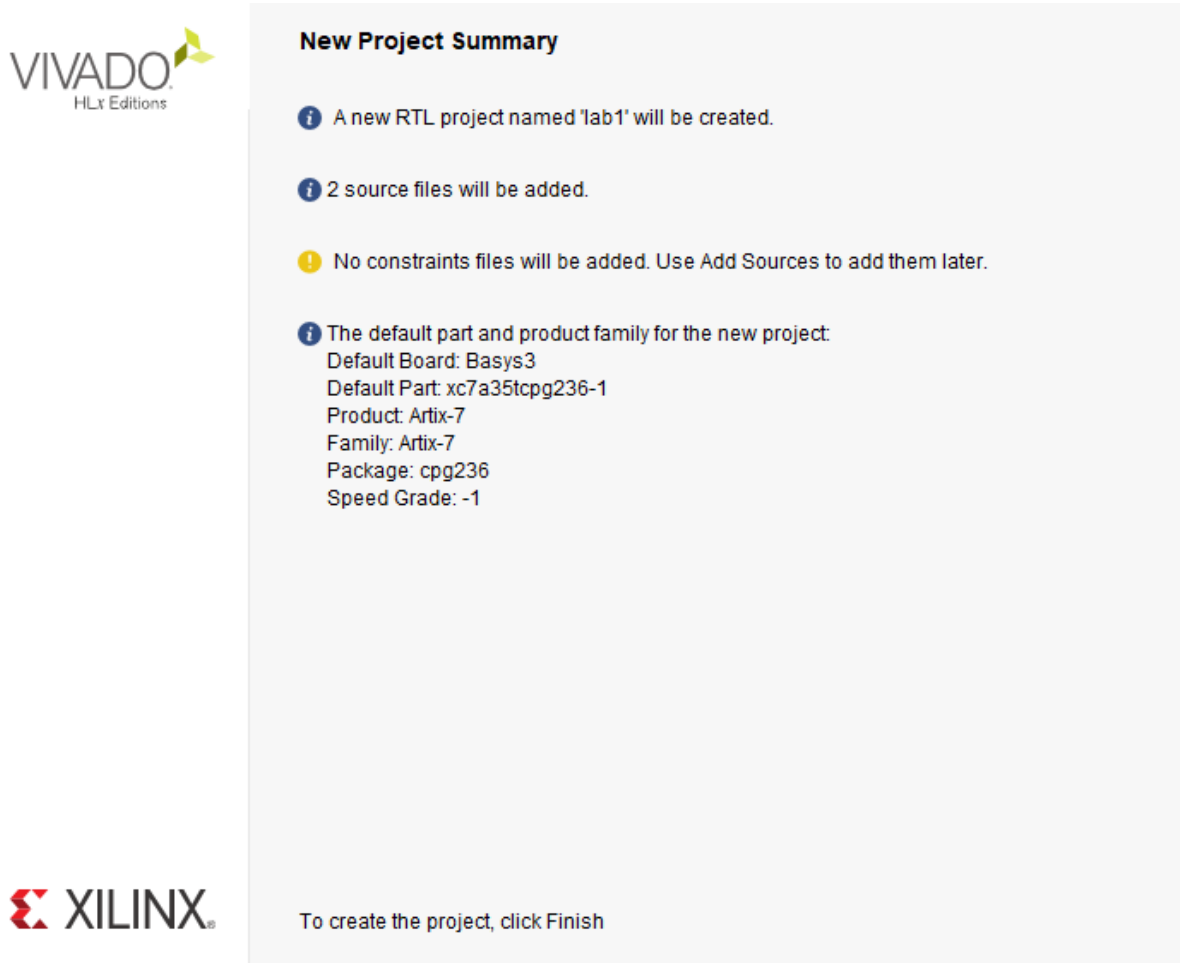
Getting started with exercise 1

5) Select the Basys3 board



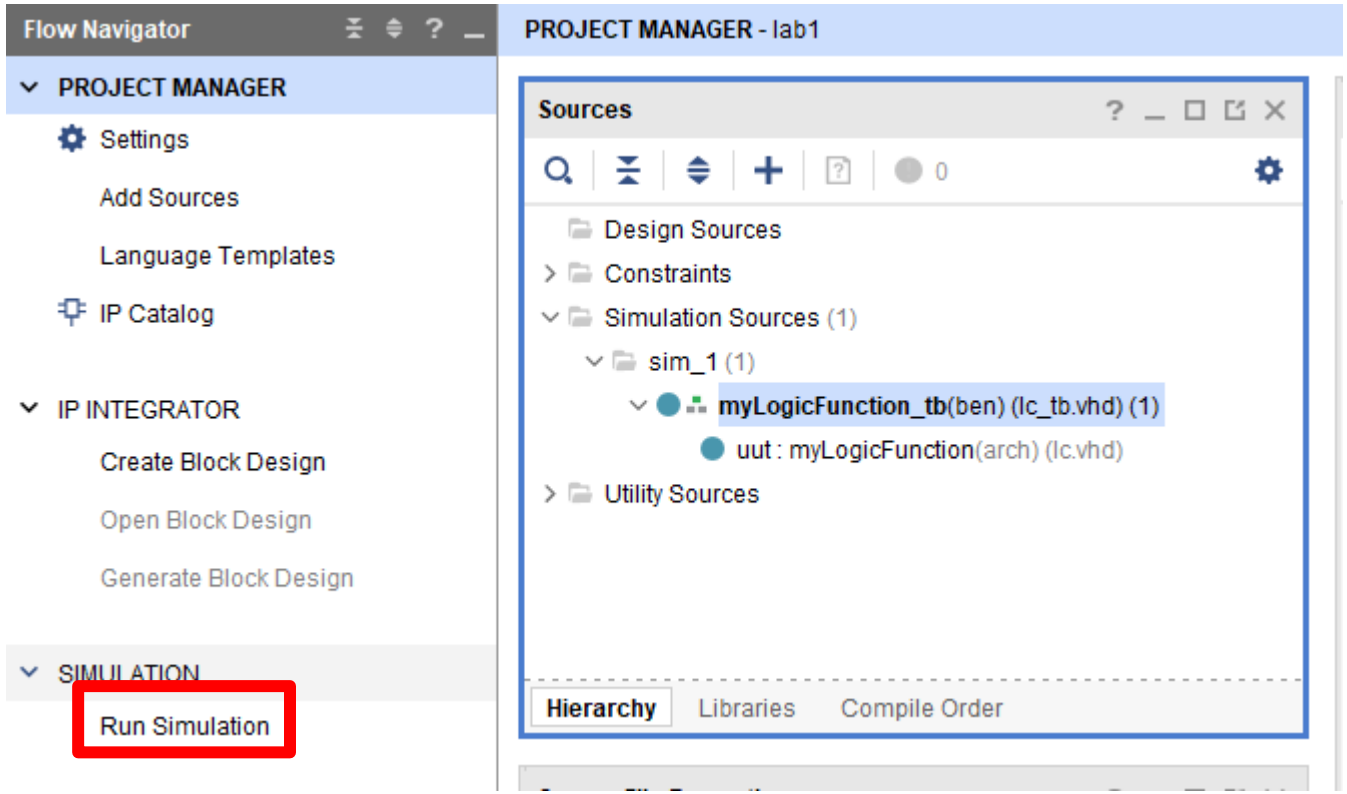
Getting started with exercise 1

6) Create your project



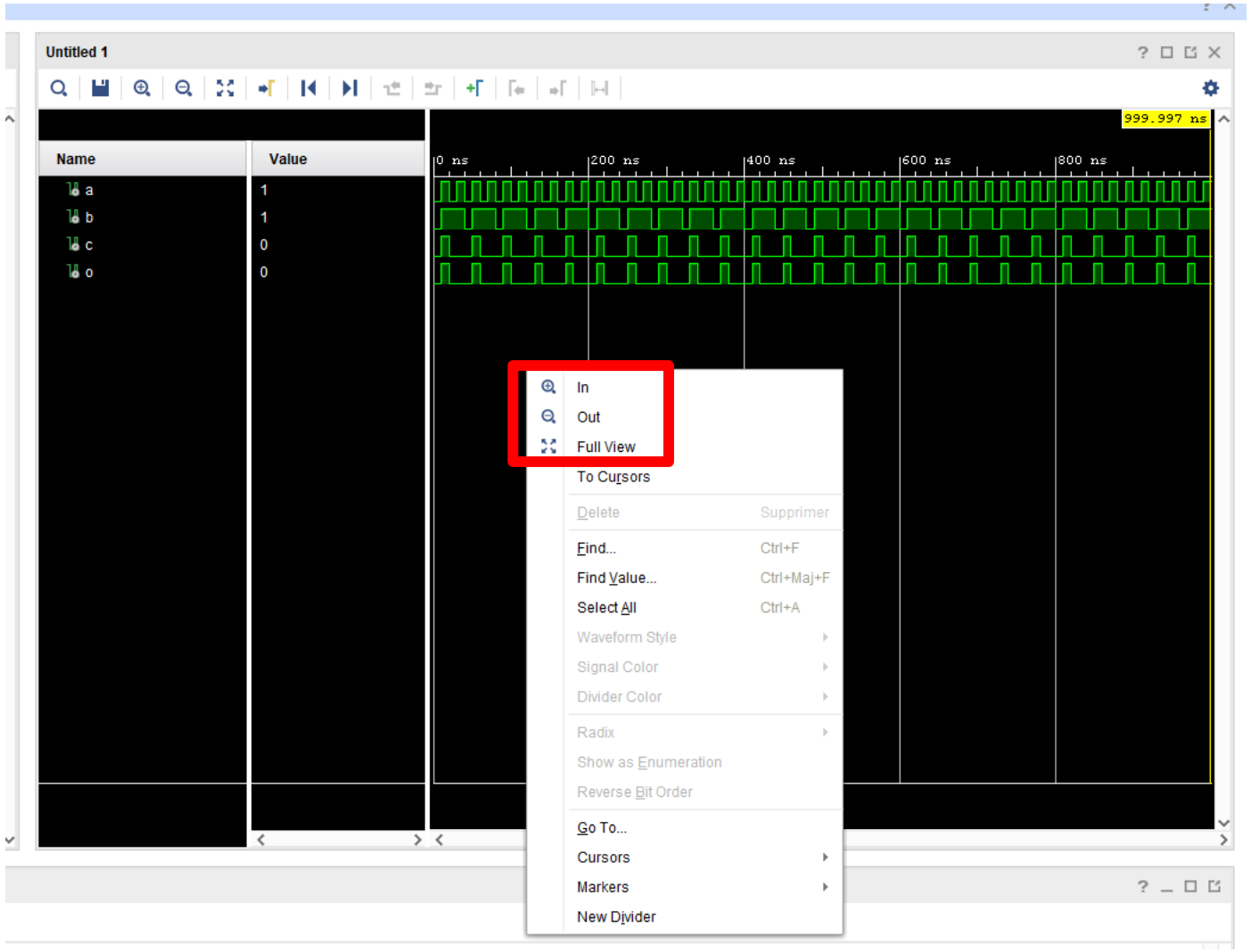
Getting started with exercise 1

7) Select *Run Simulation* then *Run Behavioural Simulation*



Getting started with exercise 1

8) Observe the waves



Do you have any questions?