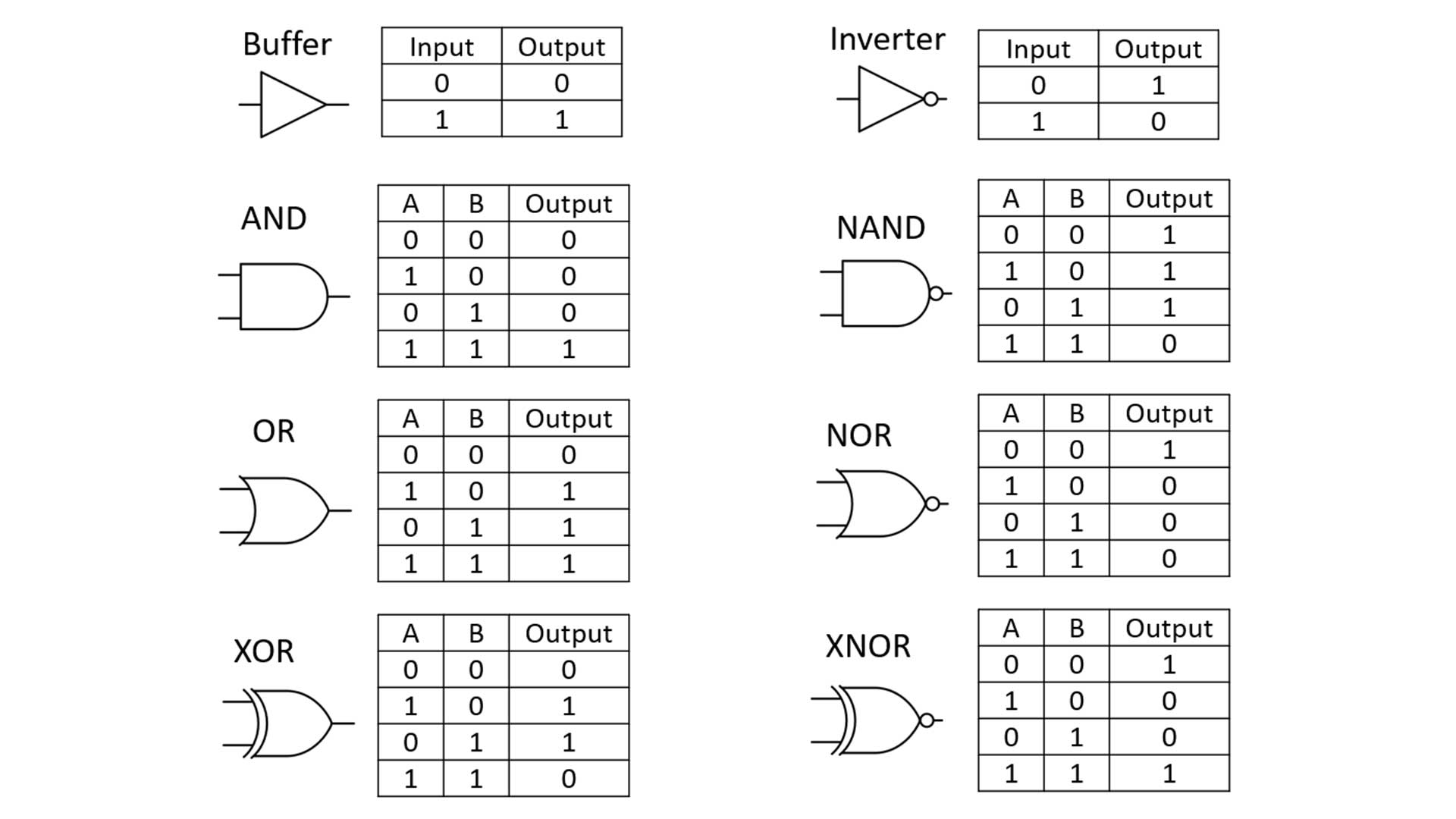


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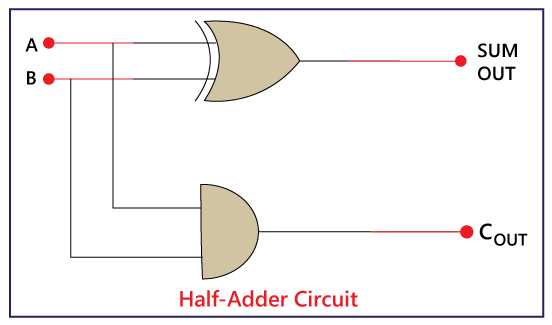
* Section1-- assignment 1 3
* Section2-- assignment 2 15

Logic gates and truth tables

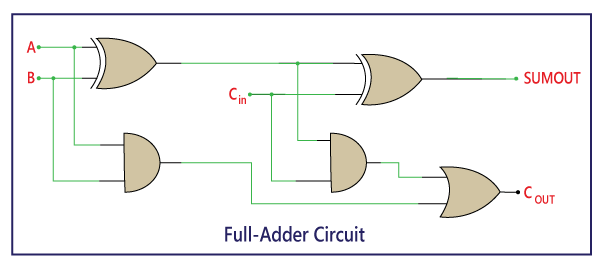
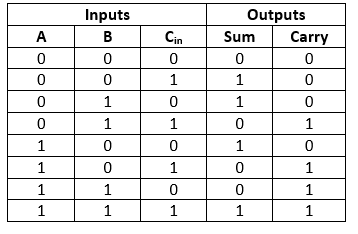


Half adder

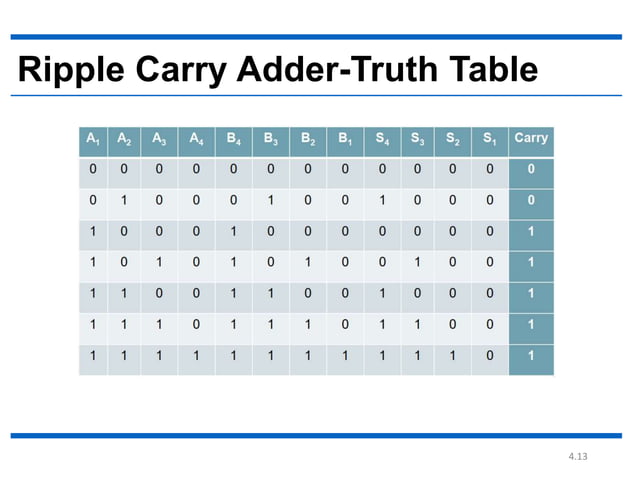
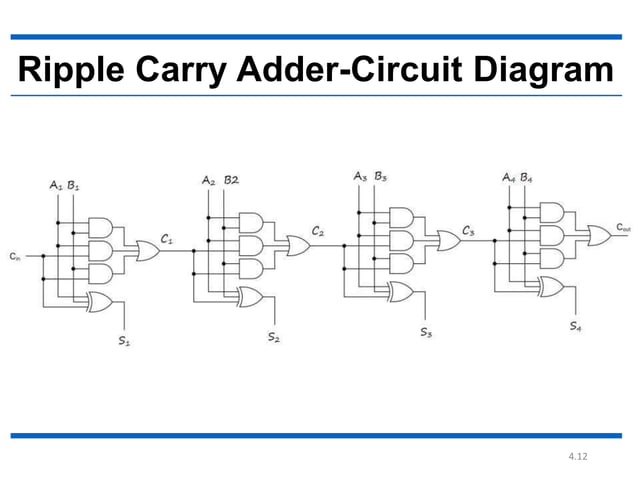
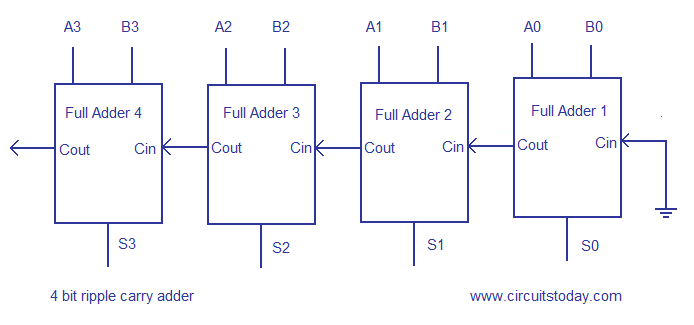
|  |  |  |  |
| --- | --- | --- | --- |
| In puts | | Outputs | |
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



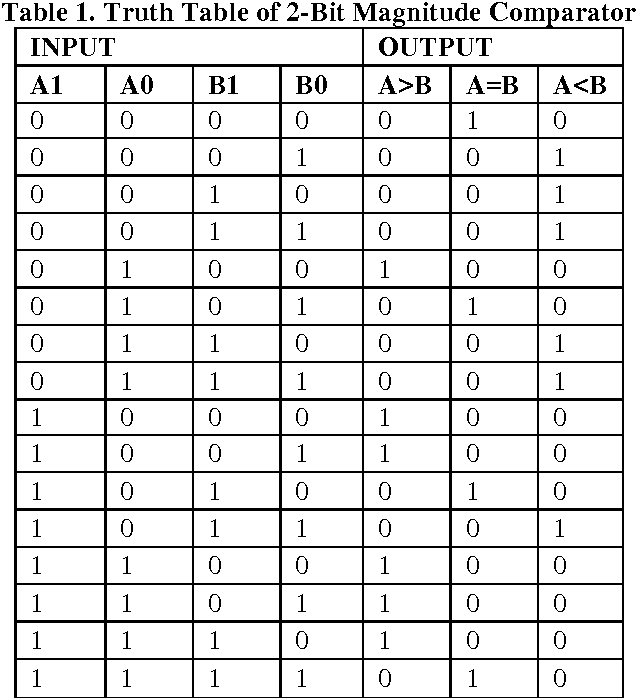
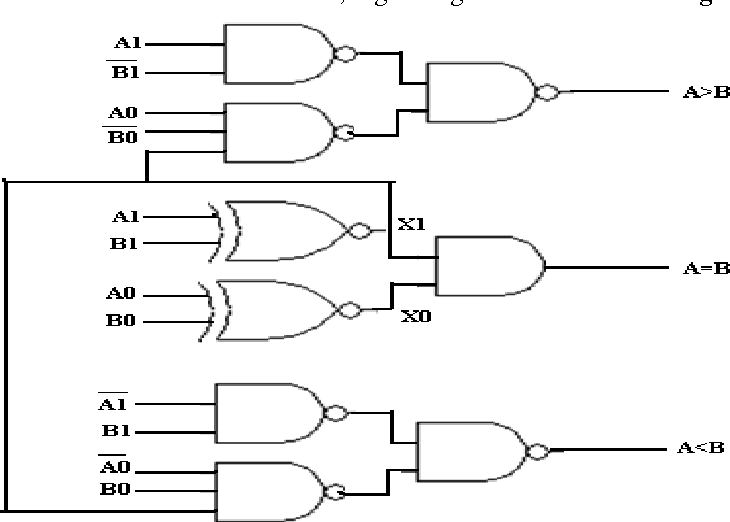
Full Adder



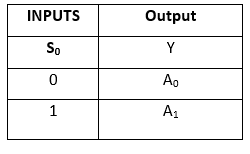
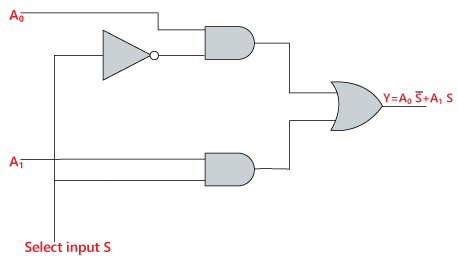
Parallel Adder



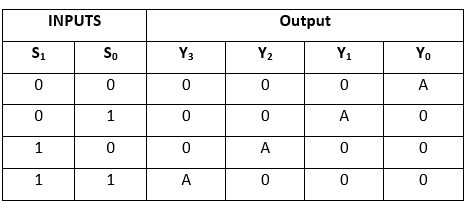
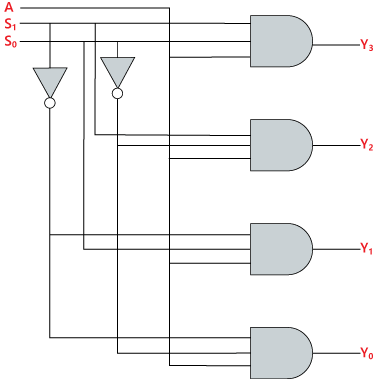
2-bit comparator



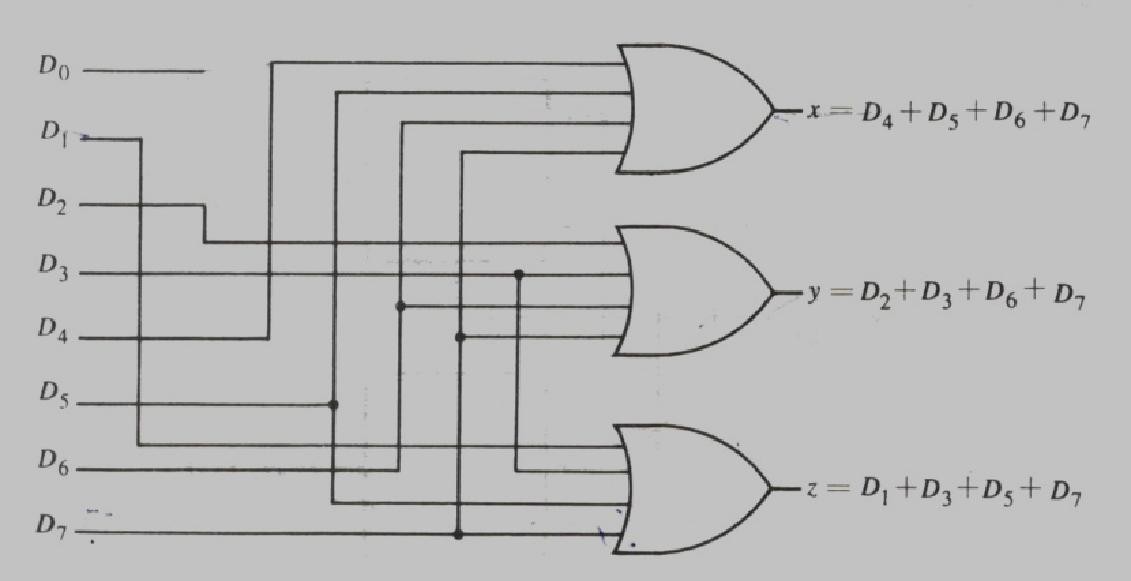
2 to 1 multiplexer



1 to 4 demultiplexer

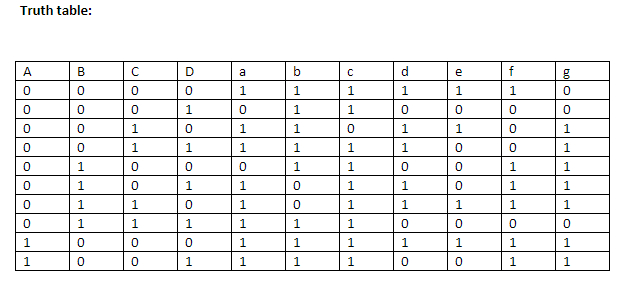
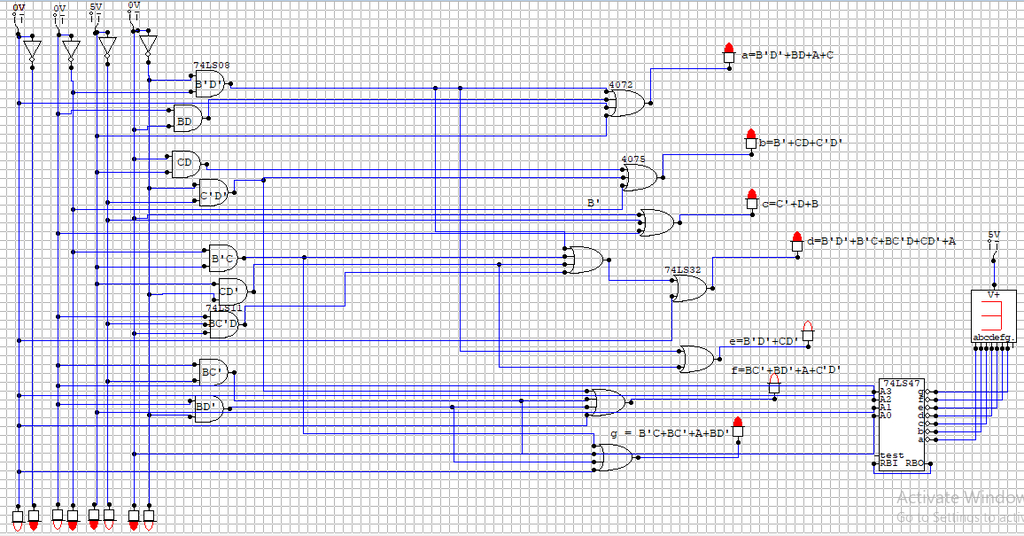


OCTAL TO BINARY ENCODER(8\*3)

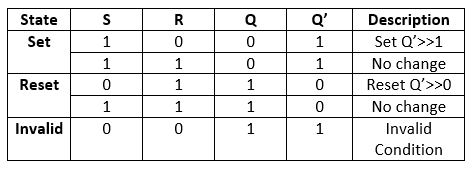
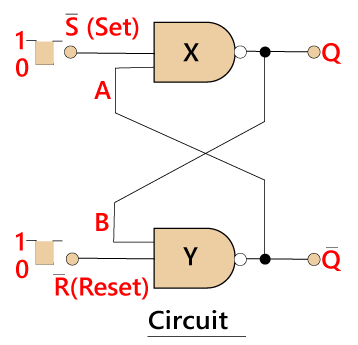


|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| inputs | | | | | | | | outputs | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A2 | A1 | A0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

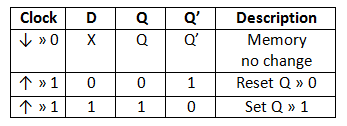
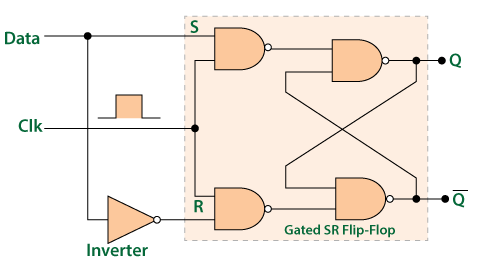
BCD to 7 Segment Decoder



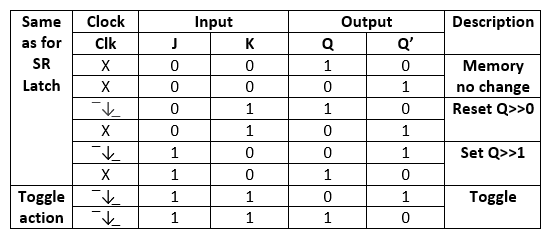
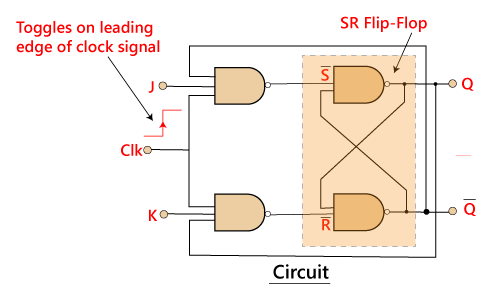
RS flip flop



D flip flop



Closed JK flip flop



**Multivibrators**: An electronic circuit that generates square waves (or other non-sinusoidal such as rectangular, saw-tooth waves).

**A fault in a digital circuit** is a physical defect that can cause incorrect outputs or a failure in the circuit. Faults can be caused by:

* Processing errors
* Material defects
* Time-dependent failures
* Packaging issues
* Manufacturing defects
* Physical damage
* Wear and tear over time

**Combinational Test Generation**

* Test Generation (TG) Methods

- (1) From truth table (2) Using Boolean equation (3) Using Boolean

difference (4) From circuit structure

* TG from Circuit Structure

- Common Concepts

- Algorithms : D-Algorithm (Roth 1967), 9-V Algorithm (Cha 1978),

PODEM (Goel 1981), FAN (Fujiwara 1983), Socrates (Schultz 1987)

**Sequential test generation** for circuits involves finding input sequences that can activate a fault and propagate its effects to the primary outputs. The process is more difficult for sequential circuits because they have state

**Built-In Self-Test (BiST)**

On-chip logic to test a design.

**Built-in self-test, or BIST**, is a structural test method that adds logic to an IC which allows the IC to periodically test its own operation. Two major types are memory BIST and logic BIST.

Memory BIST, or MBIST, generates patterns to the memory and reads them to log any defects. Memory BIST also consists of a repair and redundancy capability. In this technology, each die has spare circuits. If a circuit is bad, the defective circuit is disconnected and replaced with a good one. Memory BIST is also used to obtain known good memory stacks for 2.5D/3D devices.

Logic BIST, or LBIST, uses a Pseudo-Random Pattern Generator to generate input patterns that are applied to internal scan chains. The results are compressed into a signature. Then, a Multi-Input Signature Register determines whether the signature is correct or not to tell if all tests passed.

LBIST is most often used for safety-critical and high-reliability applications such as automotive. However, LBIST requires a very clean design with no unknown states, as this would corrupt operation. This means much more stringent design and test rules and insertion of LBIST is more complex than scan. LBIST also incurs significant overhead in timing, area, and power.

Reference:

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