

A Project Report
On

Compact DC-DC Converters For Powering FPGA Systems

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APPROVAL SHEET

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“Compact DC-DC converters for powering FPGA systems”

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Declaration

We declare that this written submission for B.E. Declaration entitled "**Compact DC-DC converters for powering FPGA systems**" represent our ideas in our own words and where others' ideas or words have been included. We have adequately cited and referenced the original sources. We also declared that we have adhere to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any ideas / data / fact / source in our submission. We understand that any violation of the above will cause for disciplinary action by institute and also evoke penal action from the sources which have thus not been properly cited or from whom paper permission have not been taken when needed.

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Abstract

Field programmable gate arrays (FPGAs) are integrated circuits with different hardware blocks and electronic systems that can be user-programmed for a specific application. The subsystems in an FPGA are under continuous or intermittent operation, that means the power requirement varies with the state of FPGA. The different systems require different low, constant voltage levels for operation. Variations in supply voltage can cause a potentially harm the FPGAs. Hence the overall assembly requires a variable low voltage and high current power supply. The power supply must be accurate, agile, controllable, smaller and efficient. Usually, sophisticated power assembly employing DC-DC converters is incorporated to meet those demands. Such modules are highly efficient but also expensive. The aim of this project deals with developing a power supply that is cost effective and also largely satisfies the requirements. The scope of the project deals with the study of supply requirements for the application and selection of a suitable method to meet the same, design of the supply, hardware assembly and testing. The proposed design is that of a DC-DC buck topology on the basis of requirements. The DC-DC converter approach involving switching regulators is adopted in the project. Simulations of the switching controllers were performed on the online simulator LTSpice. PCBs were designed on KiCad and are four layered. The selected switching regulator ICs are ADP1850, LT8652S and LTC3884. Each has it's own features, circuit and PCB design.

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Chapter 1

Introduction

1.1 Background

Power converters are essential components of modern electronic devices, because the task of a power converter is to process and control the flow of electric energy by supplying voltages and currents in a form that is optimally suited for the user loads. As such, a power converter can be used to service a wide variety of loads optimally through various configurations such as buck, boost, buck-boost etc. On such user load which makes use of a power converter is a Field Programmable Gate Array(FPGA).

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. FPGAs have varied applications throughout many industries, from video and imaging devices to automobile, from computer circuitry to military and aerospace industries, along with application in specialized processing equipment, and many other functions. An FPGA acts as a prototype for testing until the ASIC/processor design is finalised and proven to be bug-free, followed by final ASIC design manufacturing.

1.2 Motivation

An FPGA requires a varied supply of voltage and current for its operation, ranging from 0.9 to 1.8V, all the while demanding a wide berth in current requirements, with inrush current as high as 12A. Satisfying all these requirements is a demanding task for a power controller, and as such, the design tends to become complex and consequently, expensive. Solutions available for the same in the form of micro-modules are effective, but un-

economical for distribution in countries like India due to their high retail cost. If a similar, or better, solution can be developed locally, then the effective cost of powering an FPGA can be reduced significantly. This, however, is contingent on the fact that the solution developed locally can function just as effective as contemporary solutions available in the industry. So, to alleviate the cost of research and development involved in the design of such a solution, we can use low-cost underdeveloped solutions currently available in the industry to implement the powering requirements of an FPGA

1.3 Aim and Objective

We aim to design a DC-DC converter that can provide necessary voltages for different FPGA rails with limited disturbances along with continuous and transient current requirements while accounting for compactness and cost-effectiveness of design.

1.4 Report Outline

This project report contains the study the requirements of the system and solutions to meet the same, which is followed by a comparative study of various switching regulators at par with industry standards suitable for our application. We selected three different switching regulators to serve as three different approaches to powering an FPGA, and as such, the design of the system covers the design of the three different approaches. The simulations for all of the designs as well as their PCB designs for lab testing are presented. The final soldered PCBs for all the designs as well as lab testing of ADP1850 is included.

Chapter 2

Study Of the System

A voltage source is a two-terminal device which can maintain a fixed voltage. An ideal voltage source can maintain the fixed voltage independent of the load resistance or the output current. We use regulators to maintain the voltage of a power source within acceptable limits.

2.1 Regulators

2.1.1 Linear regulators

Linear regulators are simple voltage regulator circuits commonly used in electronics. Linear regulators uses a closed feedback loop to bias a pass element to maintain a constant voltage across its output terminals as shown in the Fig 2.1 [1]. The transistor is operated in the active region of its voltage-current characteristics.

Heavier load decreases the output and increases the error voltage. A higher error drives higher base current for the transistor. Consequently, a higher collector current is delivered and pulls up the output voltage. When the load decreases, all signal movements get reversed. By doing so, the output is regulated.

Advantages of linear regulators :

1. They are simple and cheap.
2. They respond quickly to the changes in load voltage.

Disadvantages of linear regulators :

1. They are less efficient as compared to switching regulators.
2. The heat dissipation is high.
3. They have poor response to load transients.

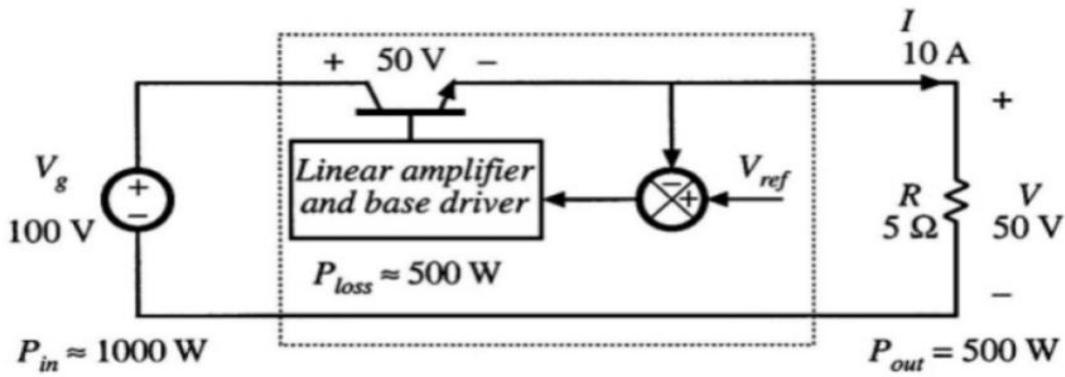


Figure 2.1: Linear Regulator [1]

2.1.2 Switching regulators

Switching regulators rapidly switch a series element on and off. They can operate with both synchronous and non-synchronous switches (FETs). These devices store the input energy temporarily and then release that energy to the output at a different voltage level. The switch's duty cycle sets the amount of charge transferred to the load.

2.2 DC to DC Converters

Depending upon the suitability of the application we have chosen DC to DC converters. Since the output voltage range is very low as compared to the input voltage levels , the duty cycle will be very low and hence if we use linear regulators their efficiency would be low. This would result in high energy dissipation.

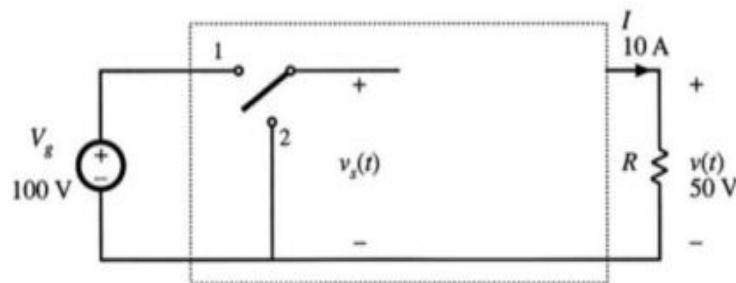


Figure 2.2: Switching Regulator

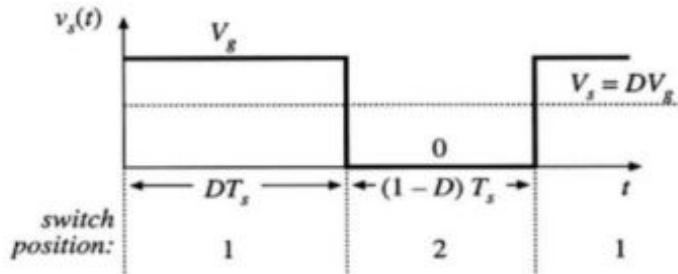


Figure 2.3: Switching Regulator Graph [1]

These are efficient because the series element is either fully conducting or switched off so it dissipates almost no power. Switching regulators are able to generate output voltages that are higher than the input voltage or of opposite polarity, unlike linear regulators.

Table 2.1: Comparision of DC-DC converters

Features	Buck	Boost	Buck-Boost	Flyback
Input Current	Pulsed	Continuous	Pulsed	Pulsed
Output Current	Continuous	Pulsed	Pulsed	Pulsed
Output voltage magnitude as compared to input voltage	Lesser	Higher	Lesser or Higher	Lesser or Higher
Output Voltage Polarity	Same	Same	Reversed	Same
Approximate steady State duty cycle (Assuming 5V Input and 3.3V Output)	0.66	Not Possible	0.39759	0.79518 (assuming turns ratio of 2)

Buck converter steps down the applied DC voltage, boost steps it up, while buck-boost can work in both configurations. Isolated DC-DC converters have an isolation element in the form of a transformer between the input and output. It can also be seen that duty cycle of buck is the highest, which ensures more efficiency. Flyback has a high duty cycle as well but the presence of transformer makes the design bulky.

Chapter 3

Proposed System

3.1 Problem Statement

To design a DC-DC converter that can provide necessary voltages for different FPGA rails with limited disturbances along with continuous and transient current requirements while accounting for compactness and cost-effectiveness of design.

3.2 Scope

Scope of this project includes but is not limited to selection of suitable DC-DC converter topology, searching for means to implement the same, circuit design via simulations, PCB design to create multiple prototypes. The prototypes will be tested and the most suitable ones will be considered for further optimisation.

3.3 Proposed System

FPGA requires discrete voltage levels to power various rails such as- VCCINT (Internal supply voltage)- 0.9 or 1V, VCCAUX (Auxillary supply voltage)- 1.8V, VCCO (Output drivers supply voltage)- 3.3V, MGTAVCC (Analog supply voltage for the GTP transmitter and receiver circuits)- 0.9 or 1V, MGTVCCTAUX (Auxillary analog supply voltage for the GTP transmitter and receiver circuits)- 1.8V, MGTAVTT (Analog supply voltage for the GTP transmitter termination circuit)- 1.2V

FPGA consumes a few amperes of continuous current (2-5) while performing an operation and around 500mA whilst idling. The transition between these two stages can introduce momentary voltage peaks or dips at the output of the power supply. The maximum change in the output voltage

must be limited to $\pm 3\%$ of the voltage specified for that rail. [2]

3.3.1 Switching Regulators ICs

The requirements of voltage levels quite below the lab supply voltage levels prompted the selection of buck topology. We chose switching regulators which operate on the principle of buck converter to serve our purpose. They have an internal oscillator with adjustable frequency which exists to provide switching pulses to the buck converter switches. The switches may or may not be integrated into the IC itself. They provide constant output voltage which can be set by the designer. We have to decide on the values of output inductor and capacitor. They also offer feature of soft start to reduce the inrush current during start-up for the converter. They have their own compensation system in the closed loop system, but we can design and connect our own compensation network according to our requirements and provision is made for the same.

Switching regulators ICs are very efficient in their intended operation, typical efficiencies are in the range of 90% to 95% for optimum loading condition. For light load conditions, they lie around 60% to 75%. The ICs have a very low form factor which contributes towards the compactness of design. They can operate on high frequencies (selectable) which can further contribute to reducing the size of passive components.

3.3.2 Comparison of Switching Regulator ICs

Controller ICs	Requires External Switch	Input Voltage (V)	Output Voltage (V)	Frequency (Hz)	Soft Start	Tunable	Cost (INR)
ADP1850 [3]	Yes	1 to 20	0.6-0.9Vin	200K-1.5M	Yes	Yes	340
TPS40303 [4]	Yes	3 to 20	0.6-18	300K	Yes	Yes	130
TPS53219 [5]	Yes	4.5 to 28	0.6-5.5	300K-970K	Yes	No	180
TPS53315 [6]	No	3 to 15	0.6-5.5	250K-1M	Yes	No	180
MAX15046 [7]	Yes	4.5 to 40	0.6-0.85Vin	100K-1M	Yes	Yes	120
LTC3884 [8]	Yes	4.5 to 38	0.5-3.5/5.5	250K-1M	Yes	Yes	1200
LT8652S [9]	No	3.6 to 18	0.6-0.9Vin	300k-3M	Yes	Yes	850

Table 3.1: Comparison of Switching Regulators

After studying the features and availability of simulation software, three controllers, ADP1850, LT8652S, LTC3884 were selected for further design.

LTC3884 comes with a built-in PMBus/I2C interface which allows for serial communication with a microcontroller. There are commands to change output voltage, soft start time etc. ADP1850 has a tunable control system but requires external switches. LT8652S has built-in switches and can operate at very high frequencies thereby significantly reducing the size of passive components. Description and design for these ICs is covered in upcoming chapters. Appropriate simulation software was also a deciding factor in the selection process.

Chapter 4

Design Of the System

4.1 Buck Converter Design

As can be seen in Fig. 4.1, the buck converter is composed of many individual components. The design of buck converter requires design of all these individual components which make up the converter itself like inductor, capacitors, control circuit etc. [10]

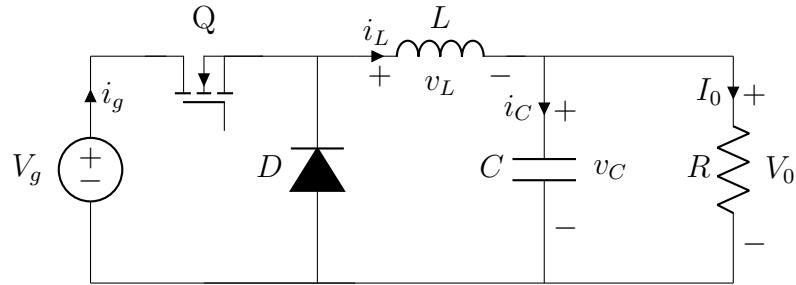


Figure 4.1: Buck Converter

The selection of each of these components is decided by considering certain parameters and also includes factoring in the tolerance and de-rating while in operation.

4.1.1 Necessary Parameters of the Power Stage

The following four parameters are needed to calculate the power stage:

1. Input voltage range: $V_{IN(min)}$ and $V_{IN(max)}$
2. Nominal output voltage: V_{OUT}
3. Maximum output current: $I_{OUT(max)}$
4. Integrated circuit used to build the buck converter. This is necessary because some parameters for the calculations must be derived from the data sheet.

4.1.2 Switching Frequency

Switching frequency is an important aspect of converter design. Since Integrated circuits were chosen to perform the control operation, the switching frequency was decided on the basis of minimum ON time of the switch. The equation for selecting switching frequency is given in 4.1

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (4.1)$$

4.1.3 Inductor Design

The filter inductor value and its peak current are determined based on the specified maximum inductor current ripple. For the purposes of this project it was decided that maximum ripple current be limited to 0.5A (ΔI_L). For each voltage output, values for inductor and switching frequency were calculated separately. With the help of 4.2, the required inductor value can be calculated.

$$L = \frac{(1 - \frac{V_{OUT}}{V_{IN}}) \times V_{OUT}}{F_{SW} \times \Delta I_L} \quad (4.2)$$

4.1.4 Capacitor

Capacitors are of 2 types :-

1. Bulk Capacitor

These are usually electrolytic capacitor. These type of capacitor are used to minimize the output voltage ripple and to minimize the voltage change during load current transient. 4.3 is used to calculate capacitor value required.

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_{OUT} \times F_{SW}} \quad (4.3)$$

2. Decoupling Capacitor

Ceramic capacitor of low values are used to decouple input and output parts of the circuit and to bypass any noise. Decoupling capacitor is placed as close as possible to the device requiring the decoupled signal. This minimizes the amount of line inductance and series resistance between the decoupling capacitor and the device.

4.2 Calculated values for components of each switching regulator

Using Equation 4.1, Equation 4.2 and Equation 4.3 ([3],[8] and [9]), the values of components required to limit the Output ripple current (ΔI_L) to 0.5A and to limit output ripple voltage to 2mV were calculated.

4.2.1 ADP1850

The ADP1850 is a configurable dual output or two-phase, single output dc-to-dc synchronous buck controller capable of running from commonly used 3.3 V to 12 V (up to 20 V) voltage inputs. It is a synchronous buck converter controller which requires external switches.

The T_{ON} time for this switching controller as given in the data sheet is 135nS [3].

Component /Parameter	1V	1.2V	1.8V	3.3V
Frequency	600kHz	740kHz	1MHz	2MHz
Inductor	$4 \mu H$	$3 \mu H$	$3 \mu H$	$5 \mu H$
Output Capacitor	$20\mu F$	$17\mu F$	$12.5\mu F$	$6.25\mu F$

Table 4.1: Calculated values for ADP1850

To keep the design uniform, a single value of inductor was chosen. The highest calculated value is $5 \mu H$, so including tolerance and de-rating, the inductor value chosen is $6.8 \mu H$ and to ensure voltage remains within 3% of the specified voltage, $100\mu F$ electrolytic output capacitor were chosen.

4.2.2 LT8652S

The LT8652S is a dual step-down regulator that delivers up to 8.5A of continuous current from both channels and supports loads up to 12A from each channel. It is a monolithic device i.e. it has Power switches integrated in IC package, thus not requiring any external switches.

The T_{ON} time for this switching controller as given in the data sheet is 20nS [9].

As in the case of ADP1850, uniformity in design was considered. The highest calculated value is $1.8 \mu H$, so including tolerance and de-rating, the

Component /Parameter	1V	1.2V	1.8V	3.3V
Frequency	3MHz	3MHz	3MHz	3MHz
Inductor	$1 \mu H$	$1.12 \mu H$	$1.08 \mu H$	$1.8 \mu H$
Output Capacitor	$10.4\mu F$	$10.4\mu F$	$10.4\mu F$	$10.4\mu F$

Table 4.2: Calculated values for LT8652S

inductor value chosen is $3.3 \mu H$ and similarly the capacitor value selected was $100\mu F$

4.2.3 LTC3884

The LTC3884 is dual output PolyPhase DC/DC synchronous step-down switching regulator controllers with an I^2C -based PMBus compliant serial interface. Switching frequency, channel phasing, output voltage, and device address can be programmed both by the digital interface as well as external configuration resistors. Additionally, parameters can be set via the digital interface or stored in EEPROM.

The Minimum on time for this controller is 60nS [8].

Component /Parameter	1V	1.2V	1.8V	3.3V
Frequency	1.38MHz	1.67MHz	2.5MHz	4.5MHz
Inductor	$1.83 \mu H$	$2.16 \mu H$	$3.06 \mu H$	$4.785 \mu H$
Output Capacitor	$31.25\mu F$	$31.25\mu F$	$31.25\mu F$	$31.25\mu F$

Table 4.3: Calculated values for LTC3884

The Inductor value chosen for this controller is $6.8\mu H$ again as the maximum inductance calculated was $4.785\mu H$. To mitigate the voltage change during transients, $100\mu F$ electrolytic output capacitors were selected again.

4.3 PCB Design

PCB of the individual selected Switching Regulator was designed using KiCad. KiCad is a free open source software suite for electronic design

automation(EDA) to design electronic systems such as Integrated Circuits(IC) and Printed Circuit Boards(PCB). Since the proposed system demands to power 6 different Voltage FPGA Rails 3 PCB per dual output switching regulator have to be produced. so, a total of 9 PCBs were to be designed and produced.

All the components used for the PCB were of Surface Mount Technology (SMT) except for Through Hole Input, Output Connectors and Pin headers.0603 Package was used for all the resistors and capacitors which were required for operation of switching regulators. This was done to make all the 3 designs of the voltage regulators uniform and they are compact but adequately big enough to perform manual soldering. Even the decoupling capacitors were of 0603 package and was placed accordingly with output decoupling capacitor placed near to output terminals and input decoupling capacitors near to switch. The power handling components of the converter were of different packages namely SOT23 for the switches and radial can for the output and input bulk capacitors.

A 4 layer PCB Stackup was used for all the switching controller where the top and bottom layer being the signal plane and 2nd layer being ground plane used for small signal grounding (AGND) for the Electronic Circuit and Power Grounding (PGND) for the Power Circuit. Minimization of copper area of the switch node was strictly ensured as suggested by PCB layout guidelines of all the voltage regulators as it is the noisiest part of the entire circuit. Multiple Vias were placed to connect the front copper ground polygon and the 2nd and 3rd layer. It was also ensured that the vias placed were not obstructing the flow of current. A current sensing resistor was used in between positive terminal of output capacitor and negative terminal of inductor so that both the terminals of resistor can be traced to a test point and can be used to analyze the inductor current . Test points of different pins of the regulator are also provided to verify that the newly assembled device is working properly or used aftermarket for necessary repairs to the device. 3 Dummy Resistors of resistance 0 ohms are also used to connect the AGND plane to PGND plane in 2nd Layer (Ground Plane). Mounting Holes at four corners of PCB is also provided for mechanical support. Hex Spacer will be used in case mounting is required.

4.3.1 ADP1850 PCB Design

ADP1850 is manufactured in a 32-lead 5 mm × 5 mm LFCSP package with an exposed pad placed below the package for thermal dissipation PCB Layout Guidelines specified in ADP1850 datasheet and ADP1850

Evaluation Kit UG205 were followed while designing the PCB of ADP1850 PCB Stackup used for this PCB was 4 copper layer PCB with the top and bottom layer being signal plane and 2nd layer is ground plane used for both AGND and PGND. 3rd layer being a combination of Power plane and ground plane specifically Power Ground Plane (PGND). A 2X10 Pin Header was used where 5 pins (PGOOD1, COMP1, FB1, TRK1, EN1) of each channel and corresponding ground pins (signal ground) were provided to enable the controller (EN1, EN2) or to check the status of the controller.

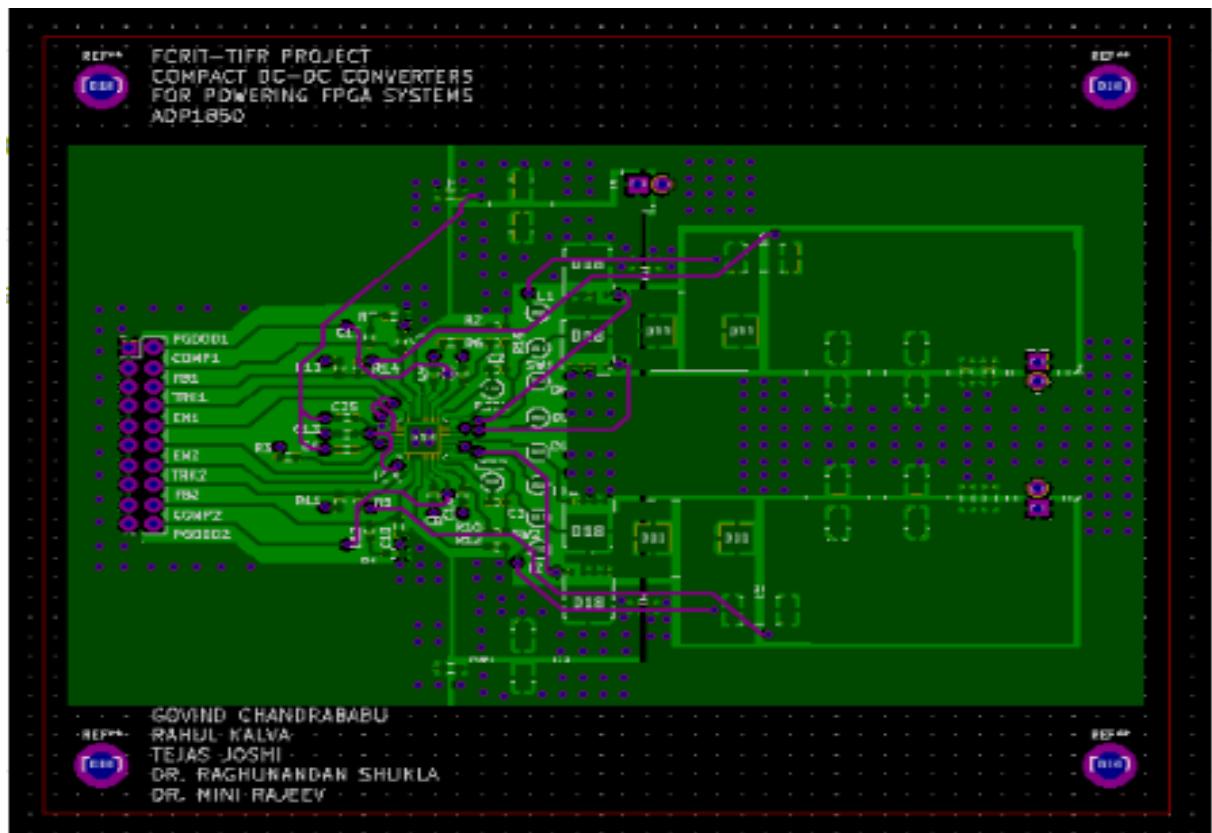


Figure 4.2: PCB Layout of ADP1850

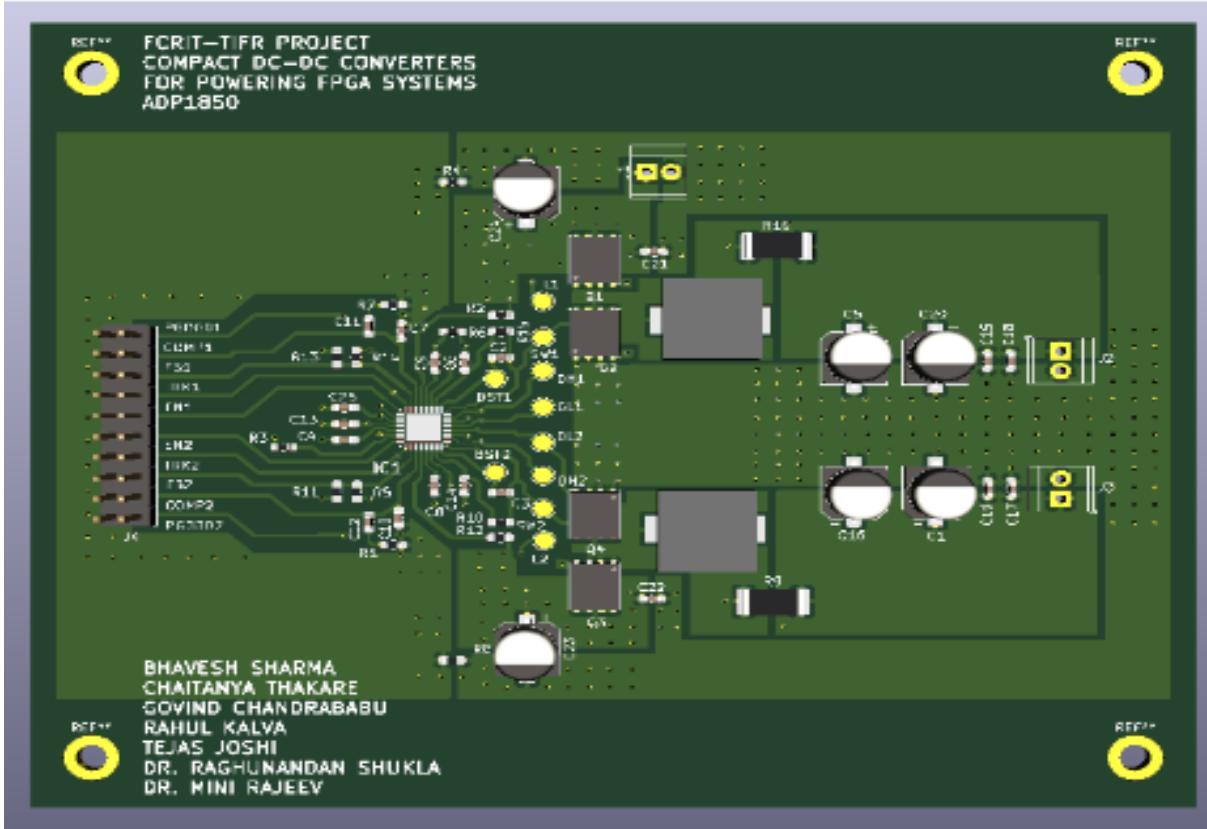


Figure 4.3: 3D View of the designed PCB for ADP1850

4.3.2 LT8652S PCB Design

The package used is a 36-lead 4mm x 7mm QFN package with 6 exposed pads. The four layer stackup had the front and back layers as signal layers. All the components were placed on the front layer. The second layer consisted of two ground planes, signal and power ground. These were connected on the front layer by two isolation resistors. The third layer had an input voltage plane and a power ground. The input voltage layer was incorporated to connect the input terminal block on the edge of the PCB to the IC input terminals. A 7x2 pin header was used to allow external connections for soft starts, PGoods, enable and compensation pins.

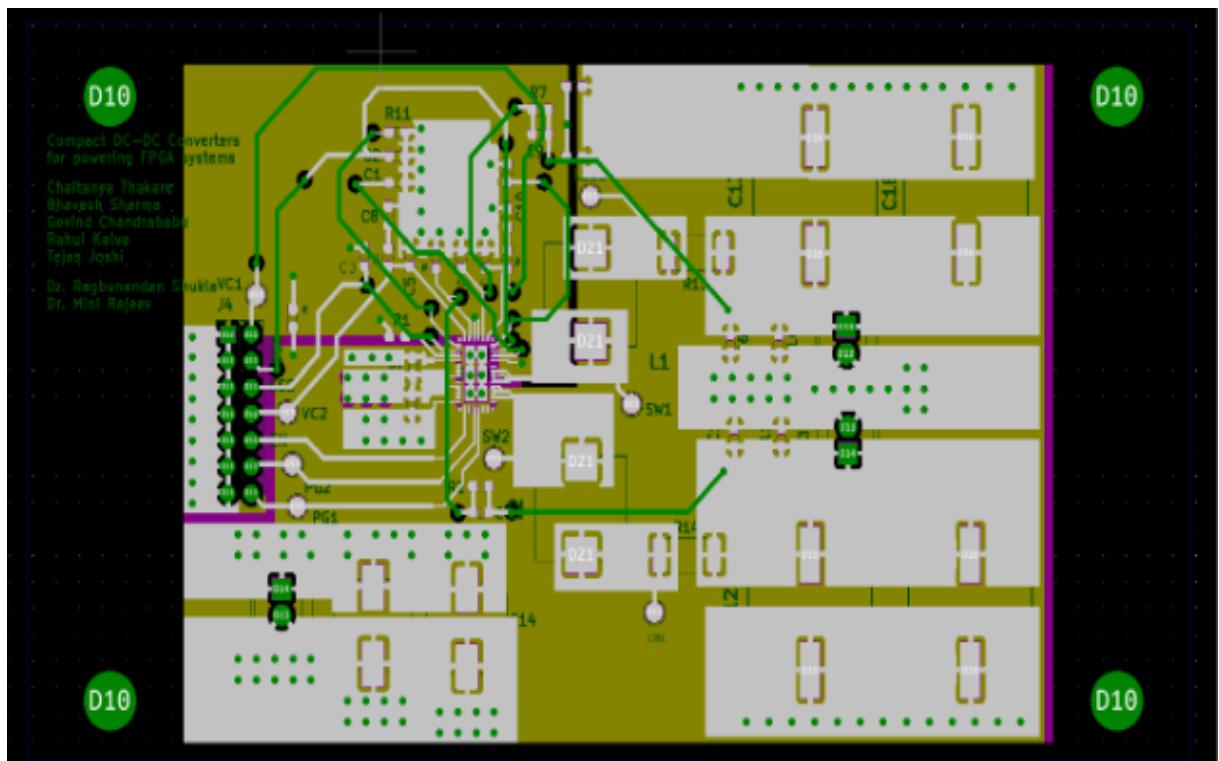


Figure 4.4: PCB Layout of LT8652S

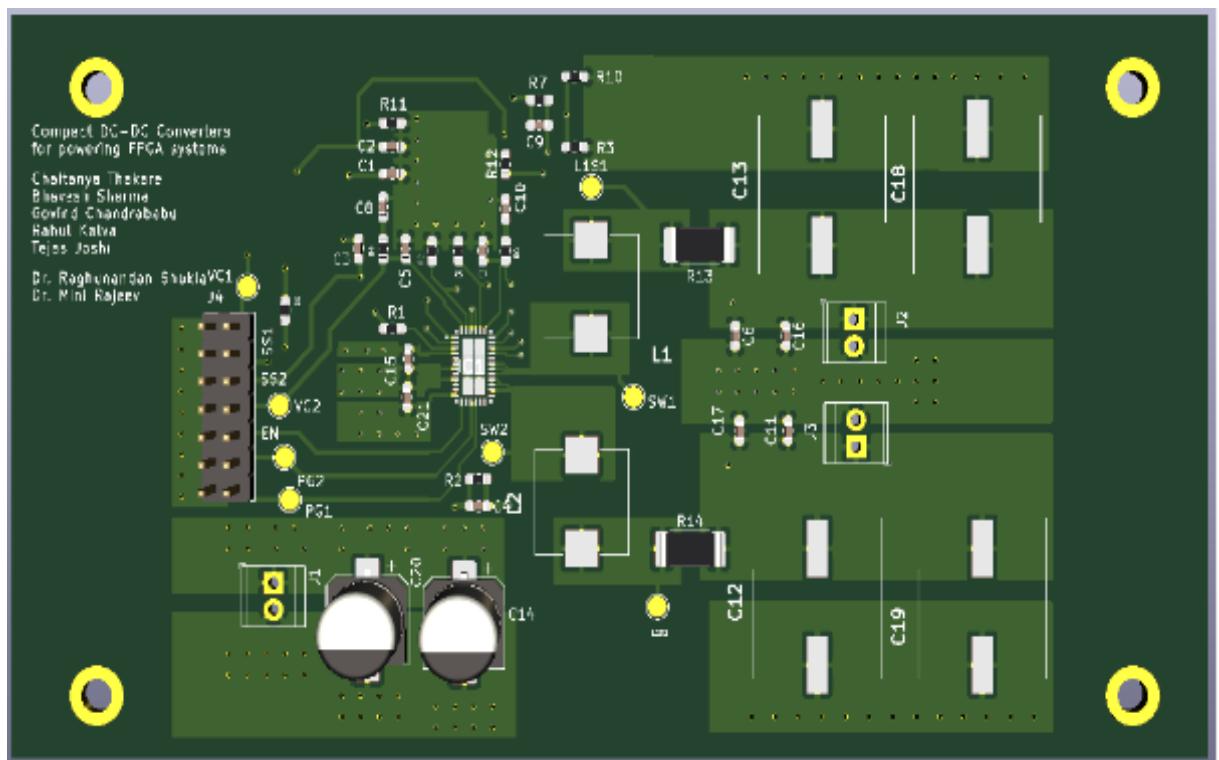


Figure 4.5: 3D View of the designed PCB for LT8652S

4.3.3 LTC3884 PCB Design

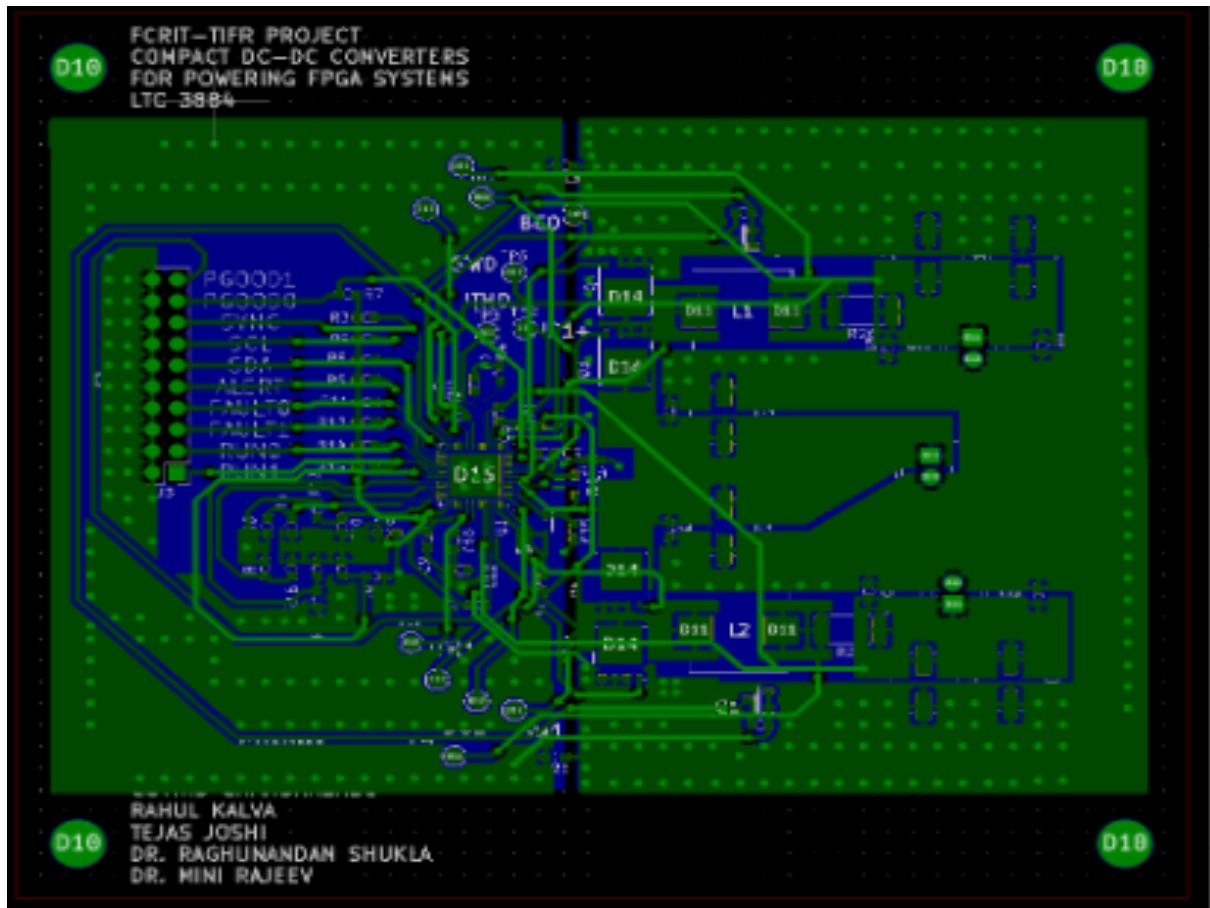


Figure 4.6: PCB Layout of LTC3884

The LTC3884 is manufactured in a 48-Lead Plastic QFN (7mm × 7mm) with an exposed pad for thermal dissipation. While placing the components, the controller was placed in centre and then other components were placed around with priority given to decoupling capacitors placing them close to the pins they are connected to so as to reduce the trace resistance and inductance. Precedence was given to the traces carrying the gate driving signal as they are noisy and elongating the paths will cause higher turn ON/OFF times.

The voltage and current sensing paths were kept distant to the switch node paths as noise might be introduced to those nodes leading to faulty sensing of voltage and current, which would further influence the operation of switching controller leading to maloperation. The left half of 2nd and 3rd layers were used as Signal Grounds (SGND/AGND) and connected to the right half which was used as Power Ground (PGND). A 20 pin pinheader was used to make the PM-Bus communication pins available so as to program the controller using an Arduino or a micro-controller with a

ground pin provided for every individual PM-Bus pin.

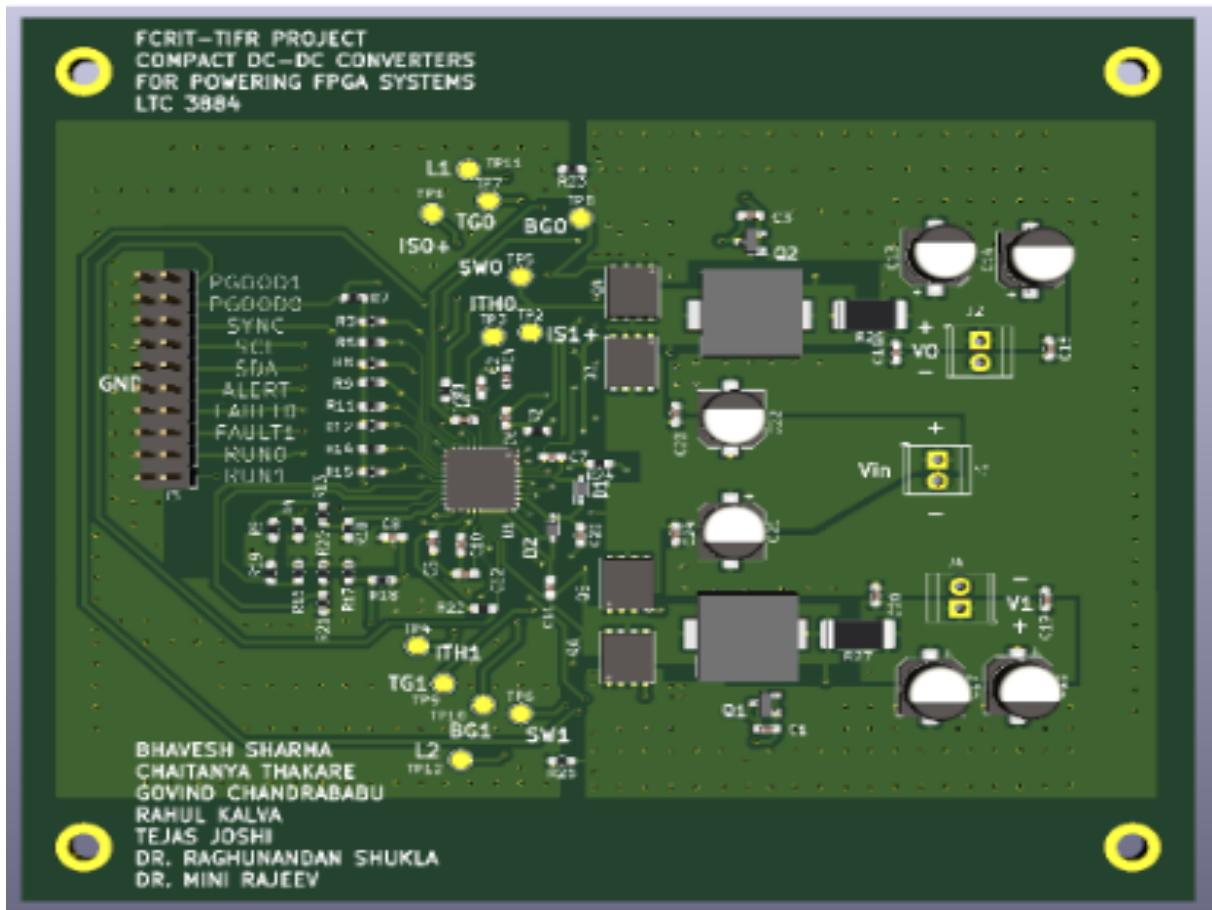


Figure 4.7: 3D View of the designed PCB for LTC3884

Keeping the current flow direction in consideration, the path of current from the switches to the output pin was kept as short as possible to ensure low resistance.

Chapter 5

Result and Discussion

5.1 Simulation Results and Analysis

The Simulations of all the selected Switching Regulators were performed in LTspice XVII. LTspice is a open source SPICE-based analog electronic circuit simulator computer software. Macromodels of all the above selected Switching Regulators were available in the software. All the values of supported resistor and capacitors (soft start capacitor or frequency setting resistor etc) were calculated referring the respective datasheets of the regulators and used in the simulation. All the Selected Switching Regulator are dual output and both the outputs are used simultaneously in the Simulations. Readily Available DC power supply Voltage of 5V and 12V were considered as the input voltage for all the regulators. Below 3 subsections provide a brief detail about the simulation results of individual switching regulators.

5.1.1 ADP1850 Simulation

Unlike other two Regulators, ADP1850 has a high value of minimum ON time and as a result there is a limitation for switching frequency in its case. Voltage Transients were high in high output voltage and therefore the frequency had to be reduced to overcome this voltage transient. The waveforms obtained from LTspice Simulations are shown below

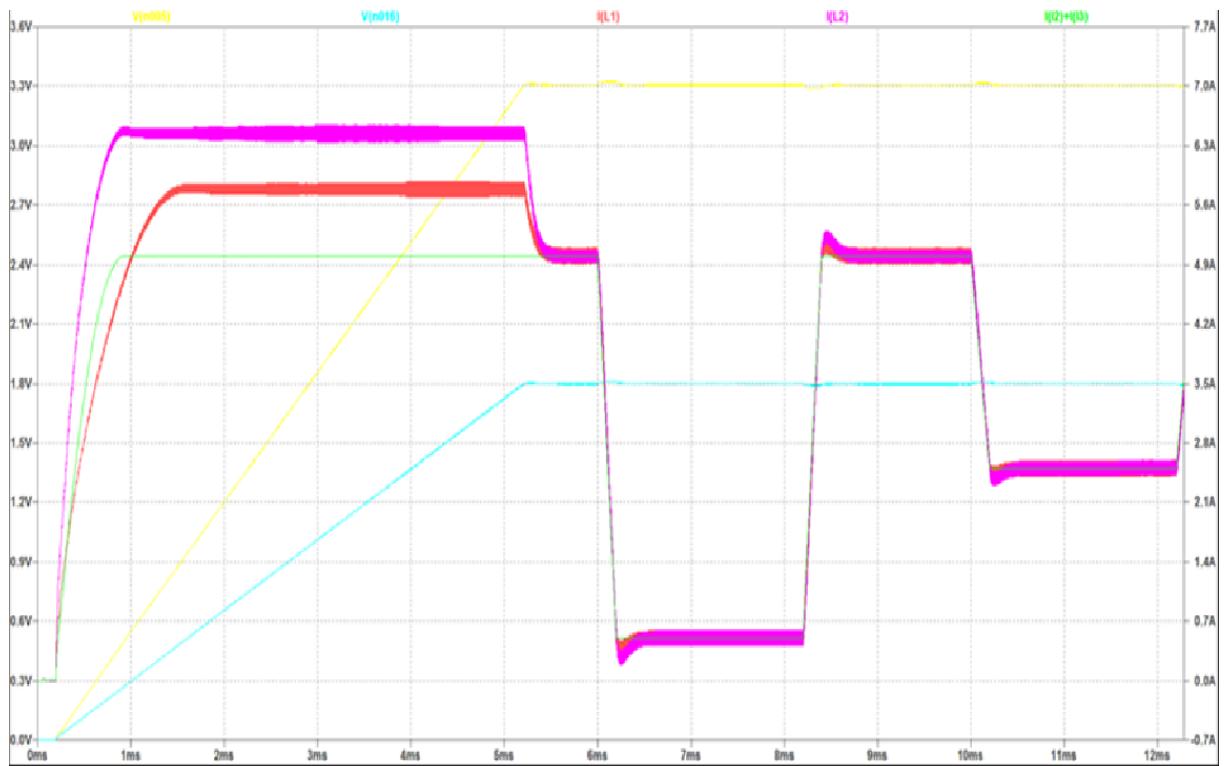


Figure 5.1: 3.3V, 1.8V Output and Inductor current Waveform

In Figure 5.1, the red and violet waveforms are the inductor currents which loosely resembles the load current with ripple included. The yellow and blue wave forms are the 3.3V and 1.8V output voltage waveform.

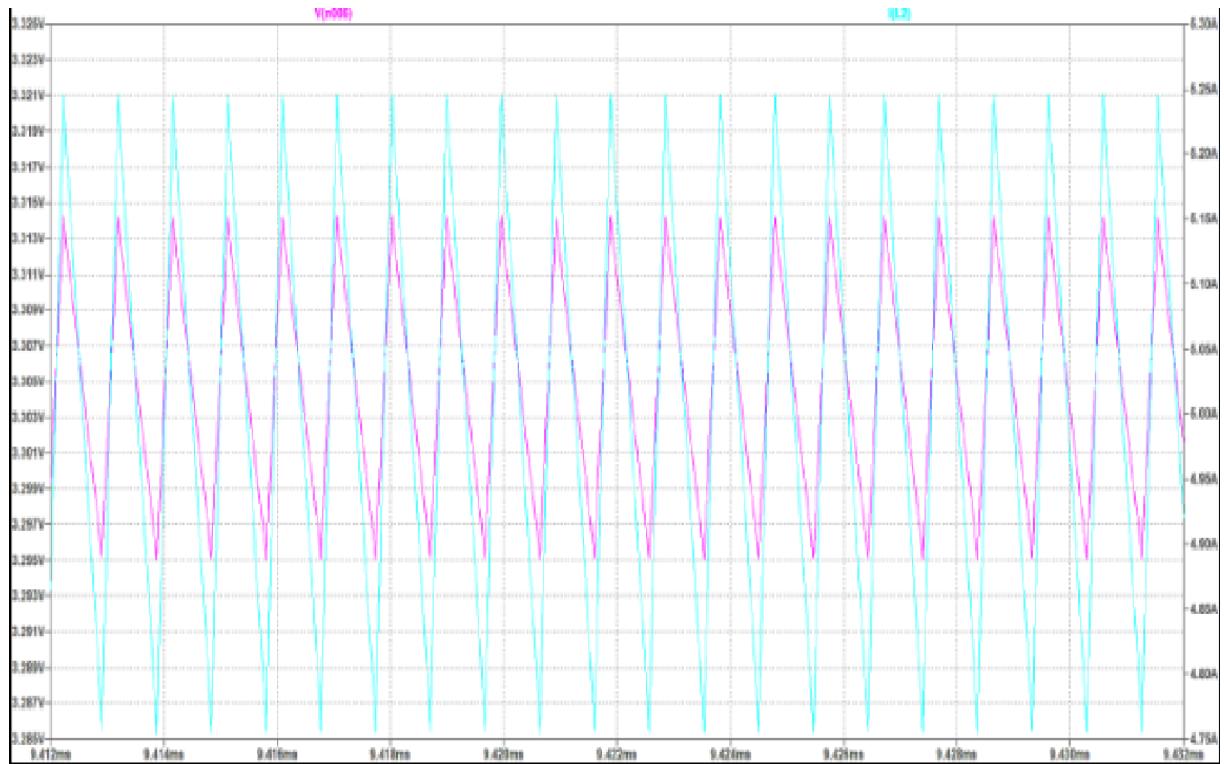


Figure 5.2: Inductor current and Output Voltage ripple Waveform

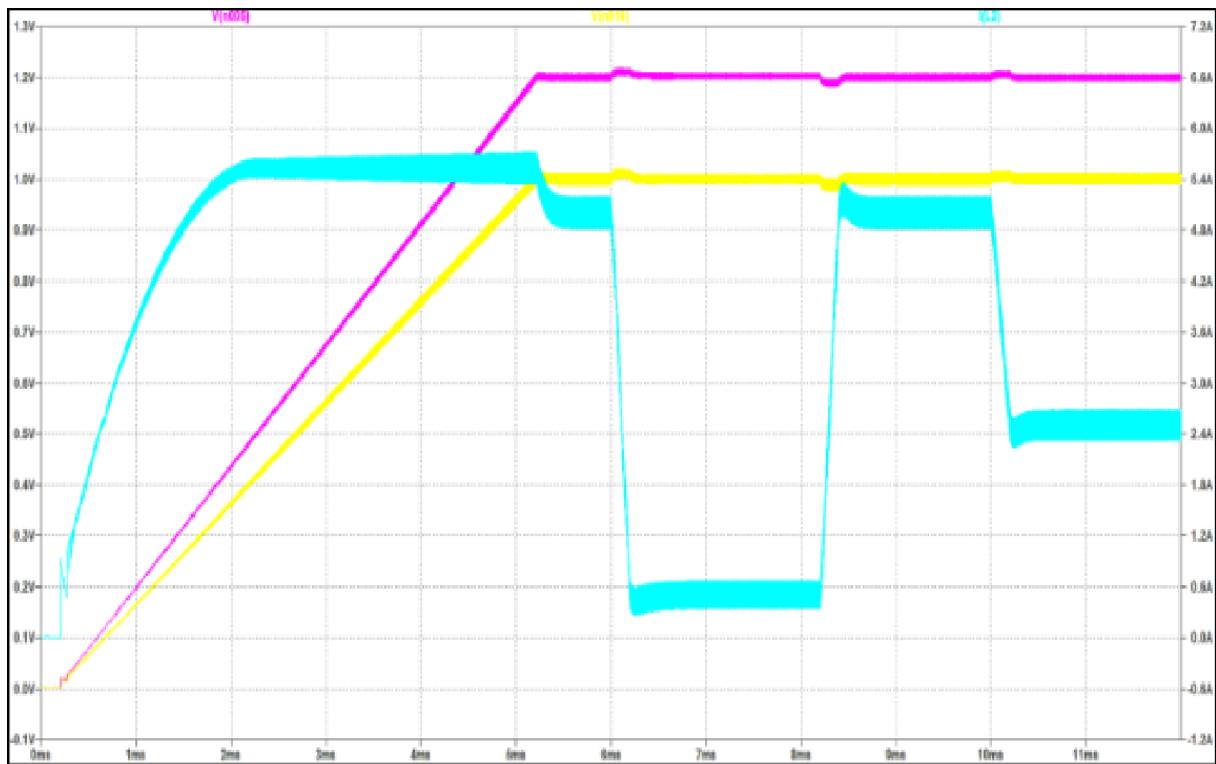


Figure 5.3: Inductor current, 1.2V and 1V output voltage Waveform

Figure 5.2 shows the ripple current in blue and ripple voltage in violet obtained at the output of the buck converter. Figure 5.3 shows the output for lower voltage rails, i.e. 1.2V (in violet) and 1V (in yellow) and the blue waveform shows the inductor.

In all the output waveforms, it is observed that the voltage change during high load transients were found to be in the required limits as well as the power quality observed at the output was satisfactory with the voltages rising steadily as set by the ramp capacitor value so as to limit the inrush current which is observed to 6.5A and even lower for the lower voltage levels.

5.1.2 LT8652S Simulation

LT8652S has a wide range of frequency and a very low minimum on/off time. This permits high switching frequency. The maximum possible value was used for some of the voltage levels. Output inductor and capacitor values were designed for extreme case and the same values were used for every voltage level.

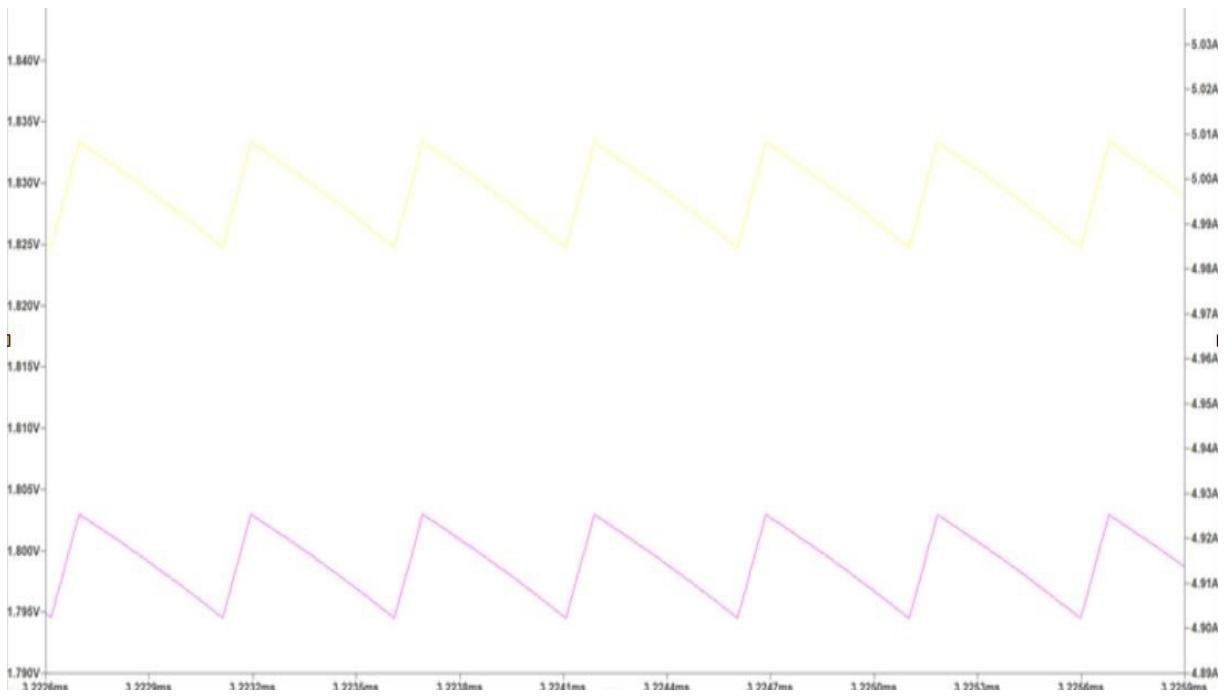


Figure 5.4: Steady state waveforms, 1.8V channel, Purple: Output voltage, Yellow: Output current

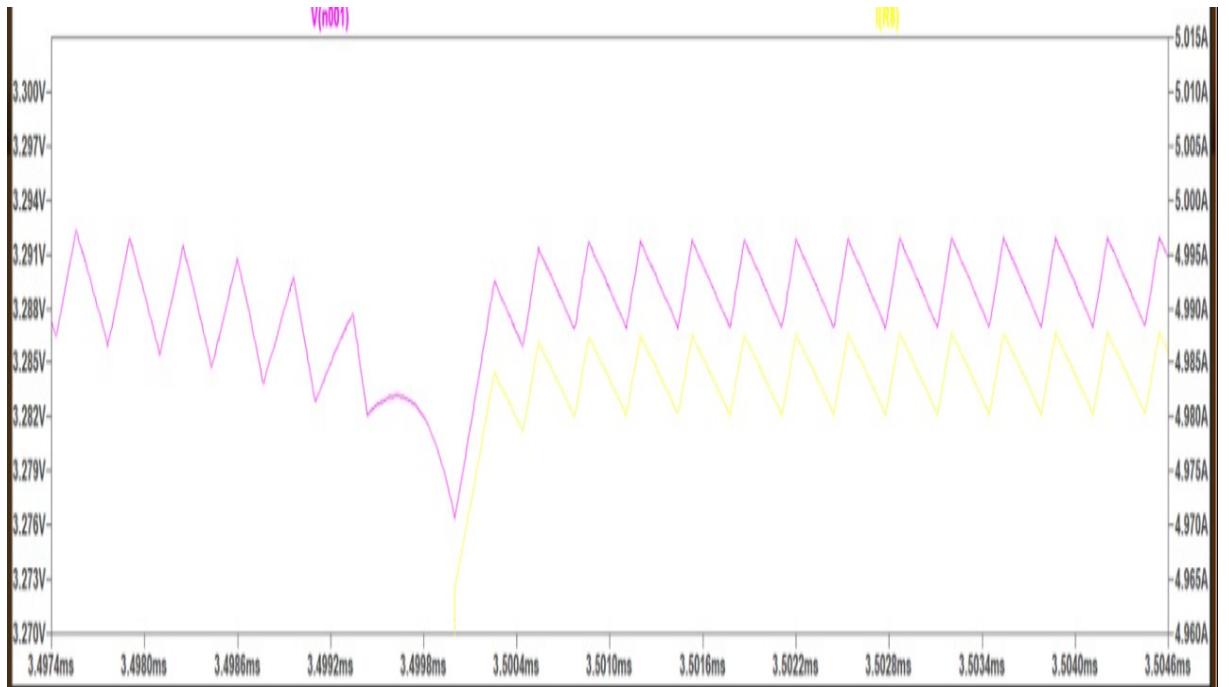


Figure 5.5: Transient at 3.3 V channel, Purple: Output voltage

We observe the output voltage and current waveform in steady state in figure 5.4. The steady state error is very less during operation. Figure 5.5 represents a transient wherein output current rises from 0.5A to 5A and the corresponding drop in voltage is recorded. Due to appropriate compensating components and output capacitors, the voltage drop is within limits and it returns to its original value quickly.

5.1.3 LTC3884 Simulation

Since LTC3884 is a programmable controller, the simulation did not yield the desired output as it requires programming the controller to with parameters which was not possible in the LTSpice environment. Also considering the reliability of simulations as compared to actual hardware, it was decided to program the controller using the resistor configuration pins and directly implement it in hardware.

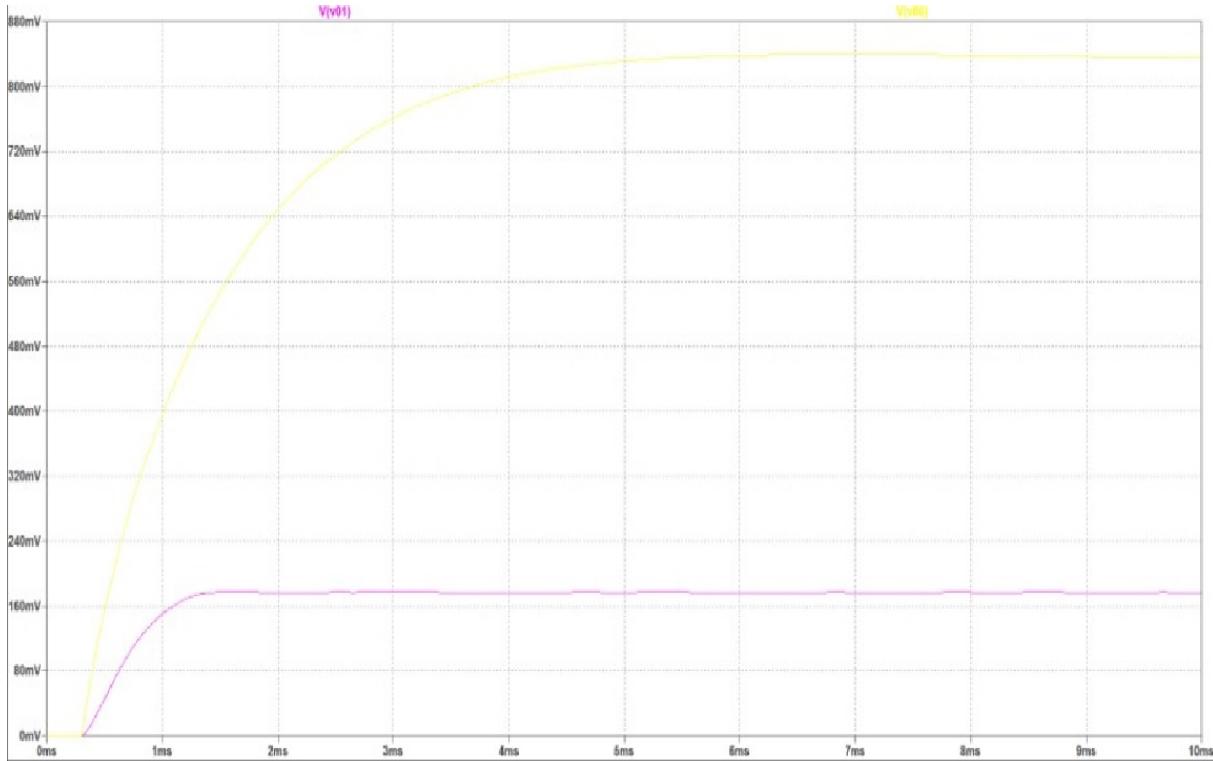


Figure 5.6: Inductor current and Output Voltage ripple Waveform of LTC3884

As can be seen in Figure 5.6, the violet waveform is 1V which fails to rise to the required voltage and similarly the yellow waveform is 3.3V, which too does not reach the desired voltage. Thus the output yielded by the means of simulation was not satisfactory. The simulation parameters were checked against the reference design as provided in the LTC3884 datasheet [8], but a successful output was not obtained.

5.2 Hardware Implementation and Result

After satisfactory outputs of simulation, a list of components required for hardware implementation was made. The PCB design files in KiCAD were converted to Gerber files which is a requirement for the manufacturer to print the PCBs. The components were ordered and the PCBs were assembled at TIFR premises during multiple visits. Preliminary testing

was done at TIFR to ensure the PCBs were functioning correctly. Out of the 3 PCBs, ADP1850 PCB was brought to college for further stress testing.

5.2.1 ADP1850

Fig. 5.7 shows the soldered PCB of ADP1850 switching regulator.

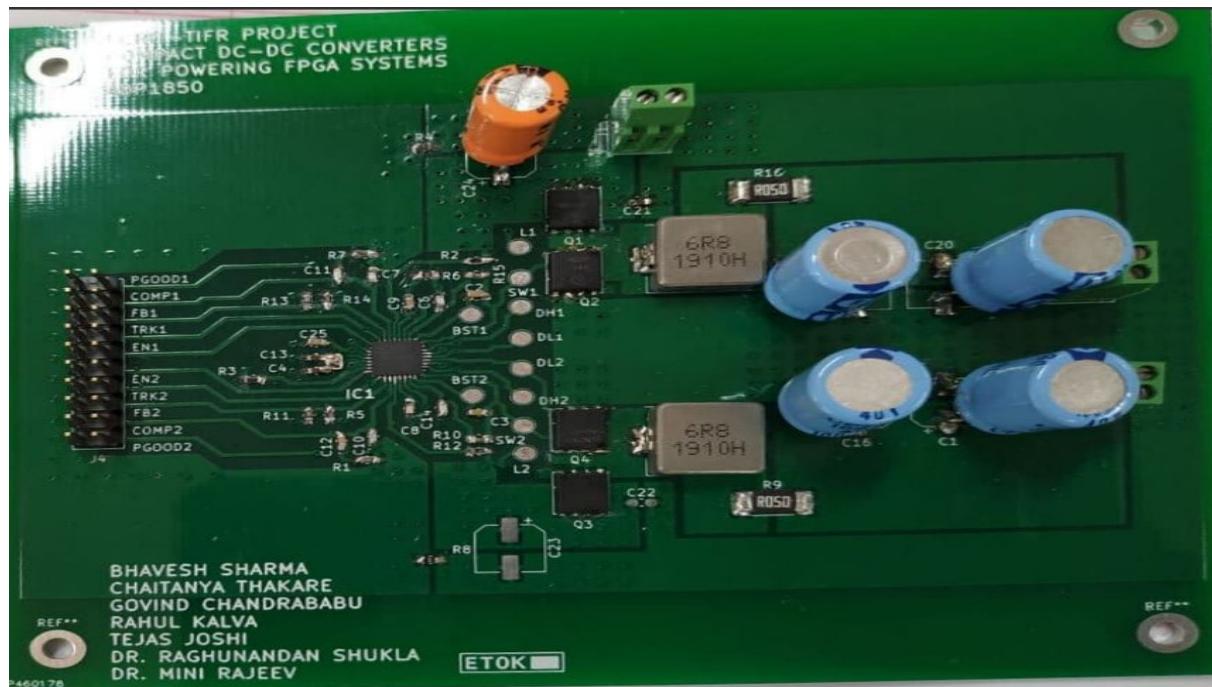


Figure 5.7: ADP1850 soldered PCB

The lab equipment used for ADP1850 PCB testing were

- PSB-1000 Programmable Multi range DC Power Supply
 - Chroma 6312A Programmable DC Electronic Load
 - Tektronix TBS 1072B-EDU Oscilloscope
 - Pintech 100AAC/DC Current Probe PI-710
 - Connecting wires

The input voltage given to the switching controller was 5V. An electronic load was used to load the assembled PCB. Loading was gradually increased. For transient testing various values of slew rate were also used with varying levels of current. Various waveforms were observed on oscilloscope to verify the correct operation of the switching converter. Fig. 5.8 depicts the laboratory set up for testing.

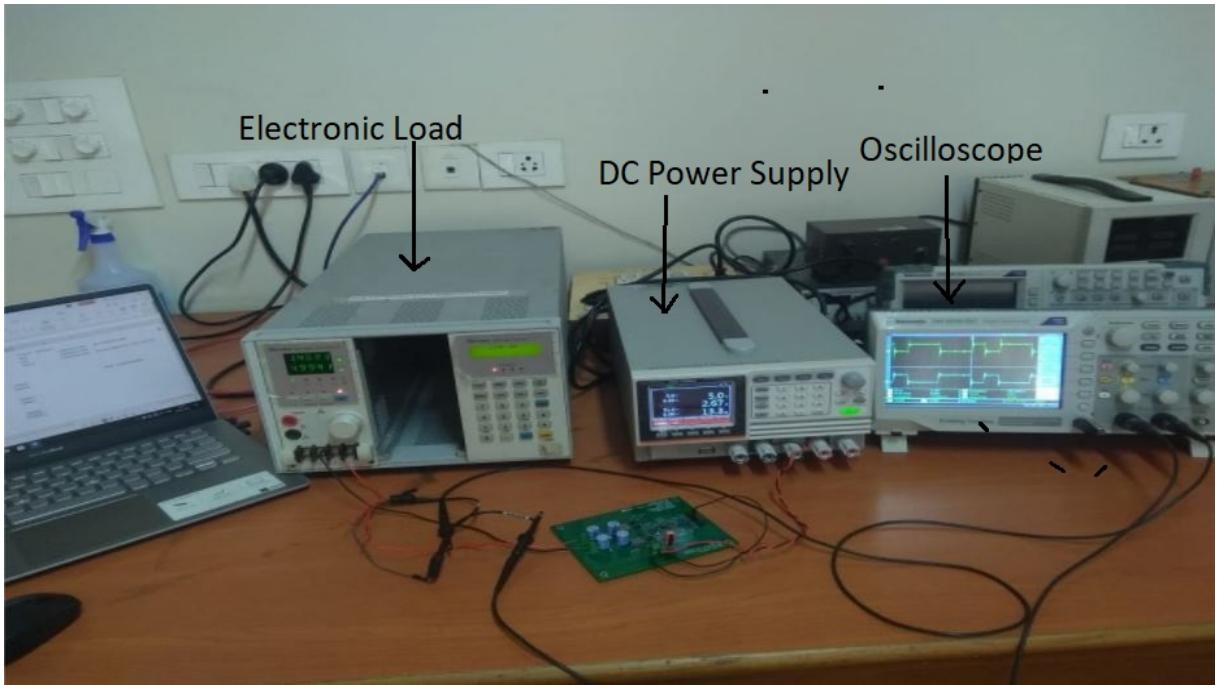


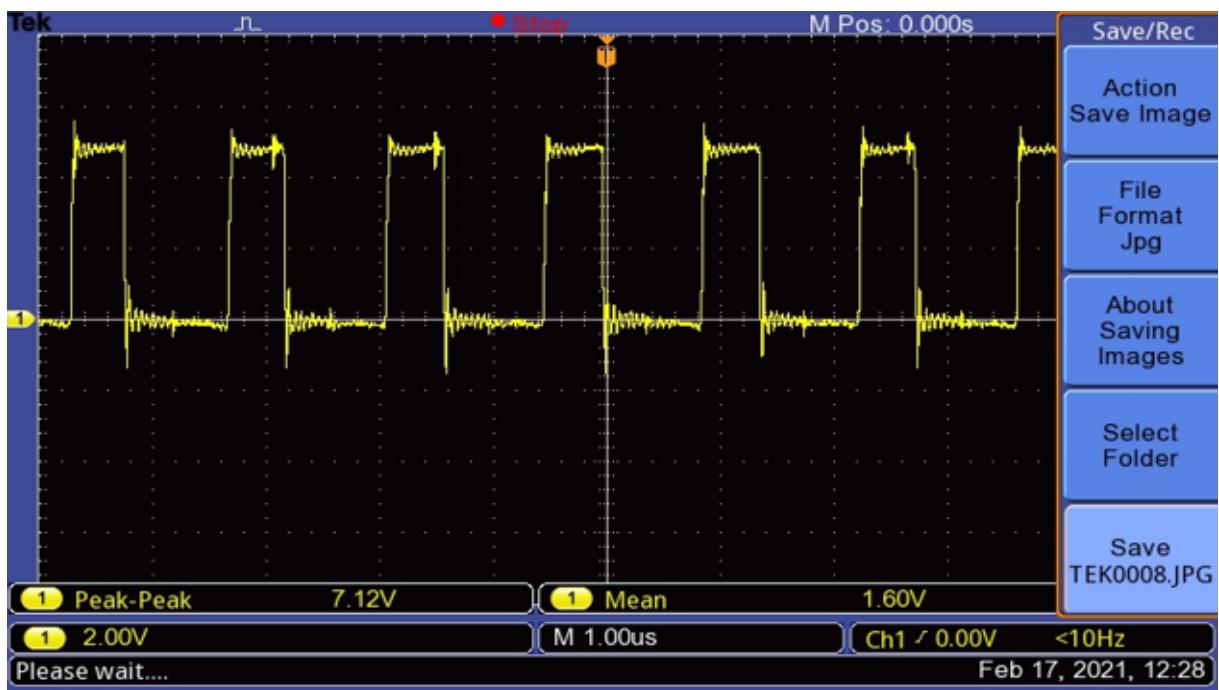
Figure 5.8: Lab Setup for ADP1850 Testing

Table 5.1 shows the design values of some of the components used in the PCB for testing.

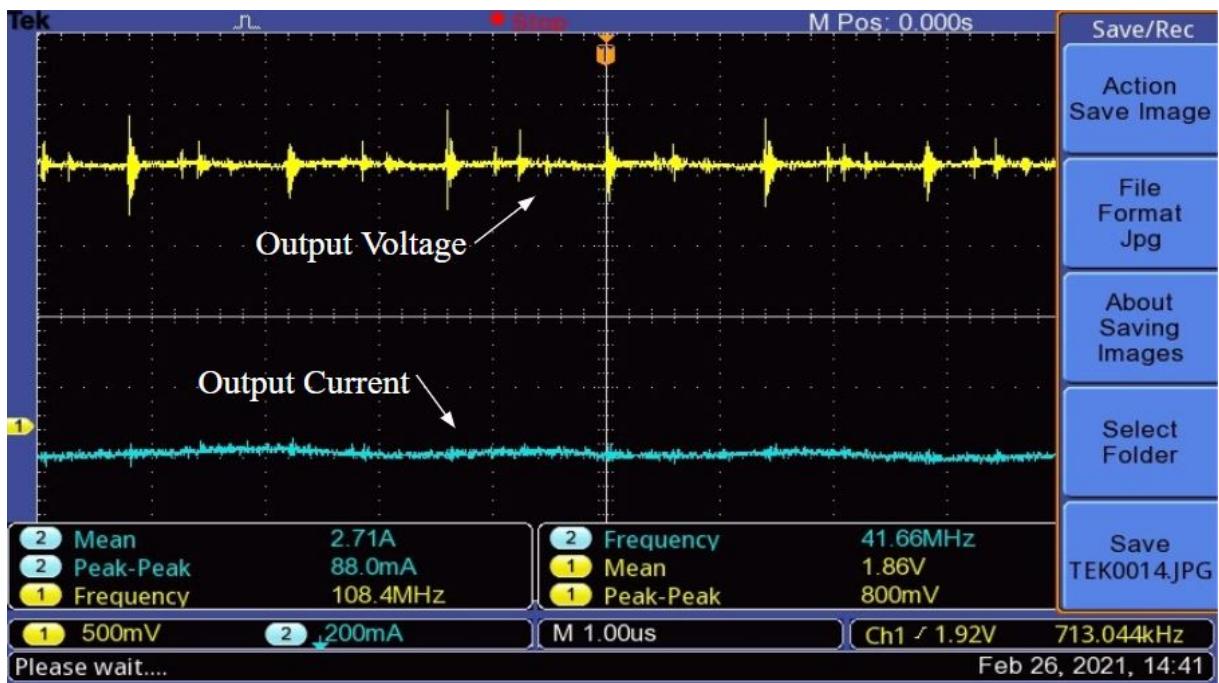
Table 5.1: Component values selected for Implementation

Component	Component Value	Description
Inductor	$6\mu H$	Limits current ripple in the output
Output Capacitor	$100\mu F$	Limits current ripple in the output
Frequency pin resistor	$86.6 \text{ k}\Omega$	Sets the switching frequency to 700kHz
Soft start Capacitor	56nF	Sets rise time during turn ON to 5ms

During hardware implementation BSC120N03MS MOSFET was used for it's compact packaging and high switching speed. To test whether the switching controller was providing appropriate pulses to the MOSFETs, gate to source voltage of MOSFETs was checked for 1.8V channel as can be seen in Fig. 5.9 which were found to be satisfactory and were providing pulses adequate enough to turn ON the MOSFET.



The time period of pulses observed was $1.4\mu s$ which corresponds to 714kHz frequency which is close to the frequency selected. The pulses had ON time of $0.6\mu s$ and OFF time of $0.8\mu s$ which indicate that the switch is operating at a duty cycle of 0.42. This is approximately equal to the ratio of Output and Input Voltage (0.36) which indicates that the controller is providing correct switching pulses to the MOSFET.



The waveforms in Fig. 5.10 were obtained by testing ADP1850 PCB with an electronic load for the 1.8V channel drawing a constant 2.5A load current. The voltage spikes observed are due to switching noise and occur during switches turning ON and OFF.

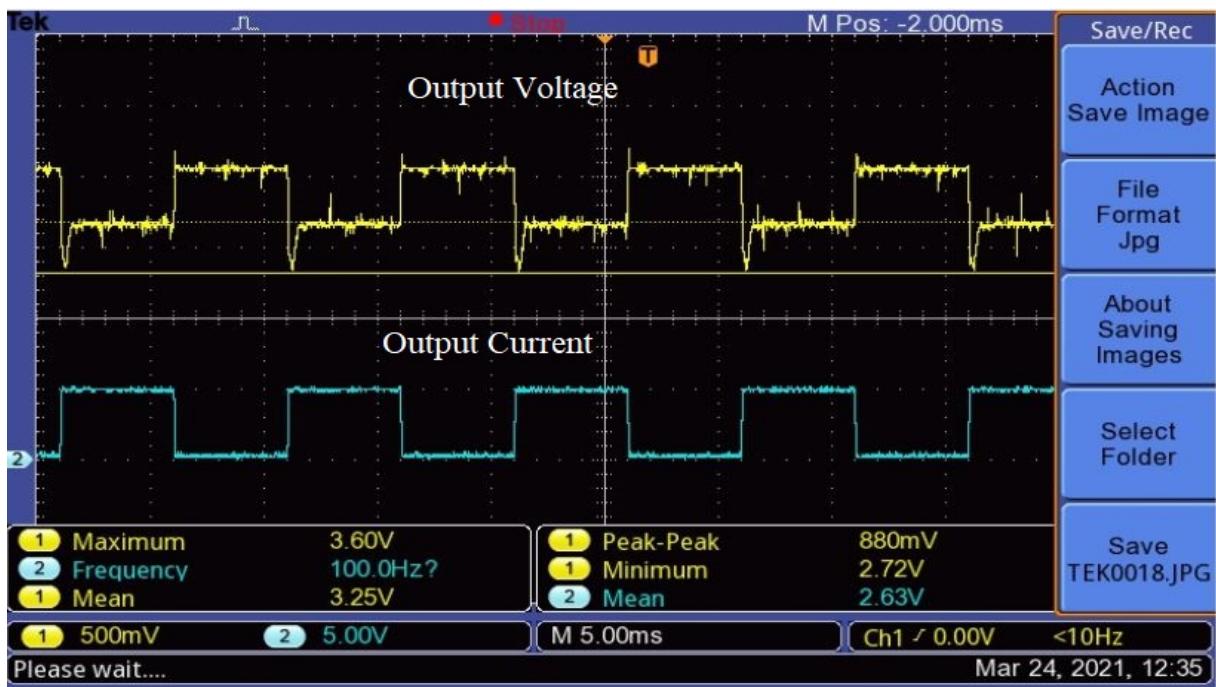


Figure 5.11: 3.3V Channel Transient Testing

The waveforms in Fig. 5.11 represent output voltage (yellow) and current (blue), the load was configured to draw 0.5A and 5A alternately at 100Hz and at a slew rate of $100\text{mA}/\mu\text{s}$. A voltage dip of 0.36V at the positive edge of the transient was observed. Results obtained while testing voltage drop during transient condition and steady state parameters with the controller ADP1850 were satisfactory.

5.2.2 LT8652S

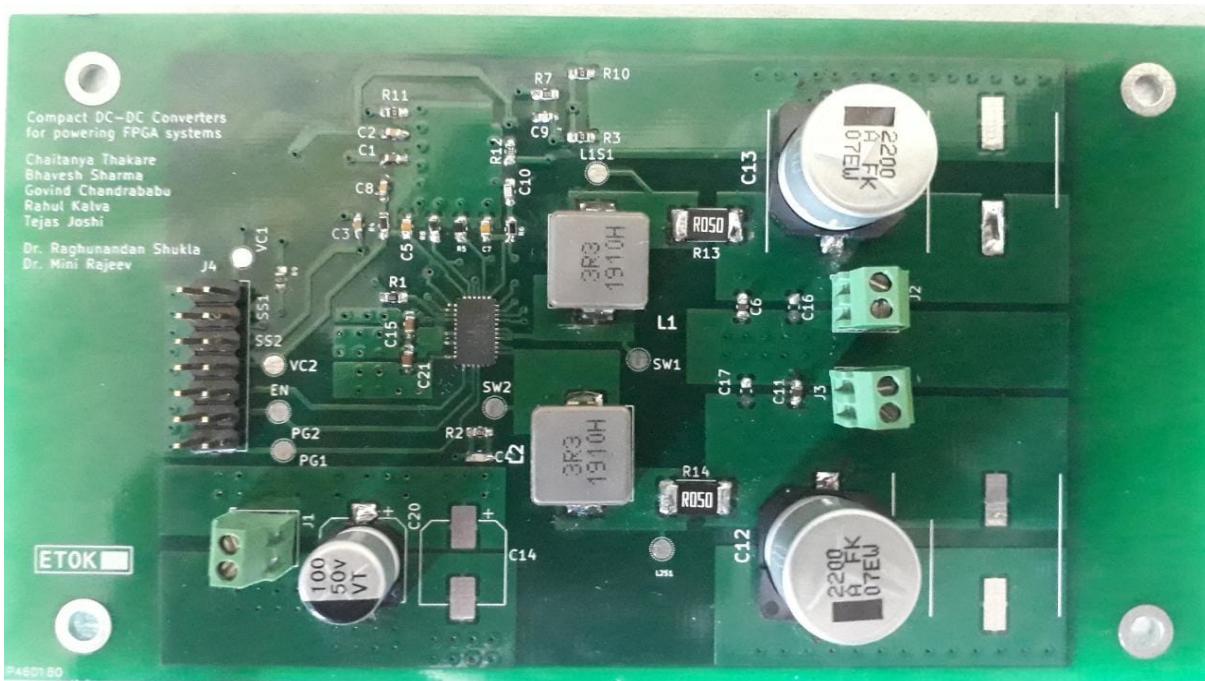


Figure 5.12: LT8652S soldered PCB

Fig. 5.12 shows the soldered PCB for LT8652S switching regulator. During the initial tests, satisfactory output was not obtained, neither did the switching regulator draw any input power. Debugging and if the situation arises, replacing the existing IC with another LT8652S IC forms the future scope for this switching regulator.

5.2.3 LTC3884

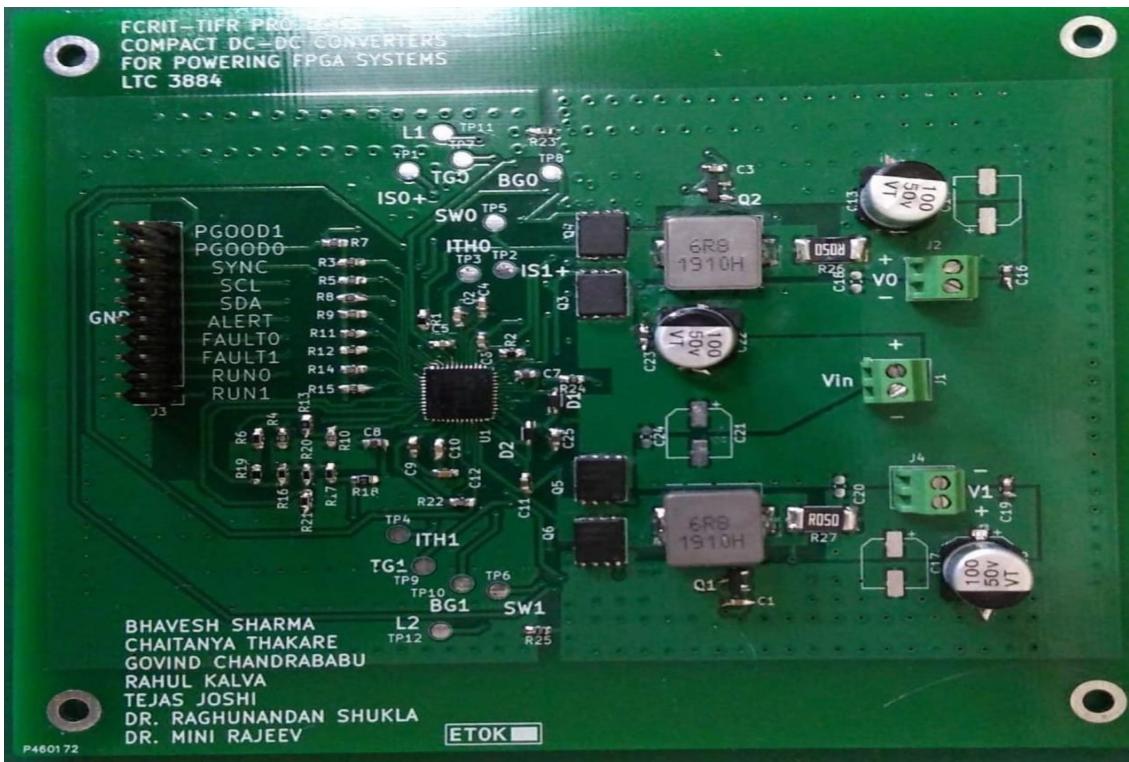


Figure 5.13: LTC3884 soldered PCB

Fig. 5.13 is an image of the final soldered PCB of the LTC3884 prototype. The operation of the LTC3884 is possible with and without programming functionality. The PMBus/I2C protocol can be used to communicate with the LTC3884. Initial testing of the LTC3884 produced unsatisfactory results, leading to implementation of the programmability functionality of the LTC3884.

To implement the I2C protocol, communication was established with the LTC3884 using an Arduino Uno as the Master device in the I2C protocol, with the LTC3884 acting as the slave device. The LTC3884 was first tested for functioning programmability, with device address testing. The global address and the local address of the LTC3884 were found to be 0x5A and 0x21 respectively using a device scanner script.

With conformation of the PMBus programmability access, we read the various internal registers of the LTC3884 to gauge the current state of the LTC3884. The LTC 3884 supports more than 80 commands of the PMBus protocol, with these commands being reverse compatible with I2C protocol as well[8]. The LTC3884 was designed to use different data conversion

protocols for various parameters such as the Linear 16u format, the Linear 5s 11s format, the Register format, the Integer Word format, the ASCII format, and Custom formats for individual commands.

When queried using the Wire library of the Arduino Uno, the LTC3884 returns binary data in response to the read command. This binary data has to be converted to useful information through processing the binary information using the algorithms mentioned in the respective data formats for each command. Data conversion programs were used to do the same.

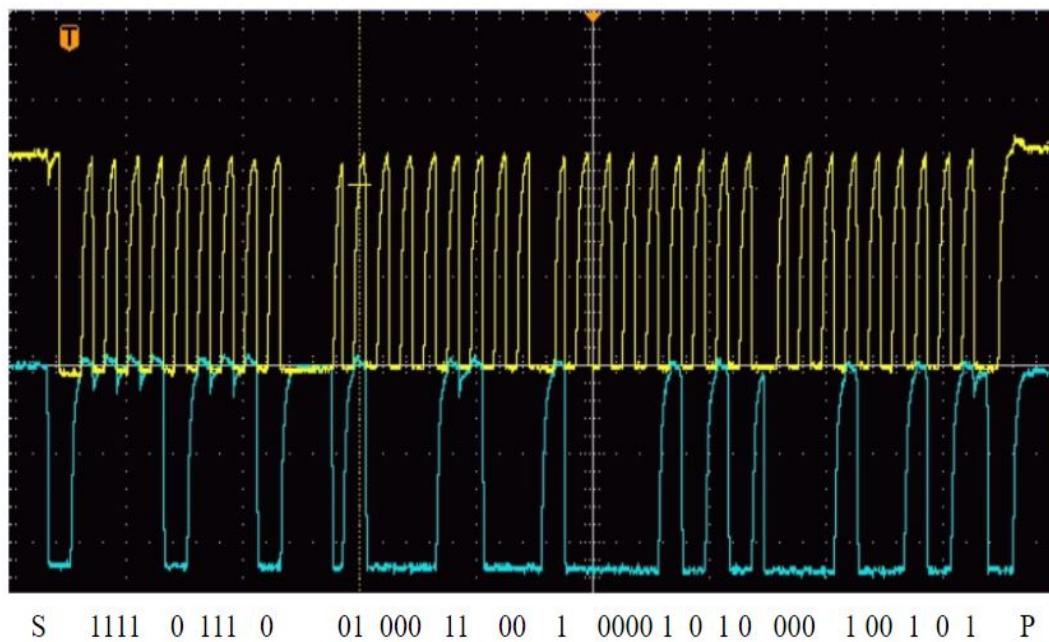


Figure 5.14: I₂C protocol to read data from the output over-current fault limit register

The internal registers of the device revealed that the LTC3884 was facing problems which were triggering fault conditions, as indicated in the CML status register and the temperature register[11]. The temperature register indicated problems with the temperature sensing component of the device, causing over-temperature fault conditions to trigger even in no load conditions. This issue was resolved by shorting the faulty temperature sensing unit, and this approach resolved the fault in the temperature register.

Table 5.2: Bits observed in STATUS_TEMPERATURE register, ADDRESS-0x7D

Bit	Meaning	Observed
7	External overtemperature fault	0
6	External overtemperature warning	1
5	Not supported (LTC3884 returns 0)	0
4	External undertemperature fault	0
3	Not supported (LTC3884 returns 0)	0
2	Not supported (LTC3884 returns 0)	0
1	Not supported (LTC3884 returns 0)	0
0	Not supported (LTC3884 returns 0)	0

Table 5.3: Bits observed in STATUS_CML register, ADDRESS-0x7E

Bit	Meaning	Observed
7	Invalid or unsupported command received	0
6	Invalid or unsupported data received	1
5	Packet error check failed	0
4	Memory fault detected	0
3	Processor fault detected	0
2	Reserved (LTC3884 returns 0)	0
1	Other communication fault	0
0	Other memory or logic fault	0

The CML register showed an improper data protocol error, which could be caused by the lack of packet error checking(PEC), an expected byte of data in PMBus protocols, in the Wire library for the Arduino Uno. This issue is also suspected to be the main hindrance in writing to the LTC3884. Therefore, future scope of the LTC3884 includes resolution of the PEC error and testing of the LTC3884 PCB.

Chapter 6

Conclusion & Future Scope

This report broadly presents the design and implementation of a DC-DC converter system for FPGAs. Various techniques to make a DC power supply are presented. Selection of the most suitable topology along with the means to achieve the same are discussed. Buck converter based switching regulator ICs, namely ADP1850, LT8652S and LTC3884, are presented as an approach and building block of the power supply. Design requirements and procedure to determine component values and other parameters regarding the regulator ICs are put forth. Designs are tested for various conditions and results are verified, software results are presented for the same. The PCB designing for each of the models is presented which was further realised in the hardware part of the project. The proposed solution proved to be more cost effective compared to solutions available in the industry.

Future scope involves further debugging and testing of the LT8652S and the LTC3884, along with PCB redesign of the ADP1850 to provide a more compact and user-friendly design, with changeable configuration resistors to provide variable voltage levels at the output terminals of the design. The prototypes were designed to accommodate extra components required for satisfactory operation, but the final product will be designed to improve overall efficiency, layout, and operation of the ADP1850 design. Microcontroller based control of LTC3884 via I₂C/PMBus is implemented and further error resolution is required to allow write command protocols to be processed by the LTC3884 and initiate regular operation, succeeded by testing of the PCB design.

References

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- [7] *MAX15046 40V, High-Performance, Synchronous Buck Controller*. Maxim Integrated.
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Appendix

Technical Specifications of Components

ADP1850

Absolute Maximum Ratings

Parameter	Rating
VIN, EN1/EN2, RAMP1/RAMP2	21 V
FB1/FB2, COMP1/COMP2, SS1/SS2, TRK1/TRK2, FREQ, SYNC, VCCO, VDL, PGOOD1/PGOOD2	-0.3 V to +6 V
ILIM1/ILIM2, SW1/SW2 to PGND1/PGND2	-0.3 V to +21 V
BST1/BST2, DH1/DH2 to PGND1/PGND2	-0.3 V to +28 V
DL1/DL2 to PGND1/PGND2	-0.3V to VCCO + 0.3 V
BST1/BST2 to SW1/SW2	-0.3 V to +6 V
BST1/BST2 to PGND1/PGND2	32 V
20 ns Transients	
SW1/SW2 to PGND1/PGND2	25 V
20 ns Transients	
DL1/DL2, SW1/SW2, ILIM1/ILIM2 to PGND1/PGND2	-8 V
20 ns Negative Transients	-0.3 V to +0.3 V
PGND1/PGND2 to AGND	-8 V to +4 V
PGND1/PGND2 to AGND 20 ns Transients	32.6°C/W
θ_{JA} on Multilayer PCB (Natural Convection) ^{1,2}	Operating Junction Temperature Range ³
Operating Junction Temperature Range ³	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Soldering Lead Temperature	260°C

Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		2.75	20		V
Undervoltage Lockout Threshold	$V_{IN,UVLO}$	V_{IN} rising V_{IN} falling	2.45	2.6	2.75	V
Undervoltage Lockout Hysteresis			2.4	2.5	2.6	V
Quiescent Current	I_{IN}	$EN1 = EN2 = V_{IN} = 12\text{ V}, V_{FB} = V_{CCO}$ in PWM mode (no switching)	0.1	4.5	5.8	mA
Shutdown Current	$I_{IN,SD}$	$EN1 = EN2 = V_{IN} = 12\text{ V}, V_{FB} = V_{CCO}$ in PSM mode $EN1 = EN2 = GND, V_{IN} = 5.5\text{ V}$ or 20 V	2.8	100	200	mA μA
ERROR AMPLIFIER						
FBx Input Bias Current	I_{FB}		-100	+1	+100	nA
Transconductance	G_m	Sink or source 1 μA	385	550	715	μS
TRK1, TRK2 Input Bias Current	I_{TRK}	$0\text{ V} \leq V_{TRK1}/V_{TRK2} \leq 5\text{ V}$	-100	+1	+100	nA
CURRENT SENSE AMPLIFIER GAIN	A_{CS}	Gain resistor connected to DLx, $R_{CSG} = 47\text{ kΩ} \pm 5\%$	2.4	3	3.6	V/V
		Gain resistor connected to DLx, $R_{CSG} = 22\text{ kΩ} \pm 5\%$	5.2	6	6.9	V/V
		Default setting, R_{CSG} = open	10.5	12	13.5	V/V
		Gain resistor connected to DLx, $R_{CSG} = 100\text{ kΩ} \pm 5\%$	20.5	24	26.5	V/V
OUTPUT CHARACTERISTICS						
Feedback Accuracy Voltage	V_{FB}	$T_j = -40^\circ\text{C}$ to $+85^\circ\text{C}, V_{FB} = 0.6\text{ V}$	-0.85%	+0.6	+0.85%	V
		$T_j = -40^\circ\text{C}$ to $+125^\circ\text{C}, V_{FB} = 0.6\text{ V}$	-1.5%	+0.6	+1.5%	V
Line Regulation of PWM	$\Delta V_{FB}/\Delta V_{IN}$				±0.015	%/V
Load Regulation of PWM	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} range = 0.9 V to 2.2 V			±0.3	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVERS						
DHx Rise Time		$C_{DH} = 3 \text{ nF}, V_{BST} - V_{SW} = 5 \text{ V}$		16		ns
DHx Fall Time		$C_{DH} = 3 \text{ nF}, V_{BST} - V_{SW} = 5 \text{ V}$		14		ns
DLx Rise Time		$C_{DL} = 3 \text{ nF}$		16		ns
DLx Fall Time		$C_{DL} = 3 \text{ nF}$		14		ns
DHx to DLx Dead Time		External 3 nF is connected to DHx and DLx		25		ns
DHx or DLx Driver R_{ON} , Sourcing Current ¹	R_{ON_SOURCE}	Sourcing 2 A with a 100 ns pulse	2			Ω
		Sourcing 1 A with a 100 ns pulse, $V_{IN} = 3 \text{ V}$		2.3		Ω
DHx or DLx Driver R_{ON} Tempco	TC_{RON}	$V_{IN} = 3 \text{ V}$ or 12 V		0.3		$^{\circ}\text{C}$
DHx or DLx Driver R_{ON} , Sinking Current ¹	R_{ON_SINK}	Sinking 2 A with a 100 ns pulse		1.5		Ω
		Sinking 1 A with a 100 ns pulse, $V_{IN} = 3 \text{ V}$		2		Ω
DHx Maximum Duty Cycle		$f_{SW} = 300 \text{ kHz}$	90			%
DHx Maximum Duty Cycle		$f_{SW} = 1500 \text{ kHz}$	50			%
Minimum DHx On Time		$f_{SW} = 200 \text{ kHz}$ to 1500 kHz			135	ns
Minimum DHx Off Time		$f_{SW} = 200 \text{ kHz}$ to 1500 kHz			335	ns
Minimum DLx On Time		$f_{SW} = 200 \text{ kHz}$ to 1500 kHz			285	ns

LT8652S

Absolute Maximum Ratings

$V_{IN1}, V_{IN2}, EN, PG1, PG2$	18V
BIAS.....	12V
FB1, FB2, VC1, VC2, SS1, SS2, IMON1, IMON2	4V
SYNC.	6V

Operating Junction Temperature Range (Note 2)

LT8652SE -40°C to 125°C

LT8652SI -40°C to 125°C

Storage Temperature Range -65°C to 150°C

Maximum Reflow (Package Body) Temperature ... 260°C

Electrical Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input Voltage		●	2.6	3.0	V
V_{IN1} Quiescent Current in Shutdown	$V_{EN} = 0V, V_{SYNC} = 0V$		6	15	μA
V_{IN1} Quiescent Current in Sleep with Internal Compensation	$V_{EN} = 2V, V_{FB1} = V_{FB2} > 0.6V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V$	●	16	30 100	μA
V_{IN1} Quiescent Current in Sleep with External Compensation	$V_{EN} = 2V, V_{FB1} = V_{FB2} > 0.6V, V_{VC1} = V_{VC2} = FLOAT, V_{SYNC} = 0V$	●	210	260 300	μA
V_{IN} Current in Regulation	$V_{IN} = 6, V_{OUT} = 0.6, \text{Output Load} = 50mA, V_{SYNC} = 0V$		7	10	mA
Feedback Reference Voltage		●	596 592.8	600 600	mV
Feedback Voltage Line Regulation	$V_{IN} = 3.0V \text{ to } 18V$	●	0.004	0.02	%/V
Feedback Pin Input Current	$V_{FB} = 0.6V$		-20	20	nA
Minimum On-Time	$I_{LOAD} = 4A, SYNC = FLOAT$	●	20	45	ns
Oscillator Frequency	$R_T = 143k$ $R_T = 60.4k$ $R_T = 20k$	● ● ●	255 660 1.85	300 700 2.00	345 740 2.15
					kHz MHz

LTC3884

Absolute Maximum Ratings

$V_{IN}, I_{IN^+}, I_{IN^-}$	-0.3V to 40V	$V_{SENSE0^-}, V_{SENSE1^-}$	-0.3V to 0.3V
$(V_{IN} - I_{IN^+}), (I_{IN^+} - I_{IN^-})$	-0.3V to 0.3V	$EXTV_{CC}, INTV_{CC}$	-0.3V to 6V
BOOST0, BOOST1 (LTC3884)	-0.3V to 46V	$(EXTV_{CC} - V_{IN})$	5.5V
Switch Transient Voltage (SW0, SW1) (LTC3884).....	-5V to 40V	PGOOD0, PGOOD1.....	-0.3V to 3.6V
(BOOST0-SW0), (BOOST1-SW1) (LTC3884).....	-0.3V to 6V	RUN0, RUN1, SDA, SCL, ALERT.....	-0.3V to 5.5V
Top Gate Transient Voltage TG0, TG1 (LTC3884).....	-5V TO 46V	ASEL0, ASEL1, $V_{OUT0_CFG0}, V_{OUT1_CFG}$, FREQ_CFG, PHASE_CFG	-0.3V to 2.75V
V_{CC0}, V_{CC1} (LTC3884-1).....	-0.3V to 6V	FAULT0, FAULT1, SHARE_CLK, WP, SYNC	-0.3V to 3.6V
Top Gate Transient Voltage PWM0, PWM1 (LTC3884-1).....	-0.3V to 6V	TSNS0, TSNS1	-0.3V to 3.6V
$I_{SENSE0^+}, I_{SENSE0^-}, I_{SENSE1^+}, I_{SENSE1^-}$, $V_{SENSE0^+}, V_{SENSE1^+}$	-0.3V to 6V	$I_{TH0}, I_{TH1}, I_{THR0}, I_{THR1}$	-0.3V to 3.6V
		Operating Junction Temperature Range (Notes 2, 17, 18).....	-40°C to 125°C
		Storage Temperature Range	-65°C to 150°C*

*See Derating EEPROM Retention at Temperature in Applications Information section for junction temperatures in excess of 125°C.

Electrical Specifications

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Voltage						
V_{IN}	Input Voltage Range	(Note 11)	4.5	38		V
I_Q	Input Voltage Supply Current	$V_{RUNO,1} = 3.3V$ (Note 16) $V_{RUNO,1} = 0V$ (Note 16)	25		23	mA
V_{UVLO}	Undervoltage Lockout Threshold When $V_{IN} > 4.3V$	V_{INTVCC} Falling V_{INTVCC} Rising	3.55		3.90	V
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts	35			ms
$t_{OFF(MIN)}$	Short Cycle Retry Time		120			ms

Gate Drivers (LTC3884)

$TG\ R_{UP}$	TG Pull-Up $R_{DS(ON)}$	TG High	2.6		Ω
$TG\ R_{DOWN}$	TG Pull-Down $R_{DS(ON)}$	TG Low	1.5		Ω
$BG\ R_{UP}$	BG Pull-Up $R_{DS(ON)}$	BG High	2.4		Ω

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
$BG\ R_{DOWN}$	BG Pull-Down $R_{DS(ON)}$	BG Low	1.1			Ω
$TG\ t_r$	TG Transition Time: Rise Time	(Note 4) $C_{LOAD} = 3300\text{pF}$	30			ns
t_f	Fall Time	$C_{LOAD} = 3300\text{pF}$	30			ns
$BG\ t_r$	BG Transition Time: Rise Time	(Note 4) $C_{LOAD} = 3300\text{pF}$	30			ns
t_f	Fall Time	$C_{LOAD} = 3300\text{pF}$	30			ns
$TG/BG, t_{1D}$	Top Gate Off to Bottom Gate on Delay Time	(Note 4) $C_{LOAD} = 3300\text{pF}$ at Each Driver	30			ns
$BG/TG\ t_{2D}$	Bottom Gate Off to Top Gate on Delay Time	(Note 4) $C_{LOAD} = 3300\text{pF}$ at Each Driver	30			ns
$t_{ON(MIN)}$	Minimum On-Time		60			ns

PWM0/PWM1 Outputs (LTC3884-1)

PWM	PWM Output High Voltage PWM Output Low Voltage PWM Output in Hi-Z State	$I_{LOAD} = 500\mu\text{A}$ $I_{LOAD} = -500\mu\text{A}$	$V_{CC} - 0.2$ -5	0.2 5	μA
-------	---	---	----------------------	----------	---------------

PMBus Interface Timing Characteristics

t_{SCL}	Serial Bus Operating Frequency		●	10	400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3		μs
$t_{HD(STA)}$	Hold Time After Repeated Start Condition After This Period, the First Clock is Generated		●	0.6		μs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6	10000	μs
$t_{SU(STO)}$	Stop Condition Setup Time		●	0.6		μs
$t_{HD(DAT)}$	Date Hold Time Receiving Data Transmitting Data		●	0		μs
● $t_{SU(DAT)}$	Data Setup Time Receiving Data		●	0.3	0.9	μs
● $t_{TIMEOUT_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event		32		ms
● t_{LOW}	Serial Clock Low Period		●	255	1.3	μs
● t_{HIGH}	Serial Clock High Period		●	0.6		μs

PMBus Commands for LTC3884

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00	73
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80	77
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	77
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	102
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					73
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N					73
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	74
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	113
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	113
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	101
SMBALERT_MASK	0x1B	Mask ALERT activity	Block R/W	Y	Reg		Y	see CMD	103
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14	83
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000	84
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HI.	R/W Word	Y	L16	V	Y	2.75 0x2C00	83
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD	84
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33	84

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
VOUT_TRANSITION_RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00	90
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	425k 0xFB52	81
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40	82
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00	82
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	0.32 0xAA8F	85
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A	83
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	92
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133	83
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD	84
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66	84
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	93
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	45.0 0xE2D0	86
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	95
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	35.0 0xE230	87
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20	88
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8	97
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEA8	88
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	-40.0 0xE580	89
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	97
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0	81
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	92
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26	82
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	87
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	89

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200	89
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.00 0xD280	90
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	95
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	90
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.00 0xD200	90
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	150.0 0xF258	91
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	104
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	104
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	105
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	105
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	106
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA	106
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	107
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA	107
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	110
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	110
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	110
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	110
READ_TEMPERATURE_1	0x8D	External temperature sensor temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	110
READ_TEMPERATURE_2	0x8E	Internal die junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA	110
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA	110
READ_POUT	0x96	Measured output power	R Word	Y	L11	W		N/A	110
READ_PIN	0x97	Calculated input power	R Word	Y	L11	W		N/A	111
PMBus_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg			0x22	101
MFR_ID	0x99	The manufacturer ID of the LTC3884 in ASCII.	R String	N	ASC			LTC	101
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC3884	101
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		5.7 0x5B33	85
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N		%		5.0%	111
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	101

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	101
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	101
USER_DATA_03	0xB3	An NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000	101
USER_DATA_04	0xB4	An NVM word available for the user.	R/W Word	N	Reg		Y	0x0000	101
MFR_INFO	0xB6	Manufacturing specific information.	R Word	N	Reg				109
MFR_EE_UNLOCK	0xBD	Contact factory.							118
MFR_EE_ERASE	0xBE	Contact factory.							118
MFR_EE_DATA	0xBF	Contact factory.							118
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1D	75
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21	76
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the FAULT pin.	R/W Word	Y	Reg		Y	0x6993	98
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0xAE	79
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7	78
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	100
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	96
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	111
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back	R/W Byte	N	Reg			0x00	112
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350.0 0xFABC	91
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTC3884.	R/W Word	Y	L11	ms	Y	500.0 0xFBEB	91
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	111
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	111
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	111
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS	R Word	N	L11	A		NA	111
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	103
MFR_READ_ICHIP	0xE4	Measured supply current of the LTC3884	R Word	N	L11	A		NA	111
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA	108
MFR_ADDRESS	0xE6	Sets the 7-bit I ² C address byte.	R/W Byte	N	Reg		Y	0x4F	75
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3884 and revision	R Word	N	Reg			0x4C0X	101
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	5.0 0xCA80	87

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	115
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA	118
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	Reg		Y	NA	115
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	108
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA	113
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA	112
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10	80
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF	ppm/°C	Y	3900 0x0F3C	85
MFR_RVIN	0xF7	The resistance value of the V _{IN} pin filter element in mΩ.	R/W Word	N	L11	mΩ	Y	1000 0x03E8	82
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000	88
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to -273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	88
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	75
MFR_REAL_TIME	0xFB	48-bit share-clock counter value.	R Block	N	CF			NA	xx
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	77

Arduino Code for LTC3884 I2C Implementation

```

#include<Wire.h>

String d,r,i, a;
float Output;
double realval111;
byte b1,b2,b4,b5;
unsigned long b3,y,ds,Data;
signed long b6, Input;

void setup() {
Serial.setTimeout(10);
Serial.begin(9600);
Wire.begin();
}

void loop() {
while(Serial.available()){
Serial.println("Enter Register address:");
String d=Serial.readString();
Serial.println(d);
Serial.println("\n");
long x=ASCIItoHEX(d);
ReadOrWrite();
DataFormat();
ByteSize();
if (y==0){
if(ds==1)
{
Wire.beginTransmission(0x21);
Wire.write(x);
Wire.endTransmission(false);

Wire.requestFrom(0x21, 1);

if(Wire.available()!=0)
{
b1 = Wire.read();
}
else
{
Serial.println("Wire Not Working");
}
b3 = b1;
}
}
else if(ds == 2)
{
Wire.beginTransmission(0x21);
Wire.write(x);
Wire.endTransmission(false);

Wire.requestFrom(0x21, 2);

if(Wire.available()!=0)
{
b1 = Wire.read();
b2 = Wire.read();
Serial.println("Wire working");
}
}
}
}

```

```

        }
    }

    else
    {
        Serial.println("Wire Not Working");
    }
    b3 = (b2 << 8);
    b3 = b3 | b1;
}

if (Data==1)
{
Output=L1itoDEC(b3);
}
else if (Data==2)
{
    Output=L16toDEC(b3);
}
else if(Data==3)
{
    Output=b3;
}
else if(Data==4)
{
    Output=b3;
}

Serial.println("Stored Value=");
    Serial.print(Output);
}
else
{
    Serial.println("Enter Value to be written:");
    delay(5000);
    i=Serial.readString();
}

double a=ASCIItoFLOAT(i);
Serial.print(a);
if (Data==1)
{
    Input=DECtoL11(a);
}
else if(Data==2)
{
    Input=DECtoL16(a);
}
else if(Data==3)
{
    Input=a;
}
else if(Data==4)
{
}

Wire.beginTransmission(0x21);
Wire.write(x);
Wire.write(Input);
Wire.endTransmission();

}

void ReadOrWrite()
{
Serial.println("Enter 0 for Read or 1 for Write:");
delay(5000);
r=Serial.readString();
y=ASCIItoHEX(r);
Serial.println(y);

}

void DataFormat()
{
Serial.println("Enter data format(1 for L11, 2 for L16, 3 for REG, 4 for Integer Word:");
delay(5000);
Data = Serial.read();
Data = Data - 48;
Serial.println(Data);
}

void ByteSize()
{
Serial.println("Enter expected data byte size(1 or 2):");
delay(5000);
r=Serial.readString();
ds=ASCIItoHEX(r);
Serial.println(ds);
}

int ASCIItoHEX(String str1)
{
char c[4];
str1.toCharArray(c,sizeof(c));
int x;
char *endptr;
x = strtol(c, &endptr, 16);
return x;
}

float L16toDEC(unsigned long a){
float Output=a/4096.0;
return Output;
}

float L11toDEC(unsigned long b3){
    b3 = b3 - 4294901760;
    b4 = b3>>11;
    b5 = (~b4)+1;
    b5 = b5 - 224;
    b6 = b3 & 2047;
    realvall11 = b6;
    for(int i = 0; i<b5; i++)
    {
        realvall11 = realvall11/2.0;
    }
    return realvall11;
}

float DECtoL16(float Input1){
    signed long g =Input1*4096.0;
    return g;
}

long DECtoL11(float input_val)
{
/*
 * Convert a floating point value into a
 * LinearFloat5_11 formatted word
 */
// set exponent to -16
int exponent = -16;
// extract mantissa from input value
int mantissa = (int)(input_val / pow(2.0, exponent));
// Search for an exponent that produces
// a valid 11-bit mantissa
do
{
}

```

```
if((mantissa >= -1024) &&
(mantissa <= +1023))
{
break; // stop if mantissa valid
}
exponent++;
mantissa = (int)(input_val / pow(2.0, exponent));
} while (exponent < +15);

// Format the exponent of the L11
long uExponent = exponent << 11;
// Format the mantissa of the L11
long uMantissa = mantissa & 0x07FF;
// Compute value as exponent | mantissa
return uExponent | uMantissa;
}

float ASCIItoFLOAT(String hstr)
{
    float r=hstr.toFloat();
    return r;
}
```