```
module shiftreg(
   input [7:0] R,
   input L, E, W, clock,
   output reg [7:0] q
);
   integer k;
   always @(posedge clock) begin
      if (L)
         q <= R;
      else if (E) begin
         for (k = 7; k > 0; k = k - 1)
            q[k-1] <= q[k];
         q[7] <= W;
      end
   end
endmodule
```