Embedded Systems

PAGE NO.
DATE : / /

44-pages. PPT.

Embedded Hardware :

↳ Hardware building blocks.

- Board buses ↔ Buses : connect components
  control signal : clk, data signal.
- Bridges : connect buses.

Buses

Types
- System: (main) (local, processor) (main memory — cache), (short, high custom)
- backplane : (memory – master process – I/O). — faster.
- I/O : (expansion, external, host), PCI, USB
  longer & slower SCSI

Diff. b/w system / I/O buss

- nor
  - ↳ IRQ (interrupt req) signal.
    ↓
    indicate master processor using signal,
    ISA bus — unique IRQ.
    PCI → two or more I/O with same IRQ.

- Expandable : PCMCIA, PCI, IDE, SCSI, USB (addition comp. can be plugged)
  - ↓
    - expensive
    - flexible
    - too much – bad poor design.
- non-expandable : DIB, VME, I2C. (X)

Bus arbitration - Give access for bus to board device

↓

Devices

- Master — initiate bus trans. (Master process)
- Slave — respond to master request. (else other compon)

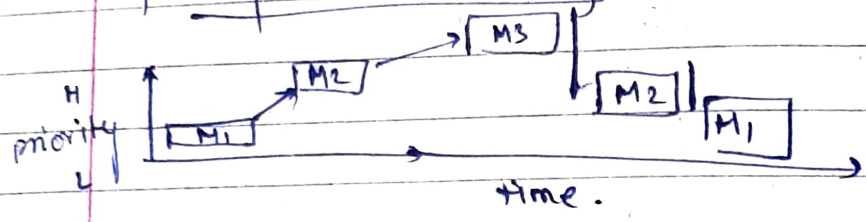
one master — No arbitration,
multiple —"— — decide by arbitrator

→ simple scheme.

Bus Arbitra. Schemes
→ Dynamic Central ⇒ (centrally located)
→ centralized-serialised / daisy-chained
→ destributed self-selection.

master → bus (centrally connect)
master → {queue}
bus → FIFO/priority.
(Starving due to front master)

priority based arbitraty



(2) Arbr. ⇒ masters → in serial.

(3) no cenral / no addition circuitry.
· master arbitrator · assing bus themselve by priority.

Two transaction
READ (recive)
WRITE (transmit)

Atomically: finished its transmiss.
split: preemt. in middle.

Bus timings:

Synch.
- includ clock signal among other signal.
- same clock rate with bus.

Asynchronaly.
- no clock signal.
- other "hand shaking" signal
- length, longer nuber of comp. — no possible for syn. comm
- bcz clock is not basis.
- need some other sync.

Transferring mode :

PAGE NO. icon
DATE : / /

Single → every word trans. of data. (good)

Blocked → address transmit only once for multiple words
→ increase bandwidth / burst transfer
→ use in cache transaction scheme. memory transaction (not good)

Bus Performance

↳ Bandwidth : amt of data/time
↳ Design - Impact.

multiplex - demultiple cause delays.

→ bus width : # data in given bus cycle. {serial → 1-bit any one time}

32-bit data. & bus-width 8-bit → 4-times

→ Delay - wait state ↑ — # of data pack ↑ ∝ 1/bus width ∝ 1/bandwidth

→ split trans → common sol for

Board I/O

Input comp. → Ip device —info→ master proc } through memory
Out comp → Master —info→ o/p

(6) type.

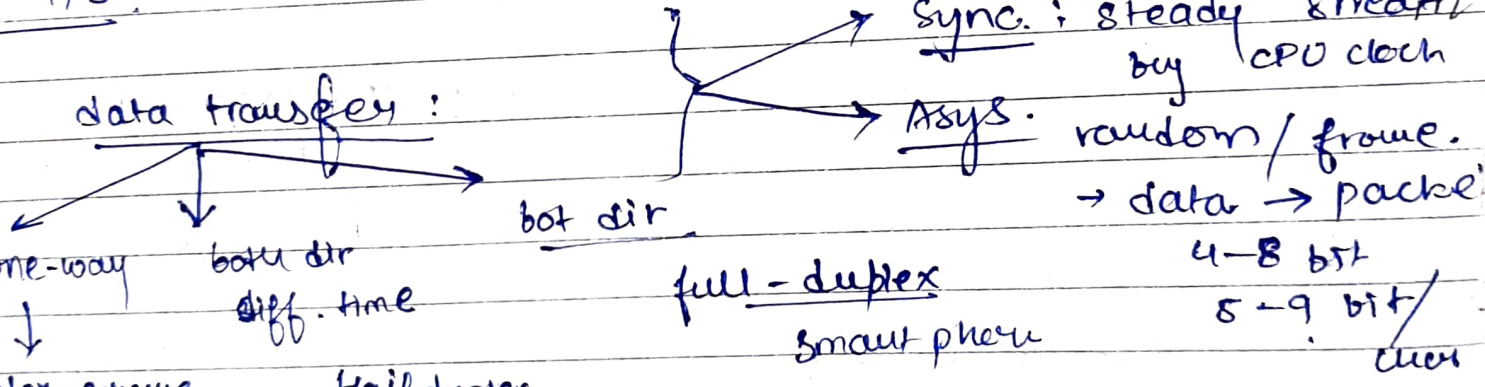
Debugging : BDM, JTAG
- realtime : timer / counter
- Storage : disk controller

- network - osi physical
- Input
- Graphic

I/O hardware

6 - Logical unit
- Transmission media, [redacted], Comm. port, comm interface
I/O control, I/O buses, master processor integrate I/O

Serial I/O:



Software :

⇒ Memory device Drivers

6- functions ⇒ memory subsystem

startup, shut down, disable, enable, write, read
hardware. cache. ROM, main mem

Byte ordering

scheme for retrive and store bit.

Big endian — lower-byte add — MSB (left) — 1st

little endian — lower byte — LSB (Right) — 0th.

⇒ On-board bus device Drives.

Bus protocol — 10-funct:

6-of above + Require, release, install, unistall.
buses buses

I2C initializing of bus.

I2C pins (SDL, SCL)

on MPC860 I2C Registers
I2C Parameter Ram.
I2C buffer descriptors.

Bit rate → # bits / time (1 sec)

Baud rate → # signal unit / 1 sec

$$\frac{\text{Bit rate}}{\text{Baud rate}} = \frac{\#\text{ actual data bit per frame}}{\text{total \# of bit per frame}}$$

Serial Interface → slave ICs on ~~board~~ ~~of~~

single bit

- Asyn trasfer
  - ✓ start, stop bit, parity.
  - diff clock of trans. & recever.
- Sync transfer:
  - × start, stop bit UART, SPI

I/O ← Transmitt data — serial port → I/O.

master CPU — convert data serial → master CPU.

Parallel I/O ~~Interface~~

multiple bit

greater capacity., CRT, SCSI

parallel port, parall. interu

I/O. Component Interfacin

- on-board — direct master — I/O dev (I/O ports)
- off-board — indirect — comm interface — comm boar port

~~greater~~

performance — Throughput: max data / time can process (1) sec (bytes)

- execution time & response time (req recie. & actual start) — write data of I/O comp.
- Benchmark — performance analyze.

Device drivers:

→ IO function for hardware

Application soft laye.
System soft layer → middle la — OS.
Device driver layer
Hardware layer → master proce.

Arch-sepcific + master proce

generic — hardware on not integrated

States: Inactive, Finish, Busy

Device Driver layer

Higher-layer interface — Hi —//—

Hardware interface —//—

Software modes : Supervisory and user mode

Interrupt Handling

signal triggered by some event during the exec of an instruction stream by master process.

asyn — sym.

↓ start process of interrupt hand

ISR — IVJ

5-Steps

→ stop process
→ Save prog count stat
→ Run ISR
→ restore prog cou
→ Resum

4-fuct + 1-fun
start — end dis start — intrs
servicing
often interrupt main exe stream

3-types of intr

Soft — explicitly by some instr within curr instr — overflow /0 — traps

hardw — int. / ext — hardware other than master cpu — Interrupt (priority base)

triggered — Level : IRQ is (H/L) — change on IRQ lines

another
→ 1-priority — Highest priority — non-maskable (NMI)
→ low-priority → masked

PAGE NO. icon
DATE : / /

context switching

by master processor ccuu ⟶ another set of instr

- vector: PC contain staust of ISR
- non-vector: VT → add. of ISR

Intrupt latency : (ISR staute eae.)

(intrupt triggured)