NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Cycle Test 2: CSPC61 - Embedded Systems Architectures

Semester: VI
Maximum Marks: 20
Duration: 1 Hour

Section: A & B
Date : 06.04.2022
Time: 10.00 am to 11.00 am

ANSWER ALL THE QUESTIONS

Note: Some MCQs may have multiple answers. In such cases, you are expected to write all the correct choices. Otherwise, no mark will be provided for that question.

1. Match the following *(4*0.25=1 Mark)* 3, 1, 4, 2

A. M37267M8 Microcontroller - 1. Auto vectored interrupt scheme
B. Non vectored interrupt - 2. Synchronous serial transmission
C. I/O Bus - 3. Internal circuitry for Interrupt transactions
D. Serial peripheral interface - 4. Interrupt request control signals

2. The parallel communication interface is responsible for _____ of receiving data being transmitted from the master CPU onto the parallel port pins and _____ of data bits transmitted from the Input device. *(2*0.5=1 Mark)* Encoding , Decoding.

3. Find odd one out in terms of Board Buses. *(1 Mark)*

A. Personal Computer Memory Card International Association Bus interface
B. Non Expandable Integrated Drive Electronics (IDE) Bus
C. Versa Modular Eurocard (VME) Bus
D. Small Computer System Interface Bus

4. _____ form the following(s) is/are true about the embedded hardware building blocks? *(1 Mark)*

A. Dynamic central parallel arbitration is one of the bus arbitration schemes in which arbitrator are connected to all masters.
B. In synchronous data transmission, separate clocks is not used by the serial interface of transmitter and receiver circuits.
C. In synchronous data transmission, the state of the communication channel between the transmissions of frames is being a non-return to zero.
D. In a full duplex communication scheme, the data stream can be transmitted and received in either direction simultaneously.

5. In embedded hardware building blocks, we are the components used to provide ability to the master CPU in configuring and monitoring the I/O Controller. And the Master CPU uses us to communicate and/or control the connected I/O devices via the I/O controller. Find out who are we? *(1 Mark)* control + Status registers,

6. Blocked data transferring mode (burst data transfer scheme) schemes are used in ____ memory transaction. *(0.5 Mark)* cache,

7. _____ or _____ is used to synchronize slower I/O devices with the high speed master CPU and _____ is used to synchronize I/O devices with the master CPU when the I/O devices have higher speed than the master CPU. *(1.5 Marks)* Status flag, interrupts, DMA

8. The baud rate is ____ *(1 Mark)*

A. the bandwidth of the serial interface.
B. the total number of bits that can be transmitted.
✓ C. the total number of bits per unit time that can be transmitted.
D. None of the above.

9. Which of the following combination of device driver function is correct when a hardware in an Inactive state. *(1 Mark)*

A. Hardware startup, enable, read
B. Hardware read, acquire write
C. Hardware startup, release, disable, shutdown
✓ D. Hardware startup, install, enable

10. Match the following *(4*0.25=1 Mark)*

A. Execution mode of device driver - 1. Hardware interrupt
B. Divide by zero trap - 2. Address of the ISR
C. Interrupt vector table - 3. Edge triggered interrupts
D. Very short or very long Interrupt signals - 4. Supervisory

4, 1, 2, 3

11. Identify the correct option for the given assertion and reason. *(1 Mark)*

Assertion: Device drivers are categorized in two ways. They may be either architecture-specific or generic. Though generic device driver manages hardware that is located on the board and not integrated onto the master processor, it has architecture-specific source code parts in it.

Reason: Because the I/O controller is the primary control unit and has access to

everything on the board, there are usually architecture-specific parts of source code in a generic driver.

A. Assertion and reason, both are true

B. Assertion and reason are false

C. Assertion is true and reason is false

D. Assertion and reason are true, but this is not the correct reason for the given assertion

12. Consider asynchronous transmission is happening in an embedded system. Three serial interfaces are involved in the data transmission. Assume that serial interface1 works in the bit rate 512Kbps, serial interface2 has 1024Mbps bit rate and serial interface3 at 256Mbps. Find out what is the minimum data rate can be expected from this transmission *(1 Mark)*. Justify your answer with explanation. *(1 Mark)*

13. Consider we have an embedded system where the serial interface at the transmitter divides the data stream into packets and encapsulated as frames with 1 start and 1 stop bit. Assume that the number of bits per character is 30. Find out the number of characters per second can be transmitted through asynchronous and synchronous serial lines with 4800bps baud rate. *(2 Marks)*

14. Write pseudocode for I^2C buffer descriptor Initialization in the implementation of on-board bus device driver. Consider you need to initialize two reception buffer and one transmission buffer in the initialization of I^2C buffer descriptor. *(3 Marks)*

15. With neat block diagrams *(1 Mark)*, list down the four differences *(1 Mark)* between Monolithic OS and Microkernel-based OS.

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