Basic Arithmetic and Logic Unit Specification

ALU 1.0

Design Type:
- Clocked Basic Arithmetic Logic Unit (ALU)

Reset Mechanism:
- Active High reset
- Reset is triggered when the reset signal is set to 1

Data Handling:
- Input data is applied on the current cycle
- ALU produces output on the subsequent cycle

Transaction Support:
- Does not support back-to-back transactions

Supported Operations:
- ADD (Addition)
- SUB (Subtraction)
- MULT (Multiplication)
- DIV (Division)

Input Constraint:
- Input A must always be greater than or equal to Input B

Port Name	Type	Property	Size
Clock	Input	Wire	1 bit
Reset	Input	Wire	1 bit
A	Input	Wire	8 bits
B	Input	Wire	8 bits
ALU_Sel	Input	Wire	4 bits
ALU_Out	Output	Reg	8 bits
CarryOut	Output	Bit	1 bit

ALU_Sel	Operation
4'b0000	A + B
4'b0001	A - B
4'b0010	A * B
4'b0011	A / B
4'b0100 – 4'b1111	Reserved