Features

- I2C-bus to 16-bit GPIO expander
- Operating power supply voltage from 1.65 V to 5.5 V
- Low standby current consumption:
  - 3.0 μA (typical at 5 V V_{CC})
  - 1.5 μA (typical at 3.3 V V_{CC})
- 400 kHz Fast-mode I2C-bus
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output (INT)
- Configurable Slave Address with 3 Address Pins
- Internal power-on reset
- Power-up with all channels configured as inputs with weak pull-up resistors
- Latch-Up performance exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 4000-V Human Body Model
  - 1500-V Charged Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers

Description

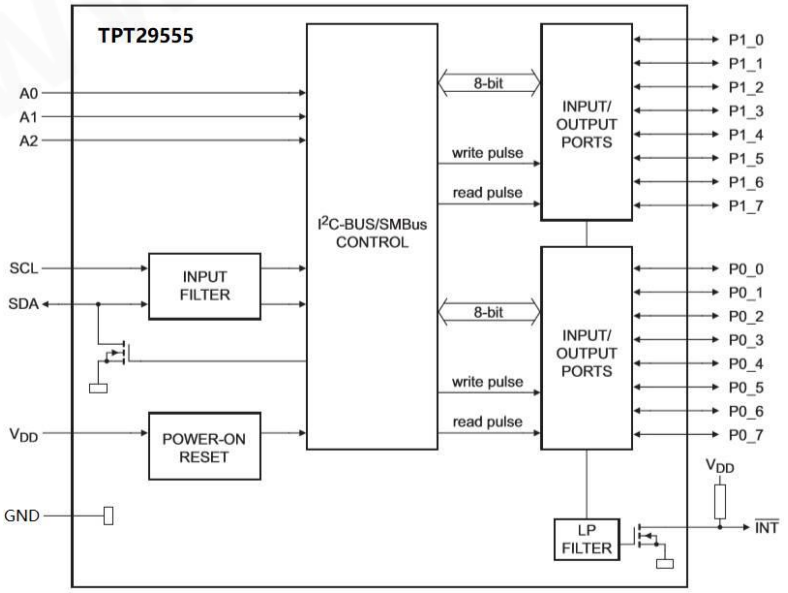
The TPT29555 is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I2C-bus applications. The power supplier voltage range is from 1.65 V to 5.5 V that allows the TPT29555 to interconnect with 1.8-V microcontrollers.

The TPT29555 contains the register set of two pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers. The open-drain interrupt (INT) output is changeable when any input state changes from its related register state and is used to indicate the system master that an input state has changed. INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I2C-bus. Thus, the TPT29555 can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have internal weak pull-up resistors to remove external components. Three hardware pins (A0, A1, A2) select the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus.

TPT29555 is available in TSSOP24 and QFN24 package, and is characterized from −40°C to +85°C.

Function Block Diagram



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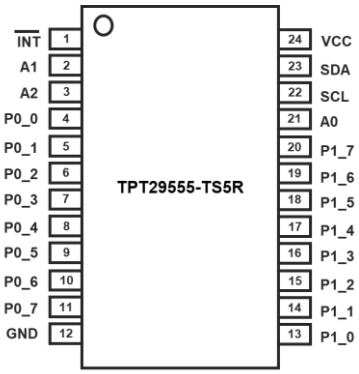
Revision History

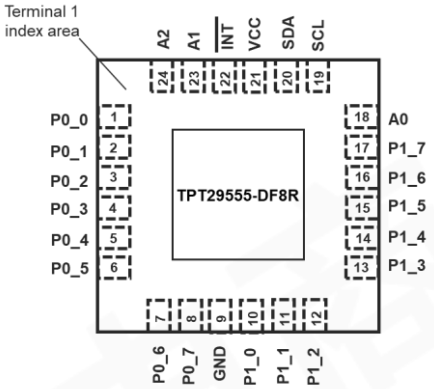
Date	Revision	Notes
2020-06-12	Rev.Pre.0	Initial Version
2020-11-20	Rev.Pre.1	Added electrical data
2021-01-18	Rev.Pre.2	Updated TSSOP24 package information
2021-03-12	Rev.Pre.3	Added register description
2021-06-15	Rev.A.0	First release version
2021-12-14	Rev.A.1	Added Standard mode timing requirements
2022-1-20	Rev.A.1.1	Fix the typo of ICC unit in page1
2022-1-29	Rev.A.1.2	Fix the typo of pin function and outline of QFN package

Pin Configuration and Functions

TSSOP24 Package
Top View



QFN4X4-24 Package
Top View



Pin Functions

Pin			I/O	Description
Name	TSSOP24	QFN4X4-24		
A0	21	18	Input	Address input 0. Connect directly to VCC or ground
A1	2	23	Input	Address input 1. Connect directly to VCC or ground
A2	3	24	Input	Address input 2. Connect directly to VCC or ground
GND	12	9	GND	Ground
$\overline{INT}$	1	22	Output	Interrupt output. Connect to VCC through a pull-up resistor
P00	4	1	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01	5	2	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02	6	3	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03	7	4	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04	8	5	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05	9	6	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06	10	7	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07	11	8	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
P10	13	10	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input

Pin Functions (Continued)

Pin			I/O	Description
Name	TSSOP24	QFN4X4-24		
P11	14	11	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12	15	12	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13	16	13	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14	17	14	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15	18	15	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16	19	16	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17	20	17	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
SCL	22	19	Input	Serial clock bus. Connect to VCC through a pull-up resistor
SDA	23	20	Input	Serial data bus. Connect to VCC through a pull-up resistor
VCC	24	21	Supply	Supply voltage

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{CC}	Supply voltage	−0.5	6	V
V_I	Input voltage	−0.5	6	V
V_O	Output voltage	−0.5	6	V
I_{IK}	Input clamp current, $V_I < 0$		−20	mA
I_{OK}	Output clamp current, $V_O < 0$		−20	mA
I_{IOK}	Input-output clamp current, $V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current, $V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current, $V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND		−250	mA
	Continuous current through V_{CC}		160	mA
T_J	Maximum Junction Temperature		125	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	V_{CC}	V
		A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	$0.7 \times V_{CC}$	5.5	V
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	mV
		A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	−0.5	$0.3 \times V_{CC}$	mV
I_{OH}	High-level output current	P0_7 ~ P0_0, P1_7 ~ P1_0		−10	mA
I_{OL}	Low-level output current	P0_7 ~ P0_0, P1_7 ~ P1_0		25	mA
		$\overline{INT}$, SDA		6	mA
T_A	Operating Temperature Range		−40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	68	21	°C/W
QFN24	60	25	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 1.65 V ~ 5.5 V, T_A = −40°C ~ +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V_{POR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND; I_O = 0 mA		1.25	1.45	V
	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND; I_O = 0 mA	0.8	1.2		V
I_{OL}	LOW-level output current, SDA	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V	3			mA
	LOW-level output current, INT	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V	3			mA
	LOW-level output current, P port	V_{OL} = 0.5 V; V_{CC} = 1.65 V	8			mA
		V_{OL} = 0.5 V; V_{CC} = 2.3 V	8			mA
		V_{OL} = 0.5 V; V_{CC} = 3.0 V	8			mA
		V_{OL} = 0.5 V; V_{CC} = 4.5 V	8			mA
	LOW-level output current, P port	V_{OL} = 0.7 V; V_{CC} = 1.65 V	10			mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V	10			mA
		V_{OL} = 0.7 V; V_{CC} = 3.0 V	10			mA
		V_{OL} = 0.7 V; V_{CC} = 4.5 V	10			mA
V_{OH}	HIGH-level output voltage, P port	I_{OH} = -8 mA; V_{CC} = 1.65 V	1.2			V
		I_{OH} = -8 mA; V_{CC} = 2.3 V	1.8			V
		I_{OH} = -8 mA; V_{CC} = 3.0 V	2.6			V
		I_{OH} = -8 mA; V_{CC} = 4.75 V	4.1			V
	HIGH-level output voltage, P port	I_{OH} = -10 mA; V_{CC} = 1.65 V	1.0			V
		I_{OH} = -10 mA; V_{CC} = 2.3 V	1.7			V
		I_{OH} = -10 mA; V_{CC} = 3.0 V	2.5			V
		I_{OH} = -10 mA; V_{CC} = 4.75 V	4.0			V
I_I	Input current: A0, A1, A2;	V_{CC} = 1.65 V to 5.5 V, V_I = V_{CC} or GND	−1		1	μA
	Input current: SCL, SDA	V_{CC} = 1.65 V to 5.5 V, V_I = V_{CC} or GND	−1		1	μA
I_{IH}	HIGH-level input current: P port	V_I = VCC; V_{CC} = 1.65 V to 5.5 V			1	μA
I_{IL}	LOW-level input current: P port	V_I = GND; V_{CC} = 1.65 V to 5.5 V			−100	μA

(1) 100% tested at T_A = 25°C.

(2) Parameters are provided by lab bench test and design simulation.

Electrical Characteristics (Continued)

All test conditions: V_{CC} = 1.65 V ~ 5.5 V, T_A = −40°C ~ +85°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Icc	Supply current	Active mode, I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz	V_{CC} = 5.5 V		16	30	μA
			V_{CC} = 3.6 V		9	20	μA
			V_{CC} = 2.7 V		6.2	15	μA
			V_{CC} = 1.95 V		4.2	10	μA
		Standby Mode, input low, I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC} = 5.5 V		0.90	1.5	mA
			V_{CC} = 3.6 V		0.48	1.3	mA
			V_{CC} = 2.7 V		0.43	1.0	mA
			V_{CC} = 1.95 V		0.31	0.9	mA
		Standby Mode, input high, I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC} = 5.5 V		2.64	3.5	μA
			V_{CC} = 3.6 V		1.55	2.3	μA
			V_{CC} = 2.7 V		1.07	1.6	μA
			V_{CC} = 1.95 V		0.68	1.2	μA
C_i	Input capacitance	V_I = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (2)			3		pF
C_{io}	Input/output capacitance	$V_{I/O}$ = V_{CC} or GND; V_D = 1.65 V to 5.5 V (2)			3		pF
		$V_{I/O}$ = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (2)			5		pF

(1) 100% tested at T_A = 25°C.

(2) Parameters are provided by lab bench test and design simulation.

I2C Interface Timing Requirements

Over recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Conditions	Standard Mod		Fast Mode		Unit
			Min	Max	Min	Max	
fscl	I2C clock frequency		0	100	0	400	kHz
tsch	I2C clock high time		4		0.6		μs
tscl	I2C clock low time		4.7		1.3		μs
tsp	I2C spike time			50		50	ns
tsds	I2C serial-data setup time		250		100		ns
tsdh	I2C serial-data hold time		10		10		ns
ticr	I2C input rise time			1000	20	300	ns
ticf	I2C input fall time			300	20 × (V_{CC} / 5.5 V)	300	ns
tocf	I2C output fall time	10-pF to 400-pF bus		300	20 × (V_{CC} / 5.5 V)	300	ns
tbuf	I2C bus free time between stop and start		4.7		1.3		μs
tsts	I2C start or repeated start condition setup		4.7		0.6		μs
tsth	I2C start or repeated start condition hold		4		0.6		μs
tsps	I2C stop condition setup		4		0.6		μs
tvd(data)	Valid data time	SCL low to SDA output valid		3.5		0.9	μs
tvd(ack)	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
Cb	I2C bus capacitive load			400		400	pF

Parameter measurement waveforms

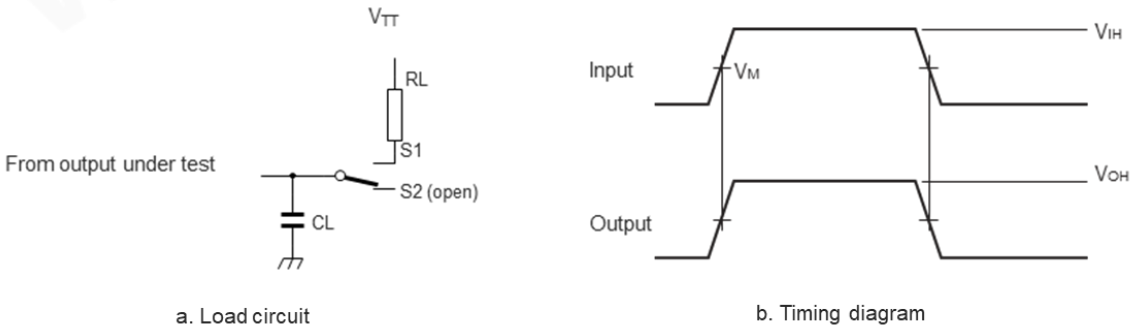


Figure 1 Load Circuit for Outputs

Switching Characteristics

Over recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	From (Input)	To (Output)	Standard Mod		Fast Mode		Unit
				Min	Max	Min	Max	
tiv	Interrupt valid time	P port	INT		4		4	μs
tir	Interrupt reset delay time	SCL	INT		4		4	μs
tpv	Output data valid; For V_{CC} = 2.3 V–5.5 V	SCL	P port		400		400	ns
	Output data valid; For V_{CC} = 1.65 V–2.3 V				400		400	ns
tps	Input data setup time	P port	SCL	15		15		ns
tph	Input data hold time	P port	SCL	1		1		μs

Typical Performance Characteristics

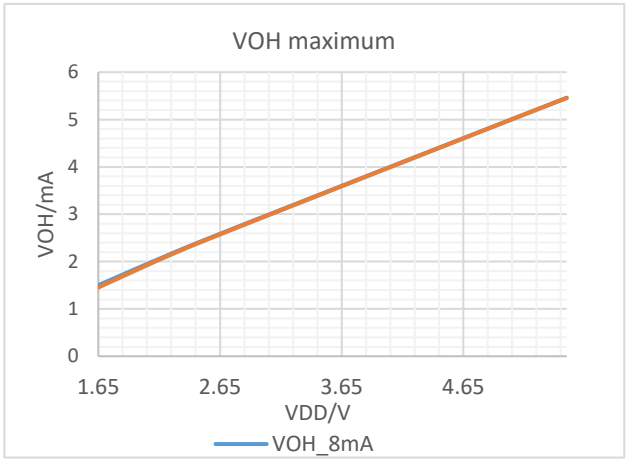


Figure 2 Voh maximum measurement

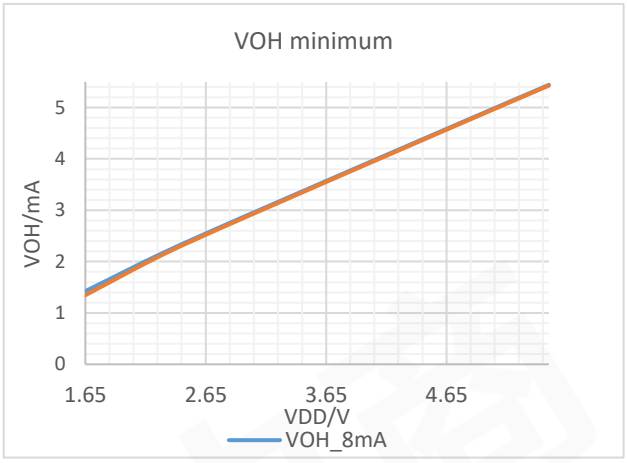


Figure 3 Voh minimum measurement

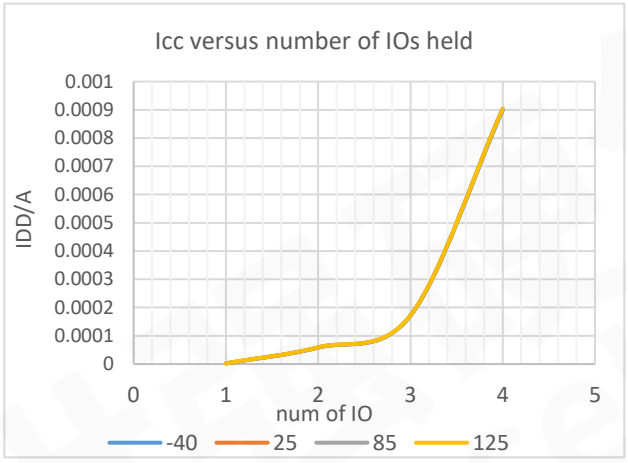


Figure 4 Icc versus number of IOS measurement

Detailed Description

Overview

The TPT29555 is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I2C-bus applications. The power supplier voltage range is 1.65 V to 5.5 V and allows the TPT29555 to interconnect with 1.8 V microcontrollers.

Function Block Diagram

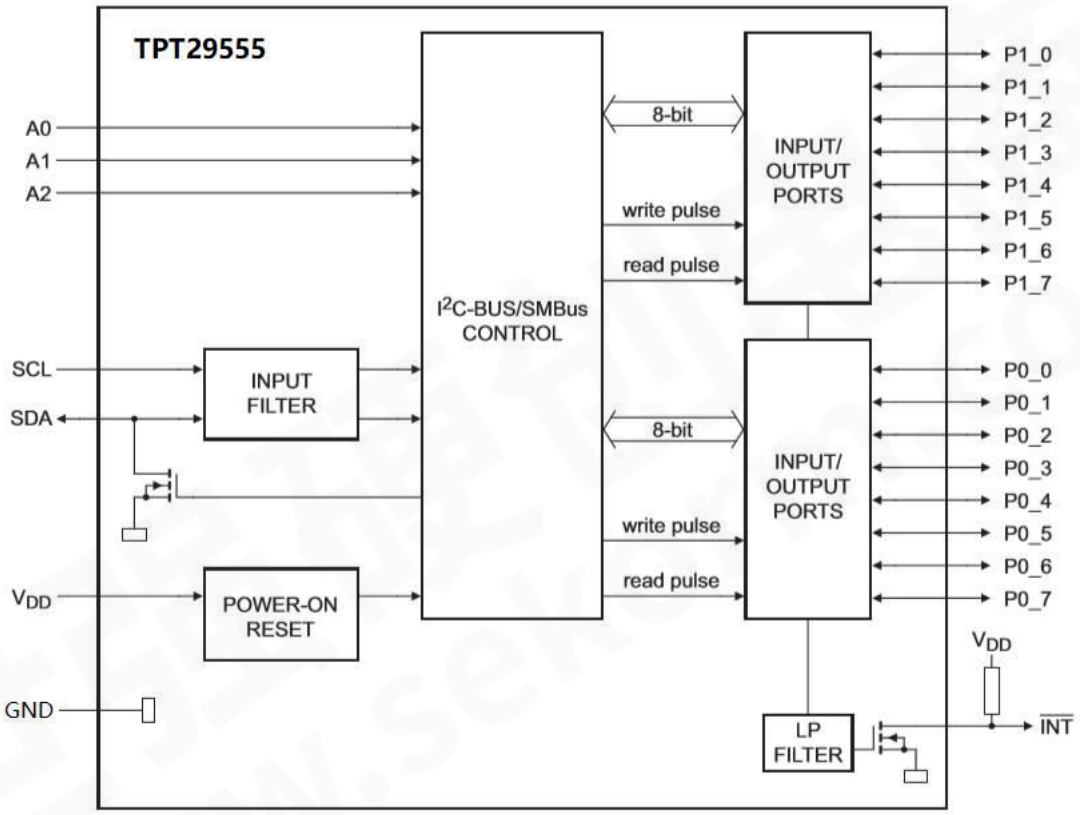


Figure 5 Function Block Diagram

Feature Description

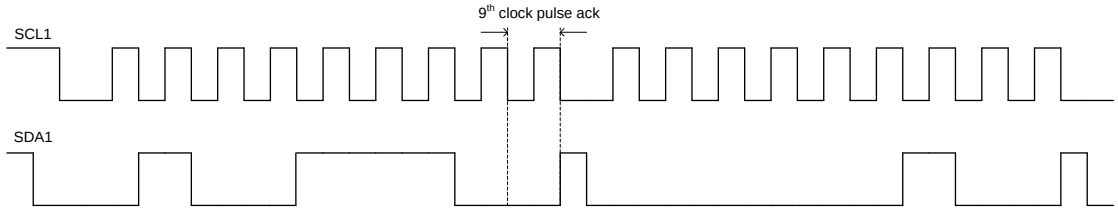


Figure 6 I2C BUS (1.65 V ~ 5.5 V) waveform

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. All input/output pins have internal weak pull-up resistors to remove external components. Three hardware pins (A0, A1, A2) select the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus. To conserve power, address pins (A0, A1, A2) must be pulled HIGH or LOW. The address of the TPT29555 is shown as below.

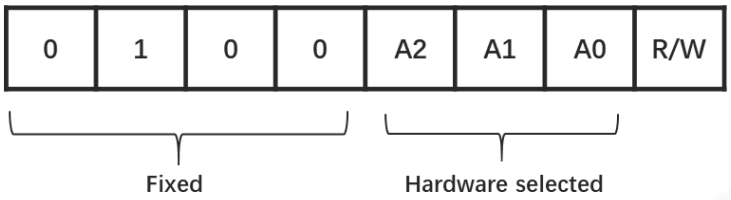


Figure 7 Slave Device Address

Control Register

Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 1 Command Byte Description

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

Register 0 and 1: Input port registers

This register is an input-only port, which means the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3（output port 1）,and writes to this register have no effect. The default value 'X' is determined by the externally logic level.

Table 2 Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 3 Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Register 2 and 3: Output port registers

This register is an output-only port, which means the outcoming logic levels of the pins defined as outputs by Register 6 (Configuration port 0) and 7 (Configuration port 1). Bit values in this register have no effect on pins defined as inputs. In fact, the value reading from this register is in the flip-flop controlling the output selection, not the actual pin value.

Table 4 Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 5 Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Register 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with '0'), the input port data polarity is retained.

Table 6 Polarity Inversion port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 7 Polarity Inversion port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to V_{DD} at each pin. At reset, the device's ports are inputs with a pull-up to V_{DD}.

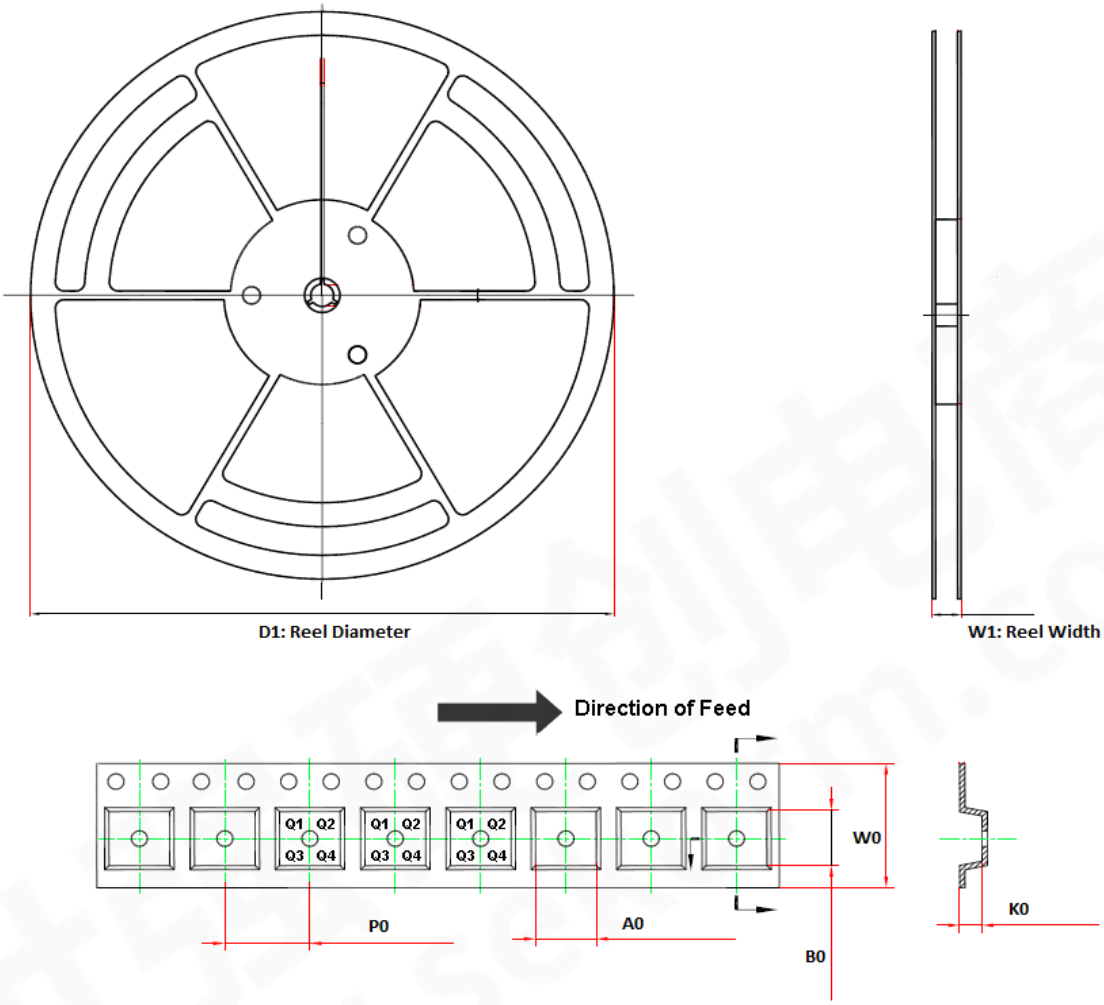
Table 8 Configuration port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 9 Configuration port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

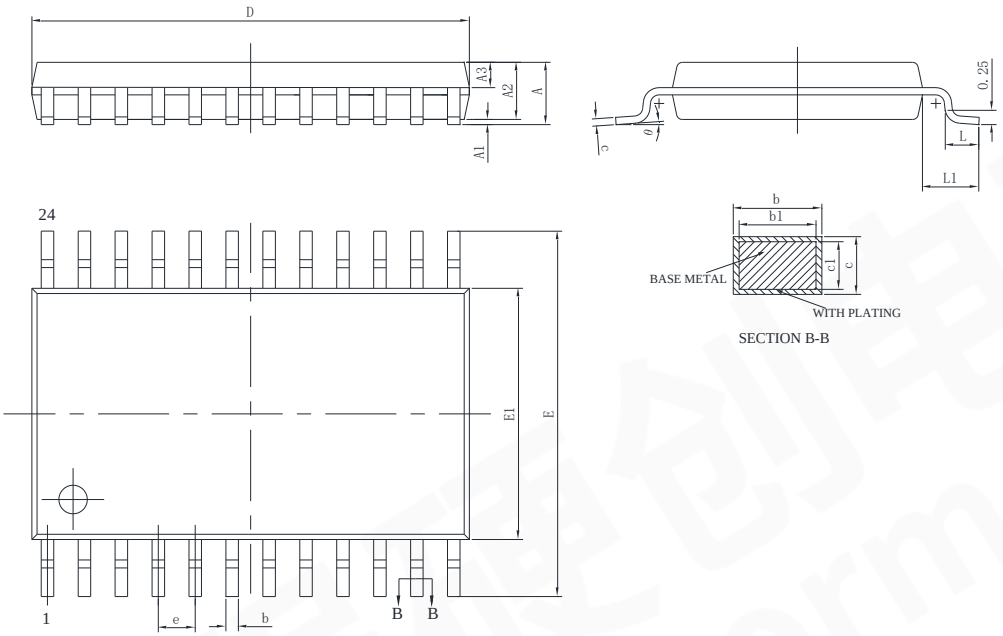
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29555-TS5R	24-Pin TSSOP	330	22.4	6.8	8.3	1.6	8	16	Q1
TPT29555-QF8R	24-Pin QFN	330	17.6	4.3	4.3	1.1	8	12	Q1

Package Outline Dimensions

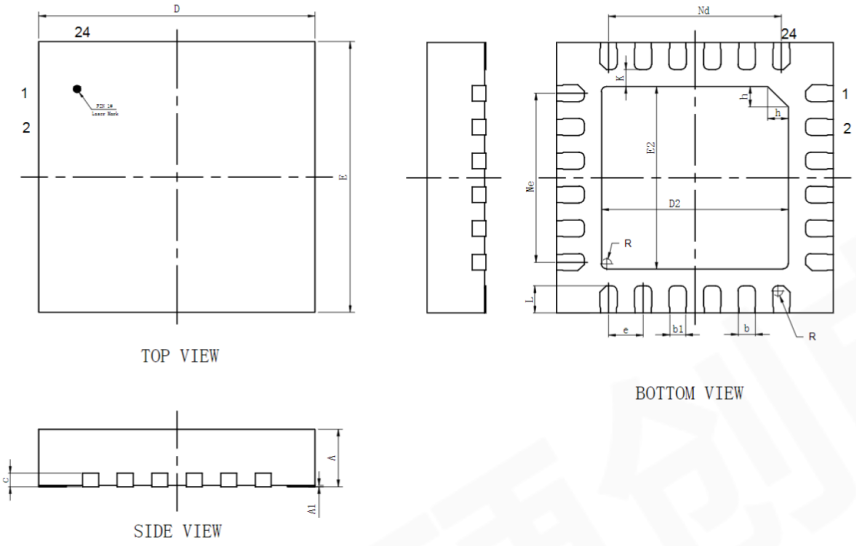
TS5R (TSSOP24)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Package Outline Dimensions

QF8R (QFN4X4-24L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.23REF	
c		0.203REF	
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
e		0.50BSC	
Nd		2.50BSC	
Ne		2.50BSC	
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
h	0.25	0.30	0.35
K		0.25REF	
R		0.075REF	

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29555-TS5R	−40 to 85°C	24-Pin TSSOP	29555	MSL3	4,000	Green
TPT29555-QF8R	−40 to 85°C	24-Pin QFN	29555	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.