

RAMA KRISHNA KETHA

Palacole, Andhra Pradesh, India



ramasketha14093@gmail.com



8466084225



linkedin.com/in/rama-krishna-ketha-aa17751b9



https://github.com/RAMA-L7

Objective

Seeking an exciting and challenging entry level position in the company which motivates me to do my best and improve my skills. Where my contribution helps to achieve company's mission and organization goals.

Education



Swarnandhra College of Engineering & Technology, Narasapur. PIN -534275 (CC-A2)

Bachelor of Technology - BTech, Electronics and Communications Engineering

2020 – 2023 — **7.40 CGPA**



Smt.b. Seetha Polytechnic Collage

Diploma of Education, Electronics and Communications Engineering

2014 – 2019 — **63.74%**



Z.P.P. High School

SSC

2014 — **8.5 CGPA**

Technical Skills

- Strong knowledge of physical design principles
- Hands-on experience with PNR flow using ICC
- Good understanding of ASIC design flow from gate-level netlist to GDSII
- Proficient in floorplanning, power planning, placement, CTS, and routing
- Skilled in identifying and resolving PnR process issues
- Familiar with various EDA tools for physical design
- Committed to continuous learning in physical design and PnR techniques

Experience

DPI INDIA SERVICES PVT Ltd., Bangalore, Karnataka.

-September 2023 to till date

Tools

- VLSI CAD Tool: ICC1

Project

- **Project:** ORCA TOP
- **Technology node:** 28nm
- **Tool:** ICC
- **Design Specifications:**
 - Number of metal layers: 9
 - Voltage: 1.1V
 - Frequency: 416.6 MHz
 - Number of macros: 40
 - Shape: Rectangular
 - Clock count: 5

Challenges

- **Power Grid Design:** Identified and resolved power plan shorts that caused unintended electrical connections, leading to potential design failures.
- **Placement Congestion:** Utilized magnetic placement techniques to address congestion, optimizing cell positions to improve routing efficiency and avoid overcrowded areas.
- **Clock Tree Delay Variability:** Managed clock tree delay variability by analyzing and optimizing the levels of logic used in clock distribution to ensure uniform signal distribution and minimize skew.
- **Routing Congestion:** Addressed routing congestion in high-density areas by optimizing path routing and ensuring efficient use of all available metal layers to avoid blockages and maintain signal integrity.

Key Strengths

- Logical and Structured Thinking.
- Adaptability.
- Strong passion for gaining knowledge and understanding
- Good Listener.

Declaration

I hereby declare that all the information above mentioned is true to the best of my knowledge.

Place:

Date:

(Rama Krishna Ketha)

