Computer Organization & Architecture

Chapter 5 – CISC-Style Processors

Zhang Yang 张杨

cszyang@scut.edu.cn

Autumn 2021

Content of this lecture

- 5.7 CISC-Style Processors
- Homework

CISC-Style Processors (1)

- CISC-style processors have more complex instructions.
- The full collection of instructions cannot all be implemented in a fixed number of steps.
- Execution steps for different instructions do not all follow a prescribed sequence of actions.
- Hardware organization should therefore enable a flexible flow of data and actions to accommodate CISC.

CISC-Style Processors (2)

- Hardware Organization of A CISC-Style Processor

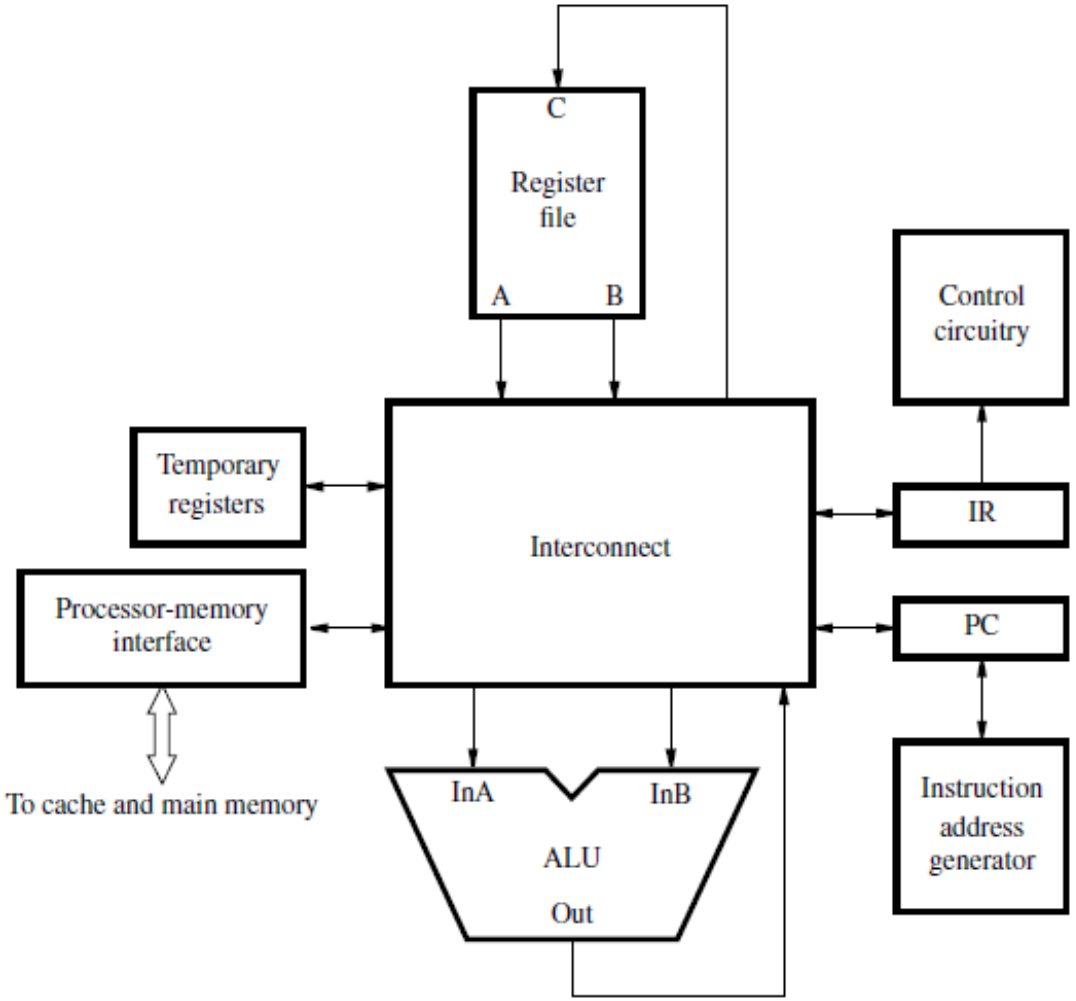

Figure 5.22 Organization of a CISC-style processor.

CISC-Style Processors (3)

- Hardware Organization of A CISC-Style Processor (ctd.)
  - Interconnect Block
    - Provide interconnections among other blocks
    - It does not prescribe any particular structure or pattern of data flow
    - It provides paths that make it possible to transfer data between any two components, as needed to implement instructions.
  - Temporary Registers Block
    - No inter-stage registers
    - Two temporary registers hold intermediate results during instruction execution
      - Temp1 and Temp2

CISC-Style Processors (4)

- Traditional Implementation of the Interconnect: Bus
- A *bus* consists of a set of lines to which several devices may be connected, enabling data to be transferred from any one device to any other.
- A logic gate that sends a signal over a bus line is called a *bus driver*.
- When functional units are connected to a common bus, tri-state drivers are needed.

CISC-Style Processors (5)

- How a flip-flop that forms one bit of a data register can be connected to a bus line
  - Rin=1, the data on the bus line to be loaded into the flip-flop
  - Rin=0
  - Rout

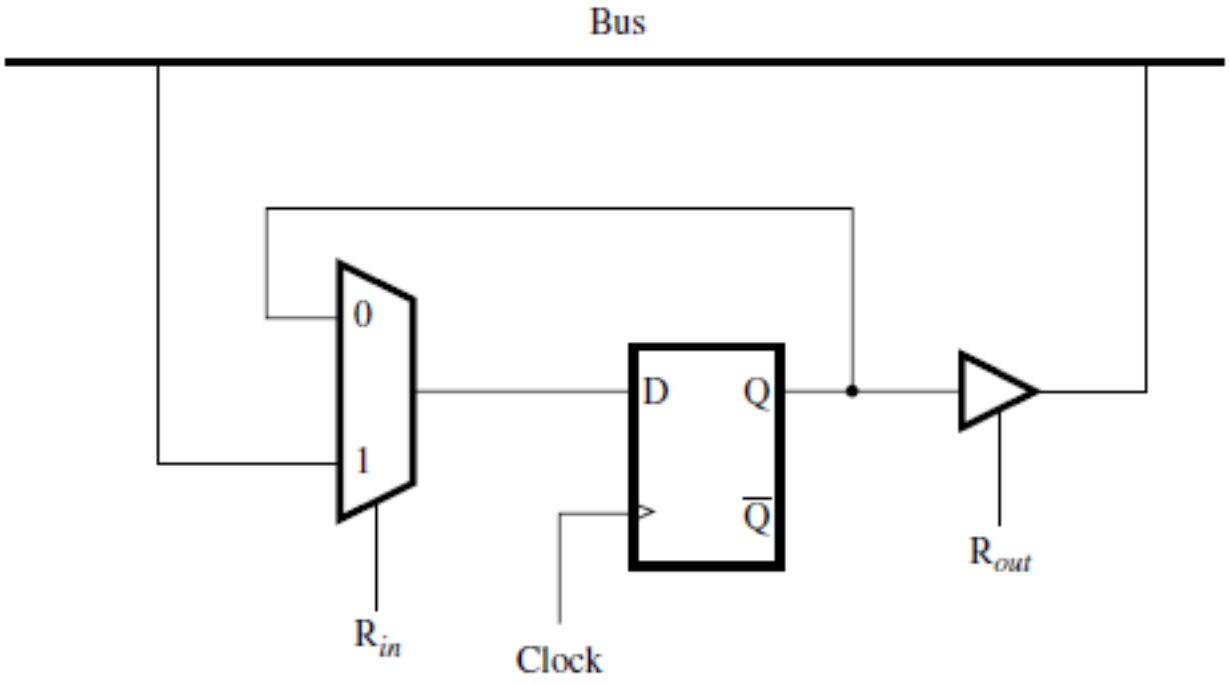

Figure 5.23 Input and output gating for one register bit.

CISC-Style Processors (6)

- An Interconnect Using Three Buses
  - All registers are assumed to be edge-triggered
    - When a register is enabled, data are loaded into it on the active edge of the clock at the end of the clock period.
  - Addresses for the three ports of the register file are provided by the Control block.
  - These connections are not shown to keep the figure simple.
  - Also not shown is the Immediate block through which the IR is connected to bus B.

CISC-Style Processors (7)

- An Interconnect Using Three Buses (ctd.)

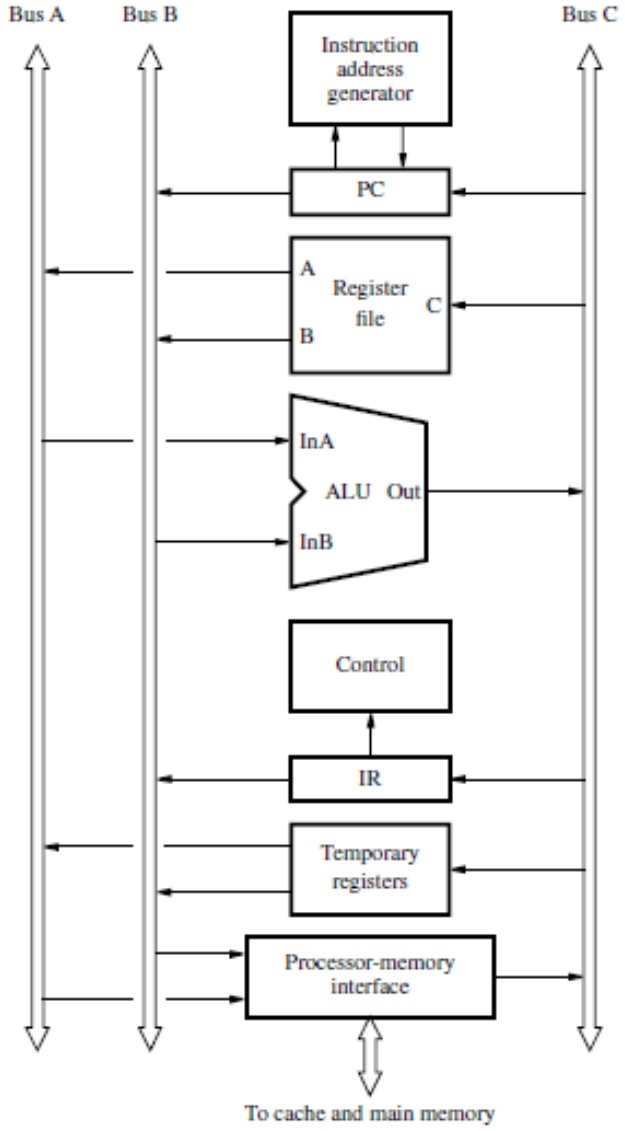

Figure 5.24 Three-bus CISC-style processor organization.

CISC-Style Processors (8)

- An Interconnect Using Three Buses (ctd.)
  - Example: Add R5, R6

Step	Action
1	Memory address ← [PC], Read memory, Wait for MFC, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction
3	R5 ← [R5] + [R6]

Figure 5.25 Sequence of actions needed to fetch and execute the instruction: Add R5, R6.

CISC-Style Processors (9)

- An Interconnect Using Three Buses (ctd.)
  - Example: Add R5, R6 (ctd.)

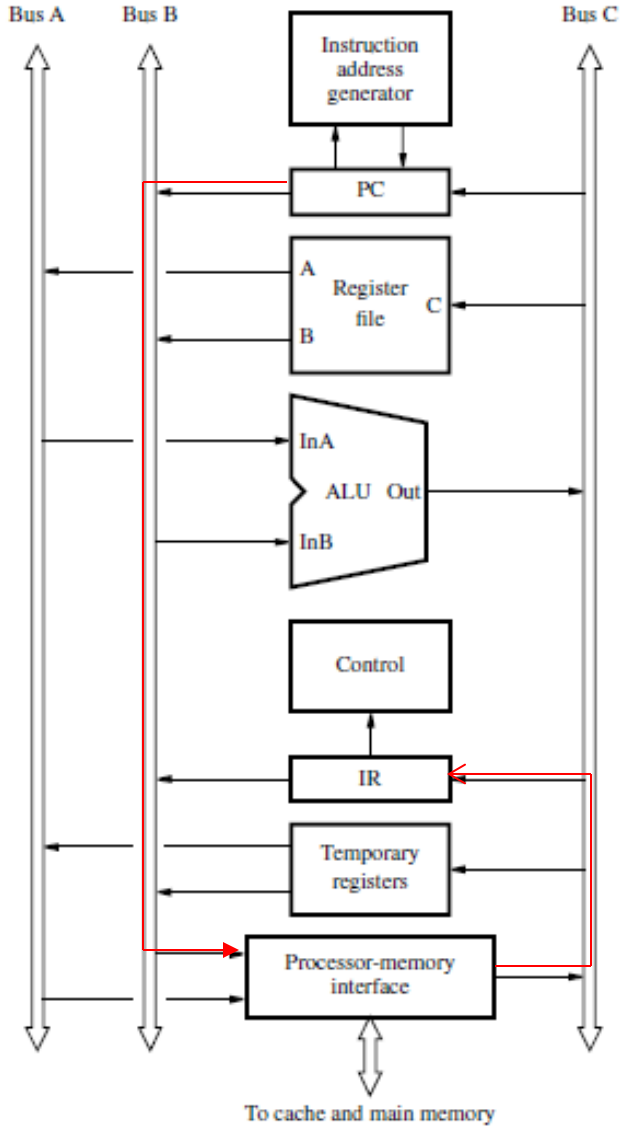

Figure 5.24 Three-bus CISC-style processor organization.

CISC-Style Processors (10)

- An Interconnect Using Three Buses (ctd.)
  - Example: And X(R7), R9

Step	Action
1	Memory address ← [PC], Read memory, Wait for MFC, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction
3	Memory address ← [PC], Read memory, Wait for MFC, Temp1 ← Memory data, PC ← [PC] + 4
4	Temp2 ← [Temp1] + [R7]
5	Memory address ← [Temp2], Read memory, Wait for MFC, Temp1 ← Memory data
6	Temp1 ← [Temp1] AND [R9]
7	Memory address ← [Temp2], Memory data ← [Temp1], Write memory, Wait for MFC

Figure 5.26 Sequence of actions needed to fetch and execute the instruction: And X(R7), R9.

Homework

- P188 5.4