Computer Organization & Architecture

Chapter 5 – Control Signals

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Content of this lecture

- 5.5 Control Signals

Control Signals

- Inter-stage Registers: RA, RB, RZ, RY, RM, and PC-Temp
  - Since data are transferred from one stage to the next in every clock cycle, inter-stage registers are always enabled.
- PC, IR, and the Register File
  - Must be enabled when new data are loaded in.
- MuxB, MuxY
  - To simplify the required control circuit, the same selection can be maintained in all execution steps.
- MuxMA
  - Must change its selection in different execution steps.
  - In Step1:Select PC
  - In Step 4 of Load and Store: Select RZ

Control Signals For the Datapath

- Figure 5.18

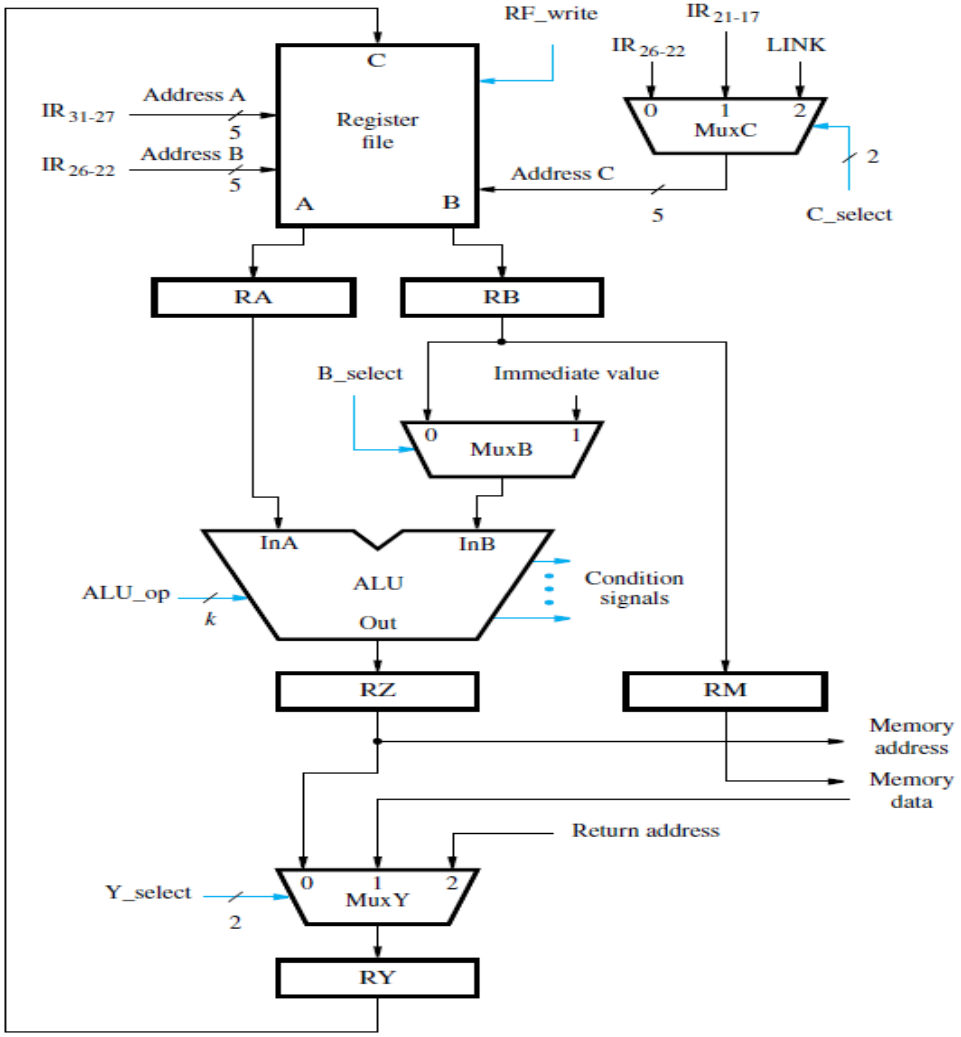
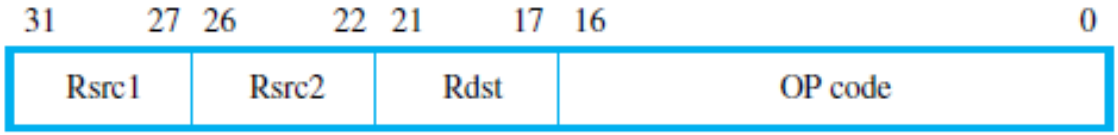


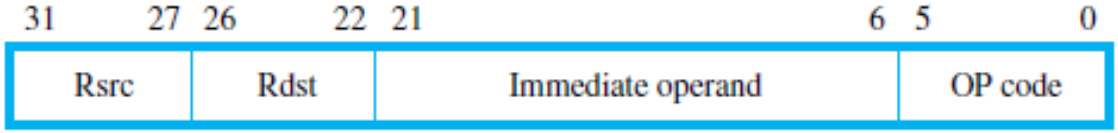
Figure 5.18 Control signals for the datapath.

Recall Instruction Encoding

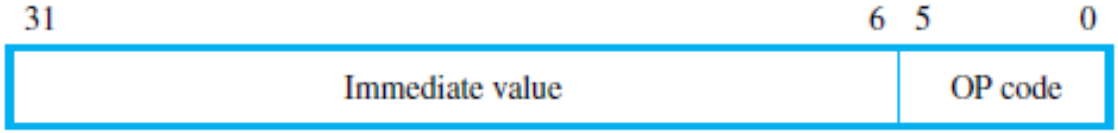
- Figure 5.12



(a) Register-operand format



(b) Immediate-operand format

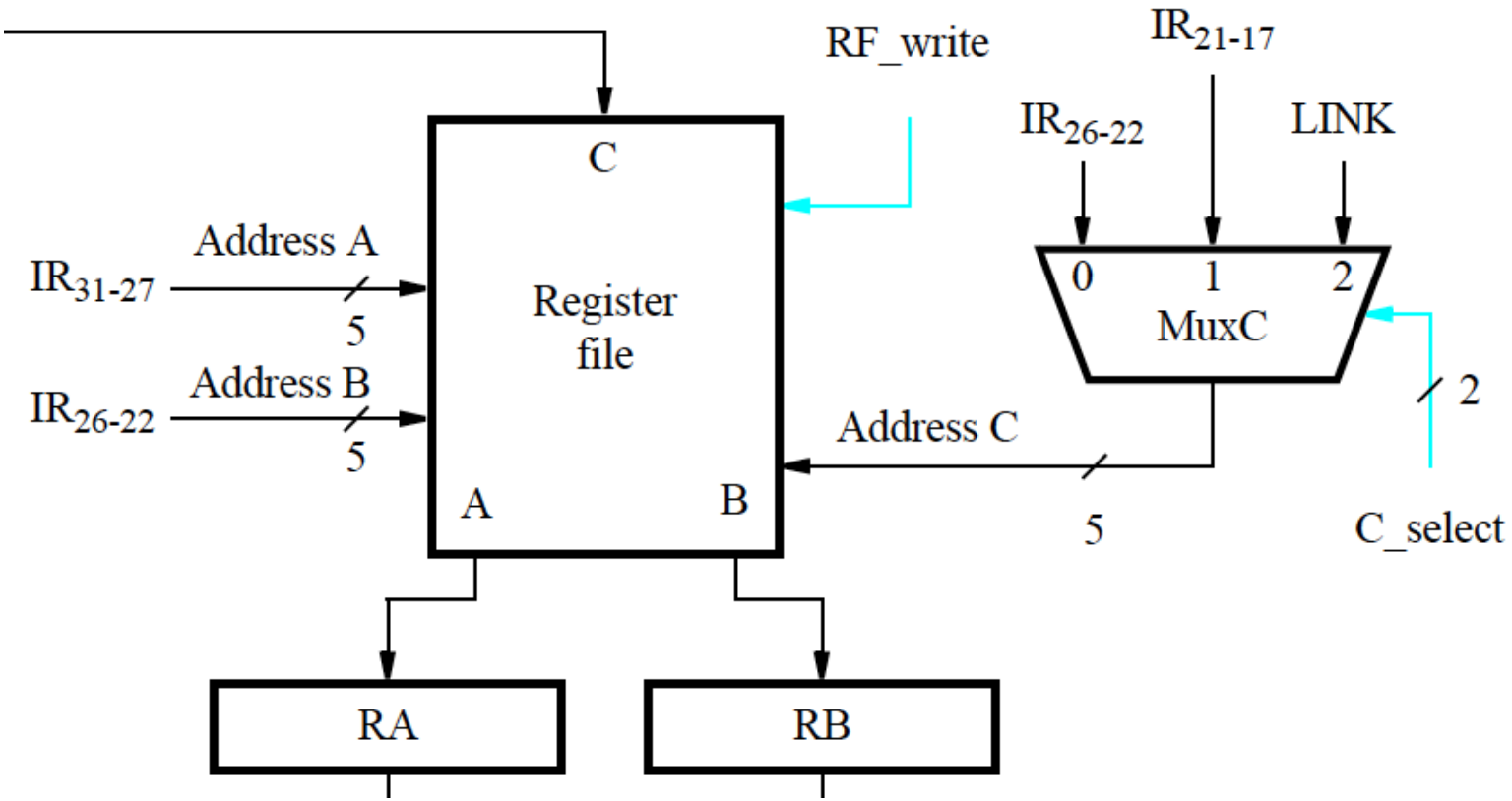


(c) Call format

Figure 5.12 Instruction encoding.

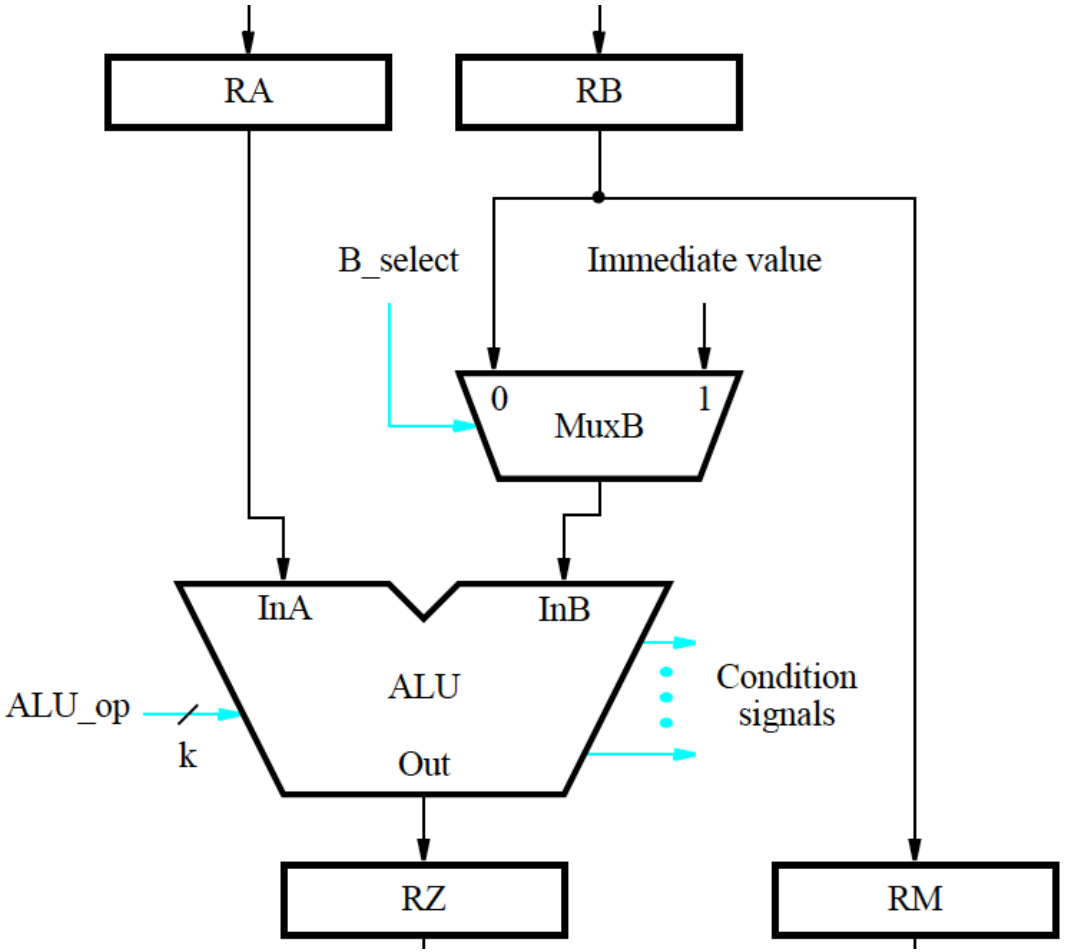
Register File Control Signals

- Part of Figure 5.18
  - RF_write
  - C_select



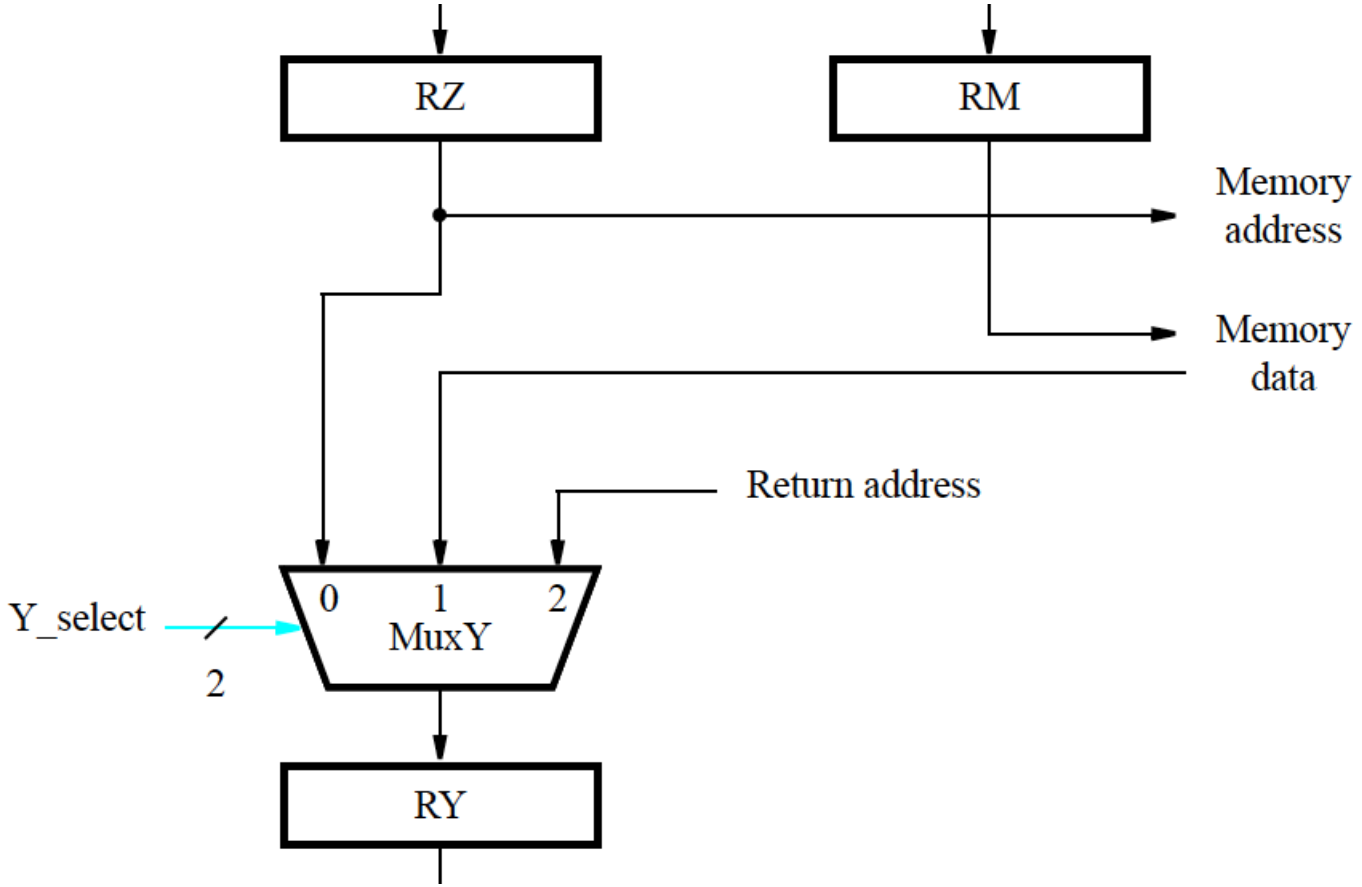
ALU Control Signals

- Part of Figure 5.18 (ctd.)
  - B_selcet
  - ALU_op
  - Condition signals



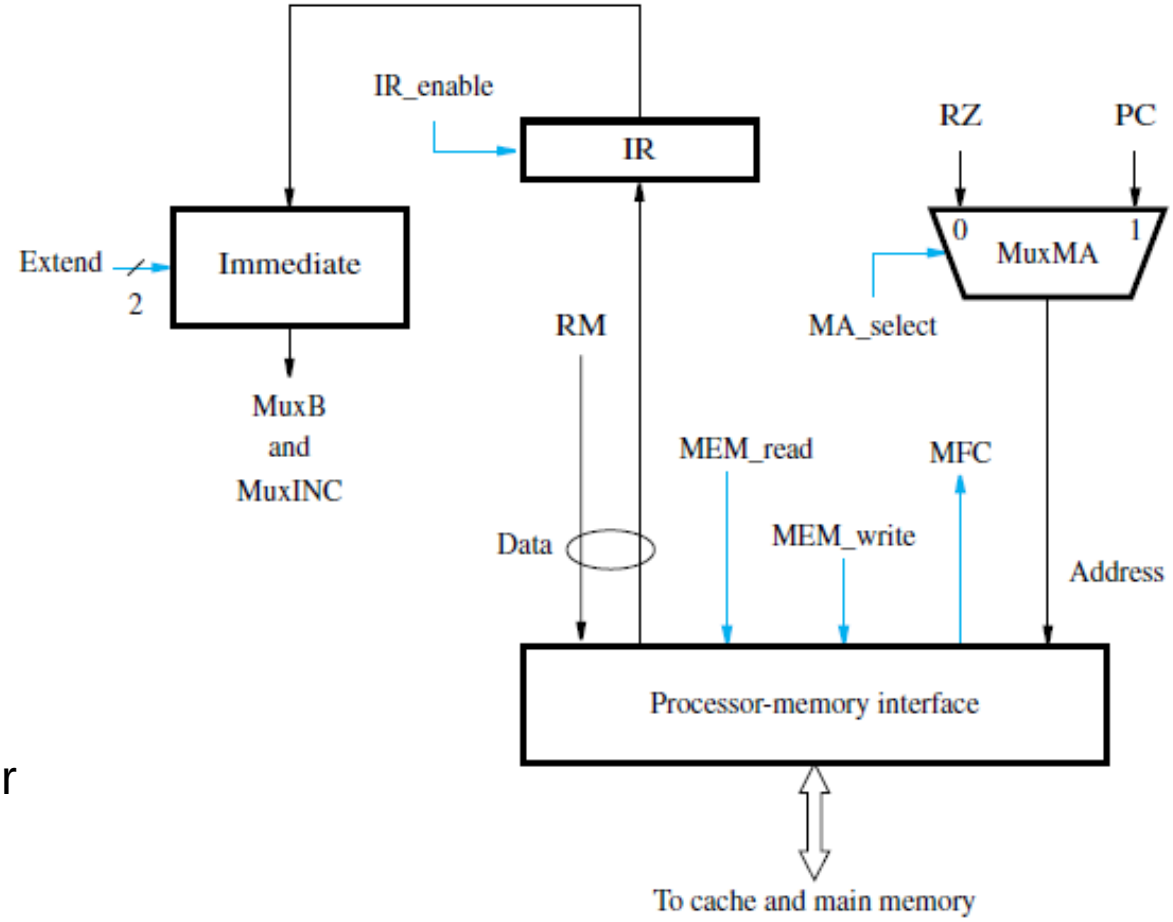
Result Selection Control Signals

- Part of Figure 5.18 (ctd.)
  - Y_select



Processor-Memory Interface Signals

- Figure 5.19
  - MA_select
  - MEM_read
  - MEM_write
  - MFC



MEM_read and MEM_write are used to initiate a memory Read or a memory Write operation.

Figure 5.19 Processor-memory interface and IR control signals.

IR Control Signals (1)

- Figure 5.19
  - IR_enable

During a fetch step, IR_enable must be activated only after the MFC signal is asserted.

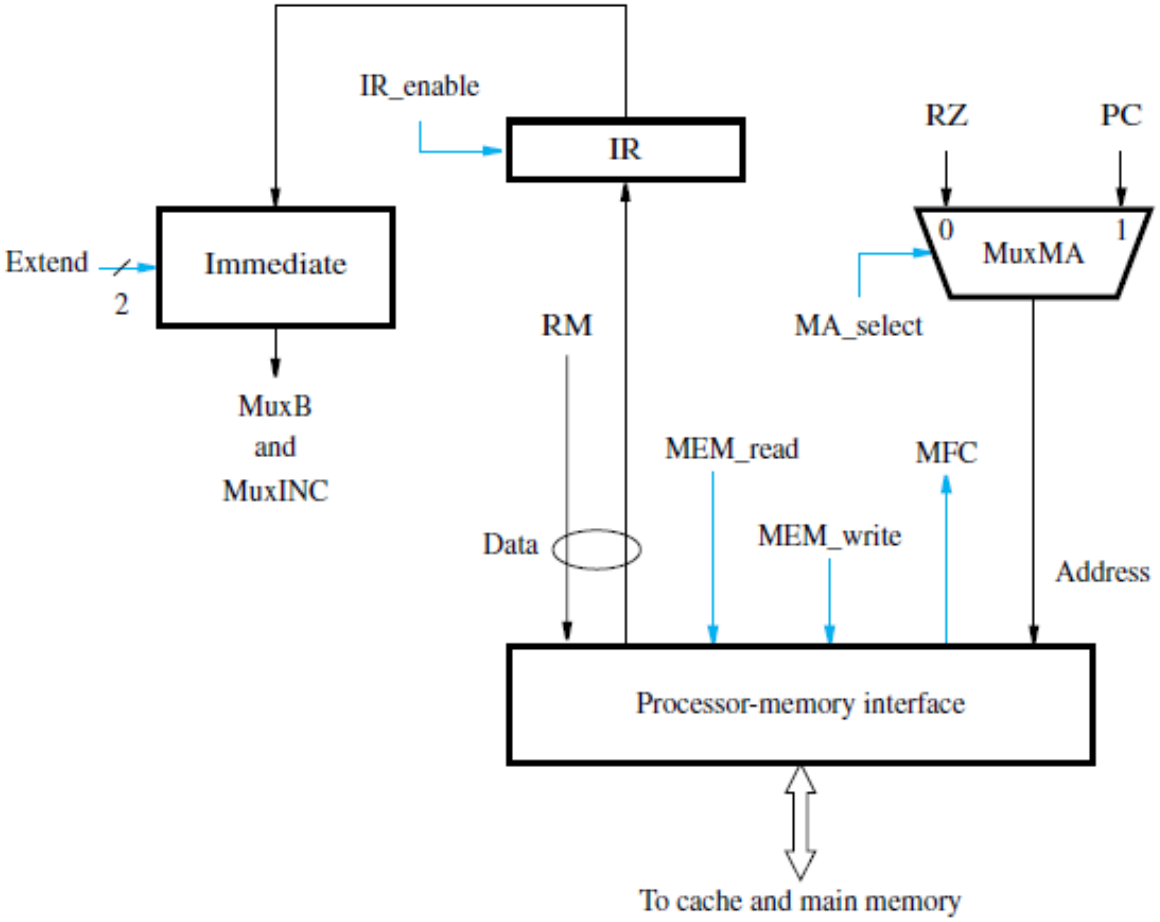


Figure 5.19 Processor-memory interface and IR control signals.

IR Control Signals (2)

- Figure 5.19 (ctd.)
  - Extend

immediate value : be extended to a 32-bit value. Assume that the immediate value is used in three different ways:
(*a*) A 16-bit value is sign-extended for use in arithmetic operations.
(*b*) A 16-bit value is padded with zeros to the left for use in logic operations.
(*c*)A 26-bit value is padded with 2 zeros to the right and the 4 high-order bits of the PC are appended to the left for use in subroutine-call instructions.

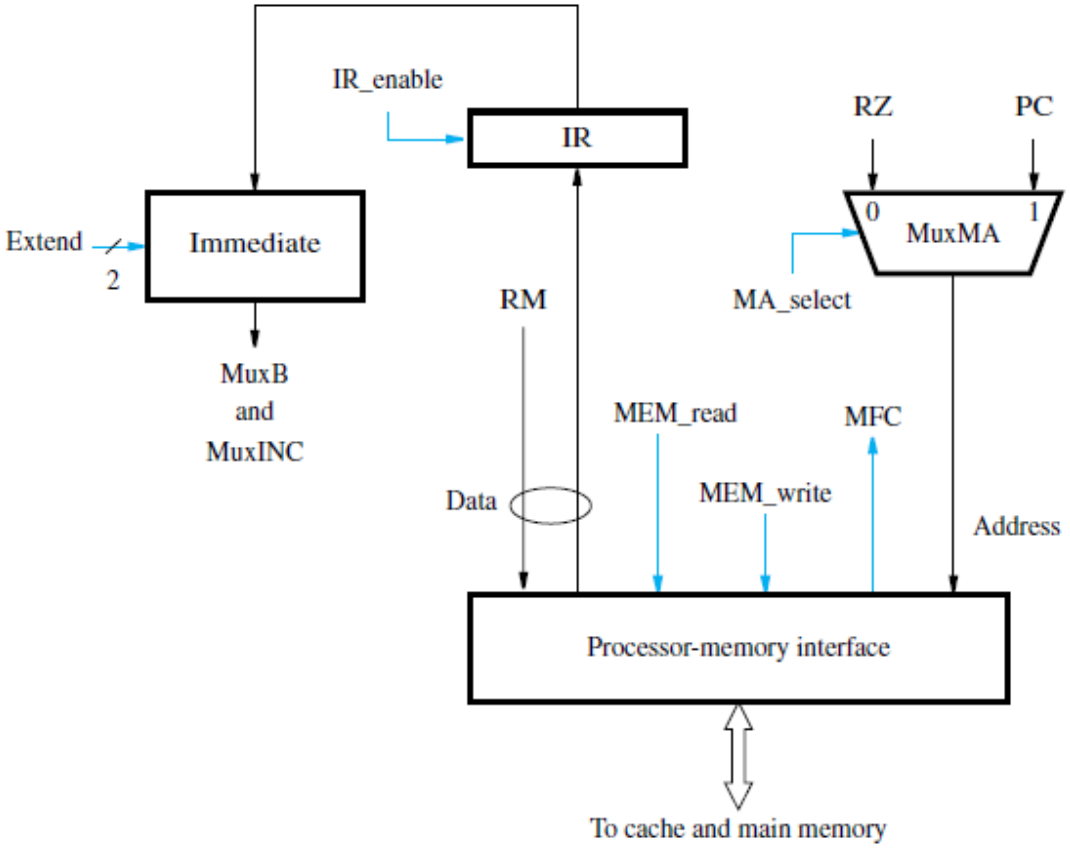


Figure 5.19 Processor-memory interface and IR control signals.

Instruction Address Generator Control Signals

- Figure 5.20
  - PC_select
  - PC_enable
  - INC_select

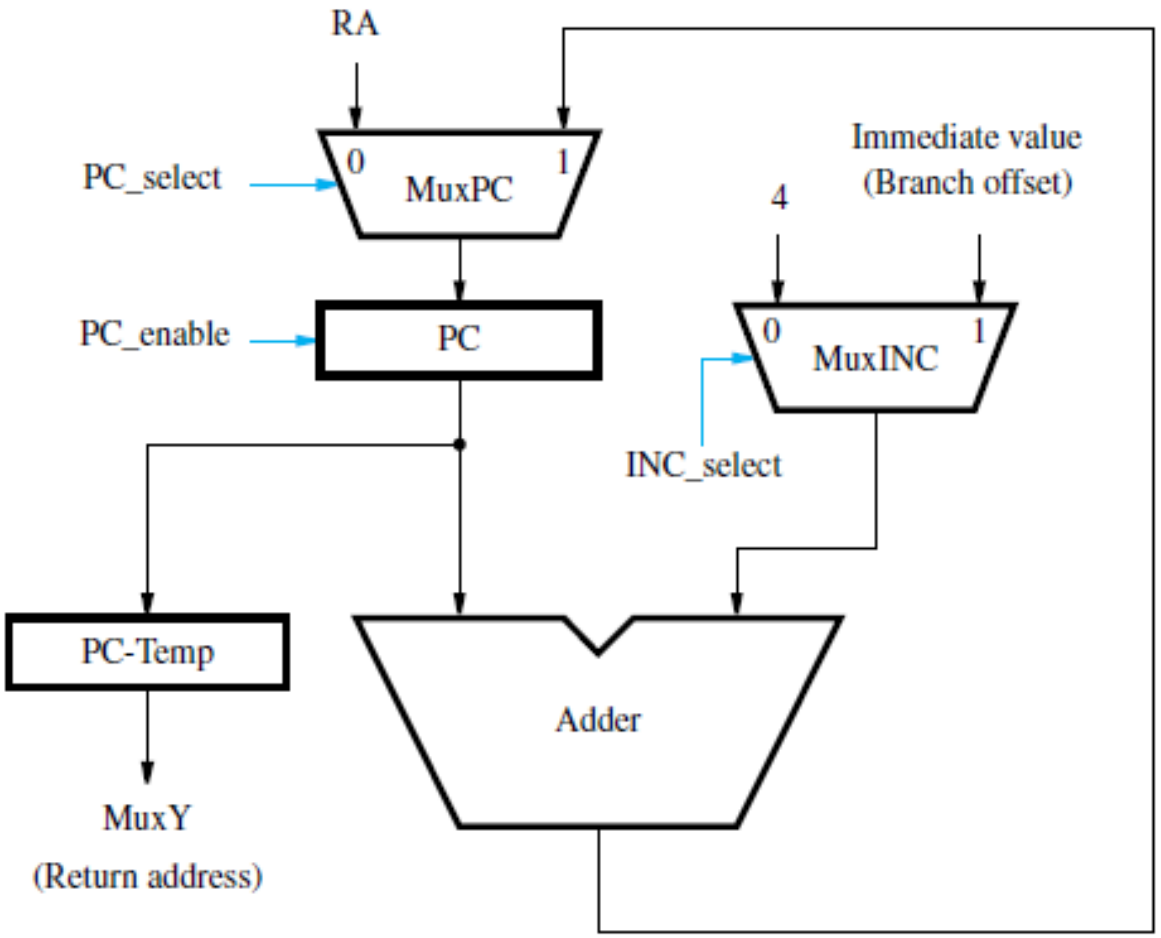


Figure 5.20 Control signals for the instruction address generator.

Summary

- 知识点：Control Signals
- 掌握程度
  - 给出数据通路图，理解各个控制信号。