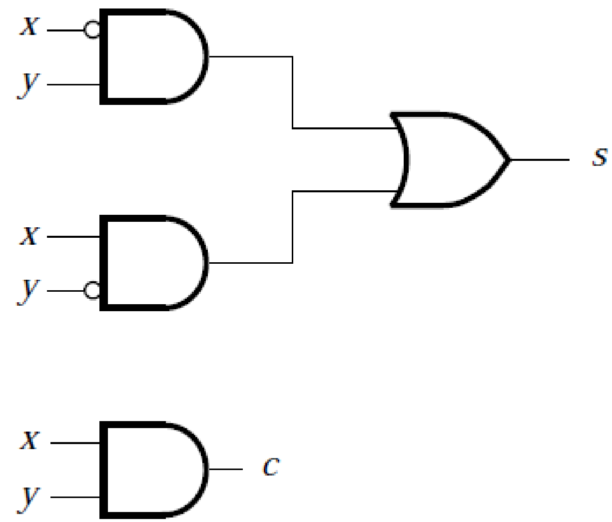
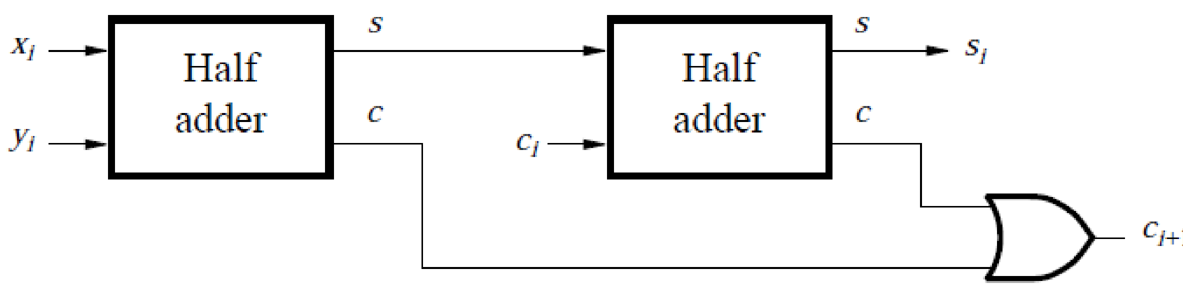
9.1. (*a*) The half adder is implemented as:

x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$$s = x \oplus y$$
$$c = x\,y$$

(*b*)



(*c*) The longest path through the circuit in part (*b*) is 4 gate delays (not including input inversions) in producing s_i; and the longest path through the circuit in Figure 9.2*a* is 2 gate delays (not including input inversions) in producing either c_i or s_i, assuming that s_i is implemented as a two-level AND-OR circuit.

9.9 Solution

(*a*)

$$\begin{array}{r} 010111 \\ \times\, 110110 \\ \hline \end{array} \qquad \begin{array}{r} +23 \\ \times\ \ -10 \\ \hline -230 \end{array}$$

sign extension

$$\begin{array}{rcccccccccccc}
 & & & & & & & 0 & 1 & 0 & 1 & 1 & 1 \\
\times & & & & & & & 0 & -1 & +1 & 0 & -1 & 0 \\ \hline
 & & & & & & & & & & & & 0 \\
 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & \\
 & & & & & & & & & & 0 & & \\
 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & & & \\
 & 1_1 & 1_1 & 1_1 & 0_2 & 1_1 & 0_1 & 0_1 & 1 & & & & \\ \hline
 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0
\end{array}$$

(*b*)

$$\begin{array}{r} 110011 \\ \times\, 101100 \\ \hline \end{array} \qquad \begin{array}{r} -13 \\ \times\ \ -20 \\ \hline 260 \end{array}$$

sign extension

$$\begin{array}{rcccccccccccc}
 & & & & & & & 1 & 1 & 0 & 0 & 1 & 1 \\
\times & & & & & & & -1 & +1 & 0 & -1 & 0 & 0 \\ \hline
 & & & & & & & & & & & & 0 \\
 & & & & & & & & & & & 0 & \\
 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & & \\
 & & & & & & & & & 0 & & & \\
 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & & & & \\
 & 0_1 & 0_1 & 0_1 & 1_1 & 1_1 & 0_2 & 1_1 & & & & & \\ \hline
 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0
\end{array}$$

9.20 Solution

A × B :

M

$\boxed{00101}$

C	A	Q	
$\boxed{0}$	$\boxed{00000}$	$\boxed{10101}$	Initial configuration
0 0	00101 00010	10101 11010	1st cycle
0 0	00010 00001	11010 01101	2nd cycle
0 0	00110 00011	01101 00110	3rd cycle
0 0	00011 00001	00110 10011	4th cycle
0 0	00110 00011	10011 01001	5th cycle

product

A / B :

	A	Q	
	$\boxed{000000}$	$\boxed{10101}$	
	A	Q	Initial configuratio
	$\boxed{000101}$		
	M		
shift	000001	0 1 0 1 $\boxed{\ }$	
subtract	$\underline{111011}$		1st cycle
	111100	0 1 0 1 $\boxed{0}$	
shift	111000	1 0 1 $\boxed{0}$ $\boxed{\ }$	
add	$\underline{000101}$		2nd cycle
	111101	1 0 1 $\boxed{0}$ $\boxed{0}$	
shift	111011	0 1 $\boxed{0}$ $\boxed{0}$ $\boxed{\ }$	
add	$\underline{000101}$		3rd cycle
	000000	0 1 $\boxed{0}$ $\boxed{0}$ $\boxed{1}$	
shift	000000	1 $\boxed{0}$ $\boxed{0}$ $\boxed{1}$ $\boxed{\ }$	
subtract	$\underline{111011}$		4th cycle
	111011	1 $\boxed{0}$ $\boxed{0}$ $\boxed{1}$ $\boxed{0}$	
shift	110111	$\boxed{0}$ $\boxed{0}$ $\boxed{1}$ $\boxed{0}$ $\boxed{\ }$	
add	$\underline{000101}$		5th cycle
	111100	$\boxed{0}$ $\boxed{0}$ $\boxed{1}$ $\boxed{0}$ $\boxed{0}$	
add	$\underline{000101}$	$\underbrace{\qquad\qquad}_{\text{quotient}}$	
	$\underbrace{000001}_{\text{remainder}}$		

9.21 Solution

(a) +1.7 0 01111 101101

1.7转换为二进制1.101100110，使用rounding方法truncation

– 0.012 1 01000 100010

+19 0 10011 001100

1/8 0 01100 000000

(d) A+B = 0 10000 000000

A – B =0 10000 110110

9.22 Solution

(a) Shift the mantissa of B right two positions, and tentatively set the exponent of the sum to 100001. Add mantissas:

$$\begin{array}{lr} (A) & 1.11111111000 \\ (B) & 0.01001010101 \\ \hline & 10.01001001101 \end{array}$$

Shift right one position to put in normalized form: 1.001001001101 and increase exponent of sum to 100010. Truncate the mantissa to the right of the binary point to 9 bits by rounding to obtain 001001010. The answer is 0 100010 001001010.

(b)

$$\begin{aligned} \text{Largest} &\approx 2 \times 2^{31} \\ \text{Smallest} &\approx 1 \times 2^{-30} \end{aligned}$$

This assumes that the two end values, 63 and 0 in the excess-31 exponent, are used to represent infinity and exact 0, respectively.