Computer Organization & Architecture

Chapter 5 – Hardwired Control

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Content of this lecture

- 5.6 Hardwired Control
- Summary

Control Signal Generation

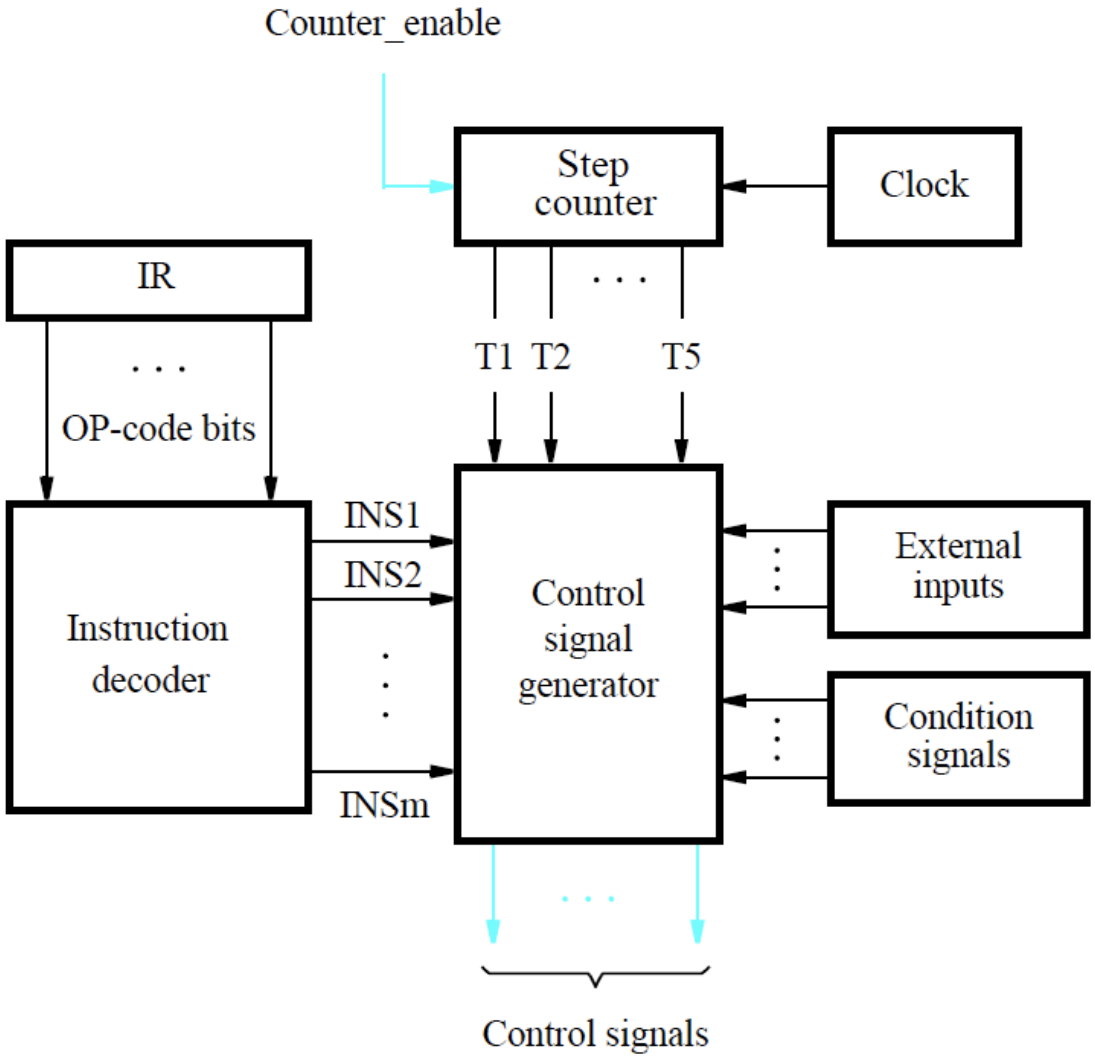
- Circuitry must be implemented to generate control signals so actions take place in correct sequence and at correct time.
- There are two basic approaches
  - Hardwired Control
    - The control unit is essentially a combinational circuit. Its input logic signals are transformed into a set of output logic signals, which are the control signals.
  - Microprogrammed Control
    - The control signals are generated by a microprogram.

Hardwired Control (1)

- Control Signal Generation
  - Contents of the step counter.
  - Contents of the instruction register.
  - The result of a computation or a comparison operation.
  - External input signals, such as interrupt requests.

Hardwired Control (2)

- Control Signal Generation (ctd.)



Instruction Fetch Control Signals (1)

- Recall : Step1 (instruction fetch):

Memory address ← [PC], Read memory, Wait for MFC,
IR ← Memory data, PC ← [PC] + 4

T1=1,

MA_select=1,

MEM_read, WMFC, IR_enable

INC_select=0, PC_select=1, PC_enable=1

Instruction Fetch Control Signals (2)

MA_select=1,

MEM_read, WMFC, IR_enable

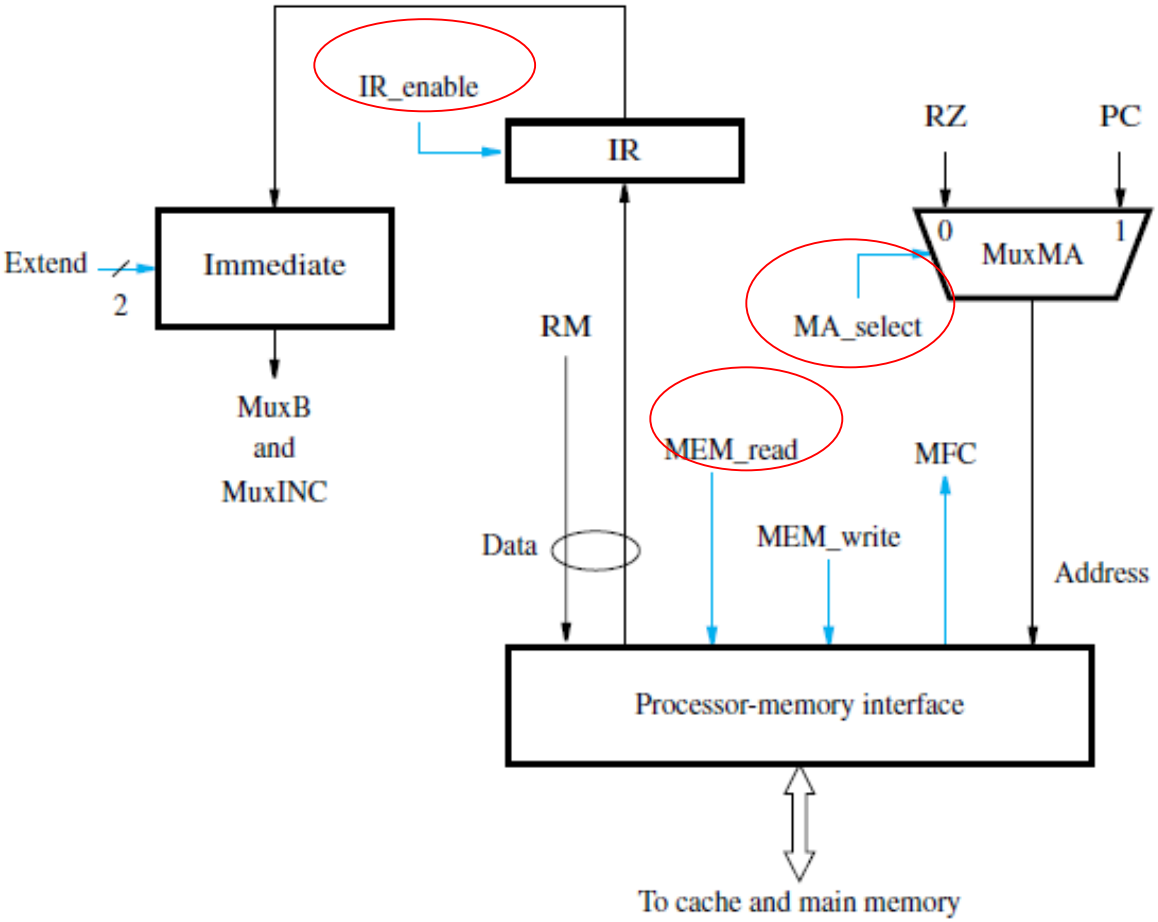


Figure 5.19 Processor-memory interface and IR control signals.

Instruction Fetch Control Signals (3)

INC_select=0, PC_select=1, PC_enable=1

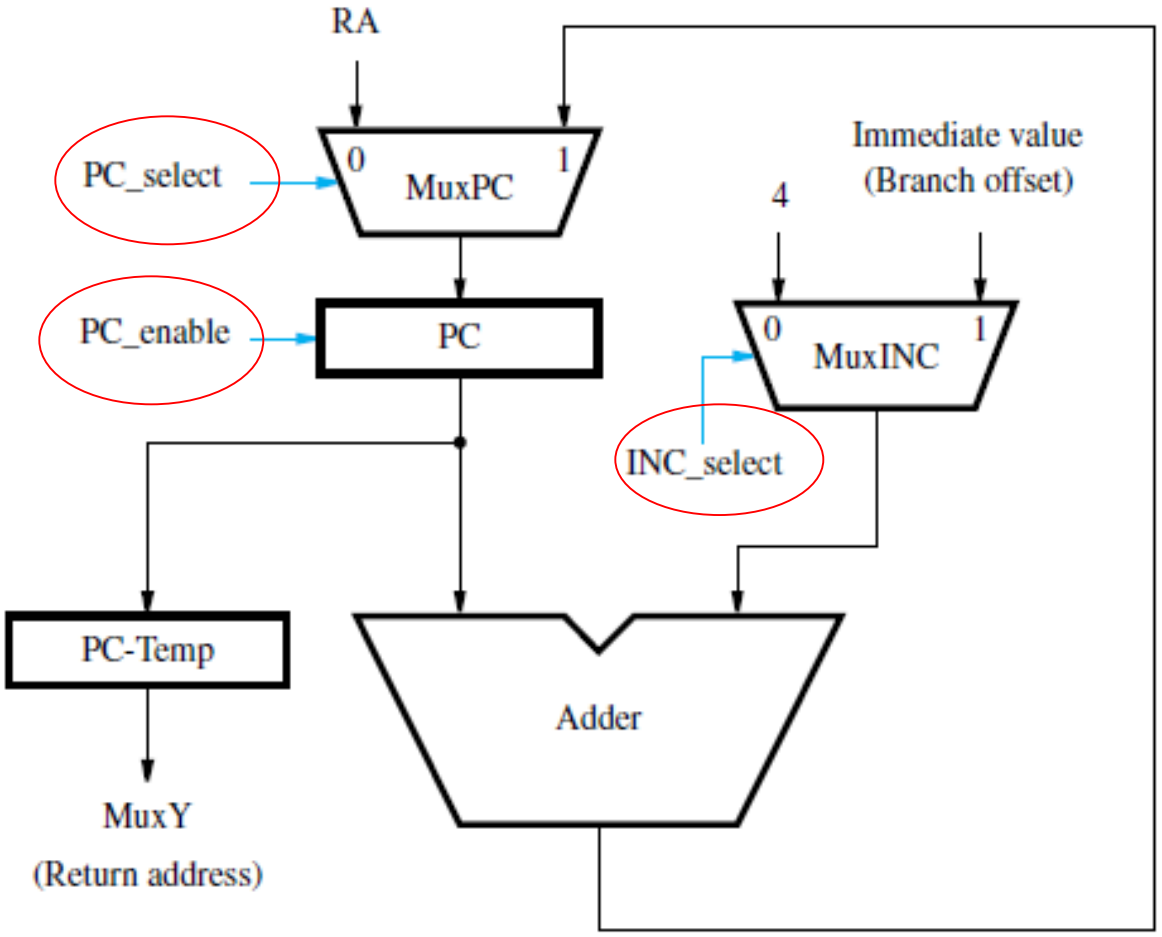


Figure 5.20 Control signals for the instruction address generator.

Data Path Control Signals (1)

- Datapath Control Signals

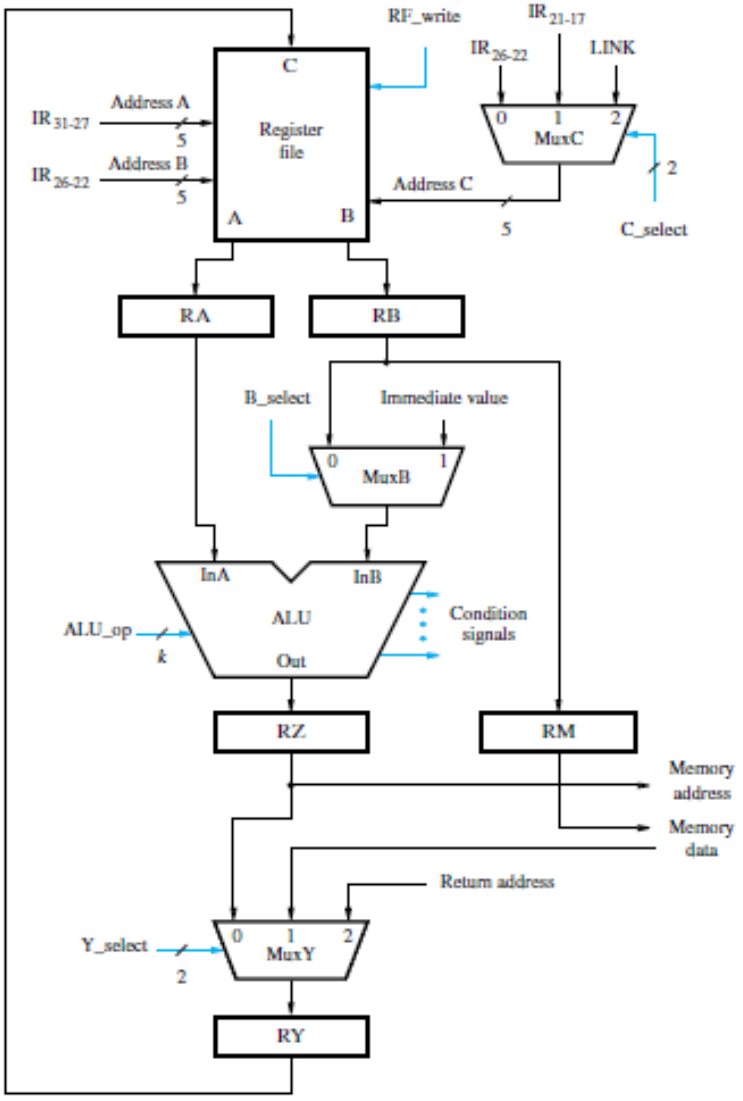


Figure 5.18 Control signals for the datapath.

Data Path Control Signals (2)

- Datapath Control Signals
  - Inter-stage registers RA, RB, RZ, RM, and RY are always enabled. This means that data flow automatically from one datapath stage to the next on every active edge of the clock signal.
  - The desired setting of various control signals can be determined by examining the actions taken in each execution step of every instruction.
    - RF_write = T5 · (ALU + Load + Call)
    - B_select = Immediate
      - Immediate stands for all instructions that use an immediate value in the IR

Data Path Control Signals (3)

- Datapath Control Signals (ctd.)
  - Recall: Add R3, R4, R5 (ctd.)
    - Sequence of Actions

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R4], RB ← [R5]
3	RZ ← [RA] + [RB]
4	RY ← [RZ]
5	R3 ← [RY]

Figure 5.11 Sequence of actions needed to fetch and execute the instruction: Add R3, R4, R5.

Data Path Control Signals (4)

- Datapath Control Signals (ctd.)
  - Recall: Load R5, X(R7)
    - Sequence of Actions

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R7]
3	RZ ← [RA] + Immediate value X
4	Memory address ← [RZ], Read memory, RY ← Memory data
5	R5 ← [RY]

Figure 5.13 Sequence of actions needed to fetch and execute the instruction: Load R5, X(R7).

Data Path Control Signals (5)

- Datapath Control Signals (ctd.)
  - Example: Call_Register R9

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R9]
3	PC-Temp ← [PC], PC ← [RA]
4	RY ← [PC-Temp]
5	Register LINK ← [RY]

Figure 5.17 Sequence of actions needed to fetch and execute the instruction: Call_Register R9.

Advantage & Disadvantages

- Hardwired control provides highest speed.
- This greater speed coupled with the much higher cost of the hardwired systems tended to restrict their use to high performance computers.
- Inflexible.
- RISCs are implemented with hardwired control.
- With the trend toward simpler instructions and control, and the advent of computer aided design (CAD) tools, the design of hardwired control unit has become much easier and less prone to errors.
- If the instruction set becomes very complex (CISCs) implementing hardwired control is very difficult. In this case microprogrammed control units are used.

Summary

- 知识点：Hardwired Control Unit
- 掌握程度
  - 会画课本图5.21，并描述原理。