计算机组成与体系结构期末考试样题

一、单项选择题

1. The part of machine instruction, which tells the central processor what was to be done is .

A. operation code B. address C. operand D. none of the above

1. Which of the following is not the basic I/O method in a computer system? .

A. DMA approach B. interrupt-driven

C. event-driven D. program-controlled I/O

3. In carry-lookahead adder, the expression is called the propagate function Pi for stage i.

A. xi+yi B. xi⊕yi C. xiyi D. xi⊕yi⊕ci

4. In hardwired control unit, the required control signals are determined by the following information except .

A. contents of the control step counter B. contents of the instruction register

C. contents of the condition code flags D. contents of the program counter

5. When I/O devices and the memory share the same address space, the arrangement is called .

A. memory-mapped I/O B. mixed I/O C. separated I/O D. relative I/O

6. Suppose that a 2M x 16 main memory is built using 256K x 8 RAM chips and memory is word-addressable. How many RAM chips are necessary? .

A. 4 B. 8 C. 16 D. 32

二、简答题

1. What is the difference between a subroutine and an interrupt-service routine?

2. What are the advantage(s) and disadvantage(s) of hardwired control unit?

三、综合题

1. Consider the memory system with the following specifications:

* Byte-addressable
* Virtual address space: 4G bytes
* Main memory size: 16M bytes
* Cache size: 256K bytes
* Page size: 64K bytes
* Block size: 128bytes
* Mapping Strategies: Main Memory to Cache: 4-way set associative; Hard Disk to Main Memory: fully associative

Virtual address is first translated to physical address. Then, it accesses the cache memory using the physical address.

1. How many sets are there in the cache memory?
2. How long is the tag field of the cache?
3. Given a virtual address 0B45DA12 (hexadecimal), its corresponding virtual page is stored in physical page 3E (hexadecimal).
   * + 1. What is its physical address under such mapping?
       2. Which set can this address be possibly found in the cache?
       3. Which byte does this address point to out of the 128 bytes in a block?
4. Give the sequence of steps needed to fetch and execute the instruction

SUB R1, R2, R3

on a 5-stage RISC processor. Assume 32-bit operands.

1. Consider the following instructions at the given addresses in the memory:

***1000 Add R3, R2, #20***

***1004 Subtract R5, R4, #3***

***1008 And R6, R3, #0x3A***

***1012 Add R7, R2, R4***

Assume that the pipeline provides forwarding paths to the ALU from registers RY and RZ and that the processor uses forwarding of operands.

1. Draw a diagram that represents the flow of the instructions through the pipeline.
2. Describe the contents of registers IR, PC, RA RB, RY, and RZ in the pipeline during cycles 2 to 8.