In this online course I learned the following things related to Digital Logic Design circuit implementation on Verilog VHDL Language as follows:

➢ ALL LOGIC GATES AND HALF ADDER. FULL ADDER (Three Modelling styles).
➢ FULL SUBTRACTOR (Three Modelling styles).
➢ 8x1 Mux (Three Modelling styles).
➢ 8x1 Mux by 4x1 mux and 2x1 mux.
➢ GATES BY 2X1 MUX.
➢ 8x1 Demux .
➢ 1x8 Demux by 1x2 demux and 1x4 demux.
➢ 8:3 enocder .
➢ 3:8 decoder .
➢ 8:3 priority enocder (Bhevioural model).
➢ BCD TO 7 SEGMENT.
➢ COMPARATOR 4 BIT(Bhevioural model).
➢ ADDER-SUBTRACTOR.
➢ FLIPFLOPS (Behavioural model).
➢ Multiplier 4-Bit.
➢ Counters.
➢ Serial in Serial Out shift register(SISO).
➢ Serial in parallel Out shift register.(SIPO)
➢ parallel in parallel Out shift register.(PIPO)
➢ parallel in Serial Out shift register.(PISO)
➢ Universal Shift Register.
➢ ALU 8-bit
➢ Swapping of two numbers
➢ N bit square number.
➢ FSM .