Shift and Add Binary Multiplier

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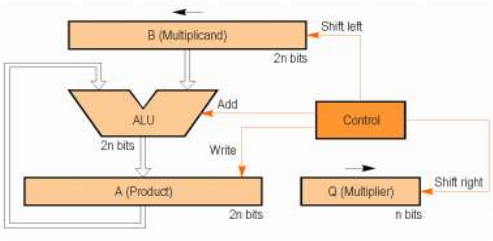
***Abstract*—This paper presents the design of a basic 4X4 shift and add binary multiplier which is used for multiplying 2 numbers in binary format .It uses adders and shifters for multiplying and is controlled to shift control appropriately for all conditions to do multiplication efficiently.**

Keywords- 4X4 Shift and Add Multiplier, Adder, Shifter, Controller

I. INTRODUCTION

Binary multipliers are used for multiplication of 2 binary numbers and are used mainly in signal processing and also in other computationally intensive applications. Shift and add binary multiplier is a type of sequential multiplier. Sequential multipliers generate the partial products sequentially and add each newly generated partial product to the previously accumulated sum. Shift and add binary multiplier is a type of sequential multiplier. Section II discusses about circuit description and algorithm of shift and add multiplier and Section III discusses about the output waveform.

II. CIRCUIT DESCRIPTION



First version of the multiplier circuit.

Shift and add multiplier is similar to multiplication done by paper and pencil. This method adds the multiplicand X to itself Y times, where Y denotes the multiplier In the case of binary multiplication, since the digits are 0 and 1, if the multiplier digit is 1, a copy of the multiplicand is placed in the proper positions; if the multiplier digit is 0, a number of 0 digits are placed. The 2n-bit product register (A) is initialized to 0. A 2n-bit multiplicand register with the multiplicand placed in the right half of the register and with 0 in the left half is used. The algorithm starts by loading the multiplicand into the B register, loading the multiplier into the Q register, and initializing the A register to 0. The counter N is initialized to n. The least significant bit of the multiplier register (Q0) determines whether the multiplicand is added to the product register. The left shift of the multiplicand has the effect of shifting the intermediate products to the left and right shift prepares the next bit of the multiplier to examine in the following iteration.

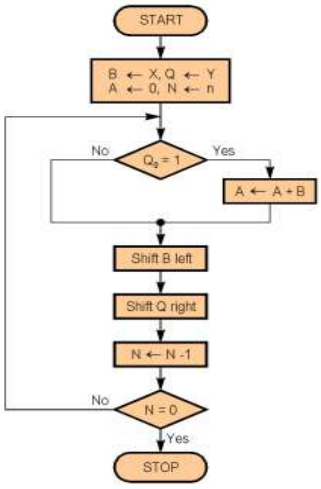
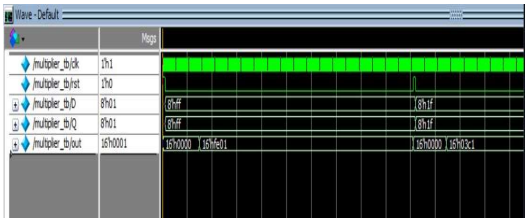


Figure 3.12. The first version of the multiplication algorithm.

III. WAVEFORM

When rst is high, no multiplication is done and in the next clock numbers are multiplied.



1) FF*FF=FE01 (255*255=65025)

2)1F*1F=03C1 (31*31=961)

REFERENCES

https://users.utcluj.ro/~baruch/book_ssce/SSCE-Shift-Mult.pdf