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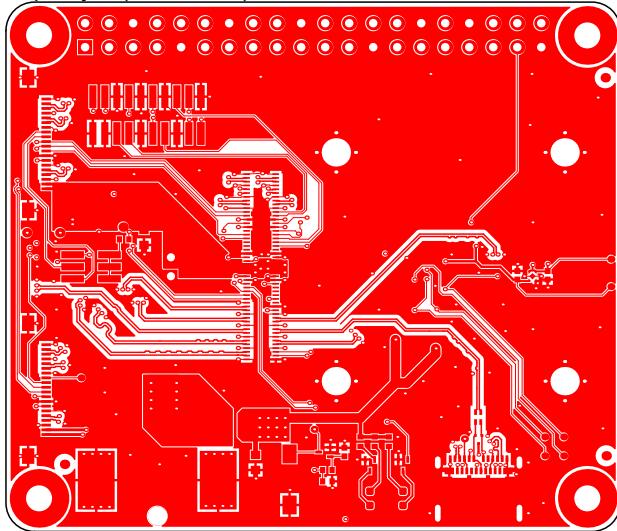
B

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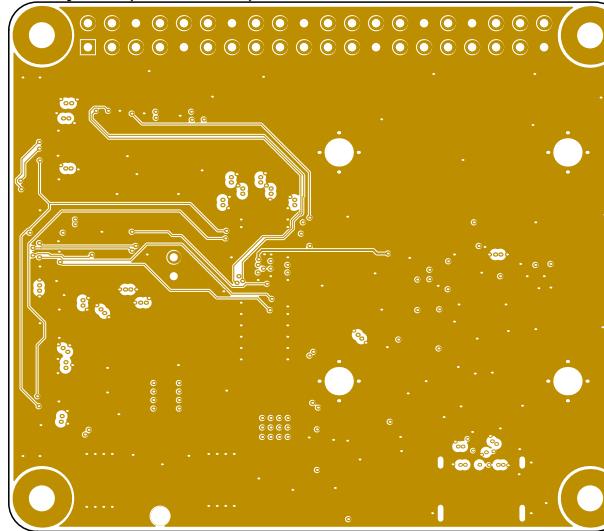
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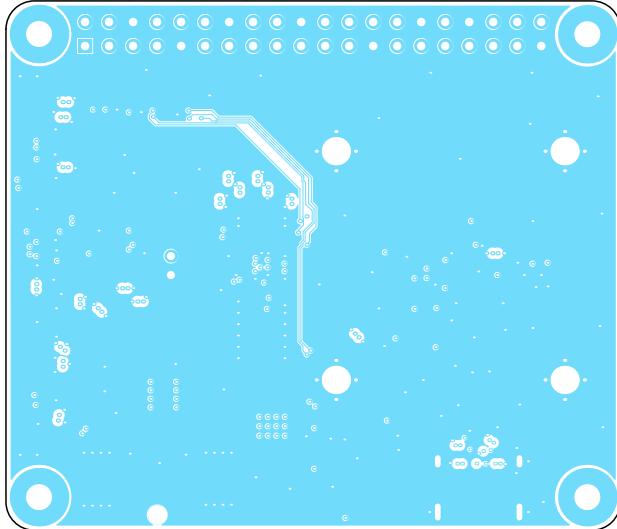
Top Layer (Scale 1.25)



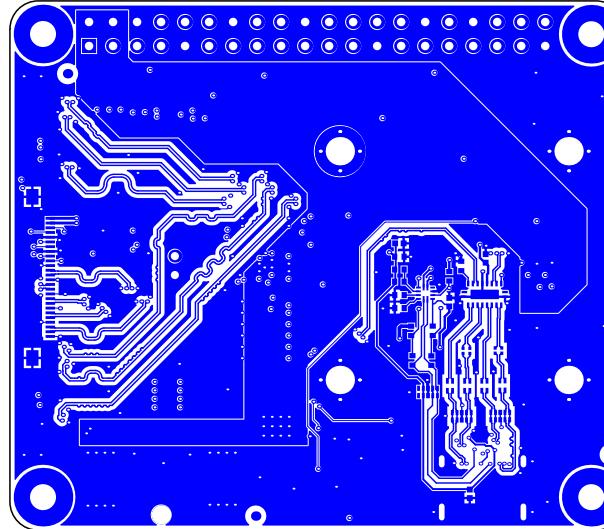
Midlayer 1 (Scale 1.25)



Midlayer 2 (Scale 1.25)



Bottom Layer (Scale 1.25)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2

Inspect per IPC-A-600 CLASS 2

Test per IPC-TM-650

PCB has 4 copper layers

Copper thicknesses are finished and include base foil plus Cu plating on plated layers.

PCB thickness: 63mil +/- 3mil

Min. trace width/clearance: 4/4mil

Min. hole drill/ring: 8mil/16mil

Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.

Silkscreen, non-conductive epoxy ink, color: white

Clip silkscreen as needed to prevent deposition on any exposed copper

Surface finish: ENIG

Hole dimensions are finished size, +/-3mil

Linear board dimension tolerance: +/-10mil

Bow, twist, warp not to exceed 0.75% of greatest diagonal span

PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0

PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side

All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondary side.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: **BW1094**Number: D0000194 Revision: R1M1
E1

Date: 12/4/2019 Sheet: 1 of 3

Drawn by: Brian Weinstein

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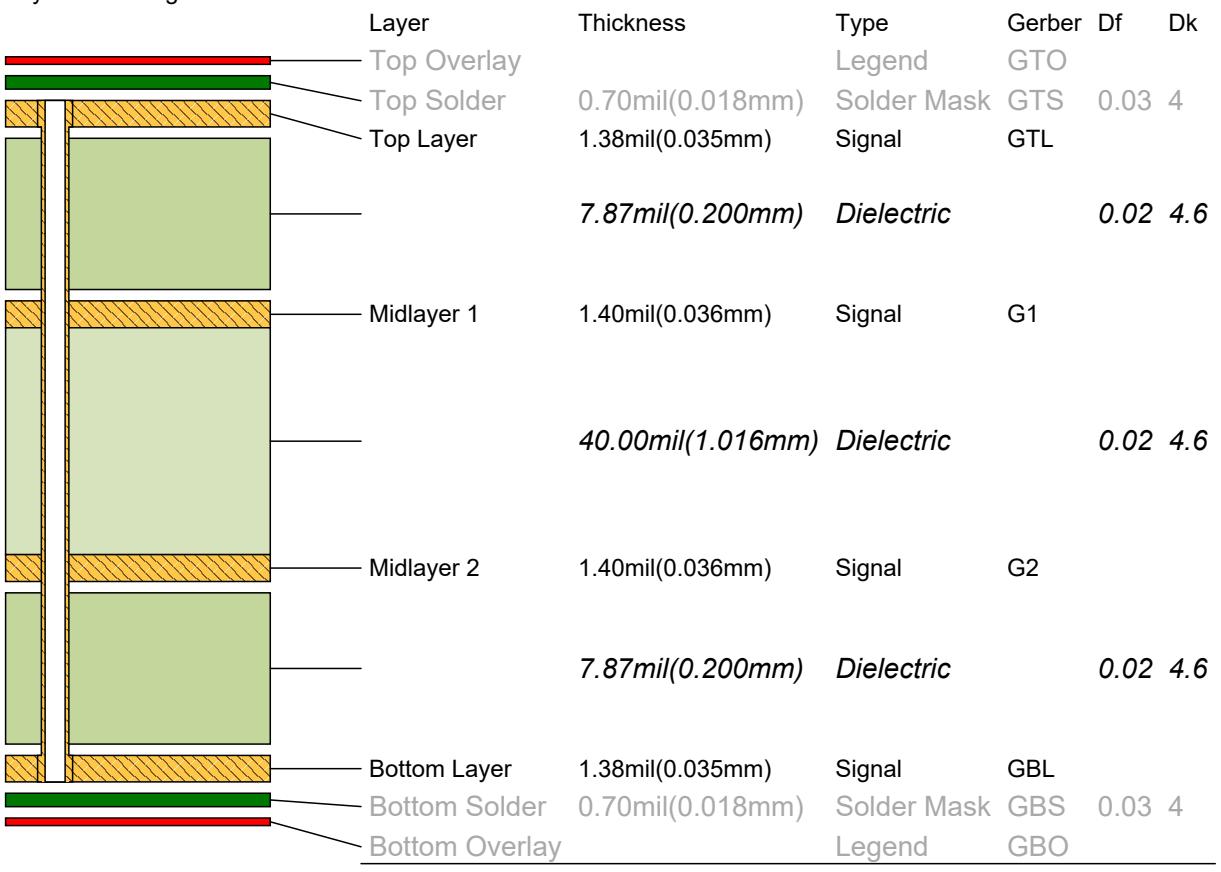
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Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
☆	321	0.01in	Plated	None
◊	16	0.01in	Plated	None
◇	4	0.02in	Plated	None
⊕	2	0.03in	Plated	None
○	40	0.04in	Plated	None
✗	1	0.08in	Non-Plated	None
❖	4	0.11in	Plated	None
□	4	0.12in	Non-Plated	None
392 Total				

Layer Stack Legend



Title: BW1094

Number: D0000194 Revision: R1M1
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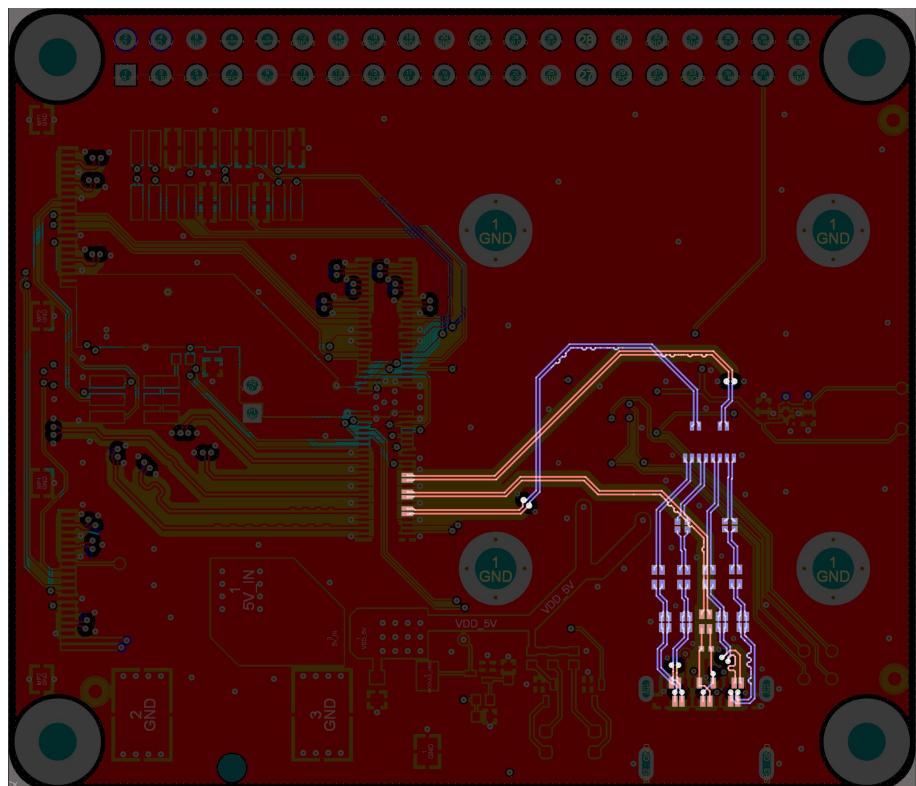
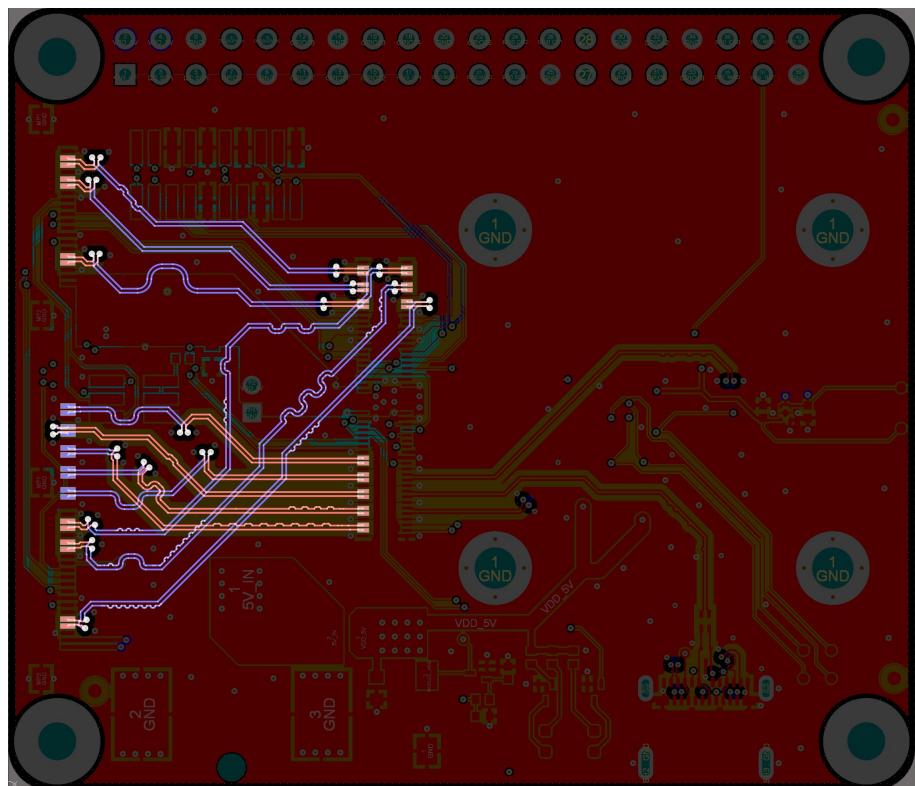
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90 OHM (+/-10%) DIFF PAIRS**100 OHM (+/-10%) DIFF PAIRS****Transmission Line Structure Table**

Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Trace Width	Gap	Reference layers
Edge-Coupled Coated Microstrip	90	89.96	Top Layer	0.16mm	0.10mm	Midlayer 1
Edge-Coupled Coated Microstrip	100	100.00	Top Layer	0.15mm	0.14mm	Midlayer 1
Edge-Coupled Coated Microstrip	90	90.02	Bottom Layer	0.16mm	0.10mm	Midlayer 2
Edge-Coupled Coated Microstrip	100	100.00	Bottom Layer	0.15mm	0.14mm	Midlayer 2

Title: **BW1094**Number: D0000194 Revision: R1M1
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