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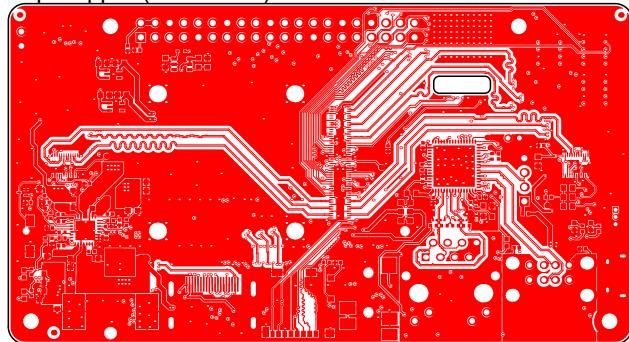
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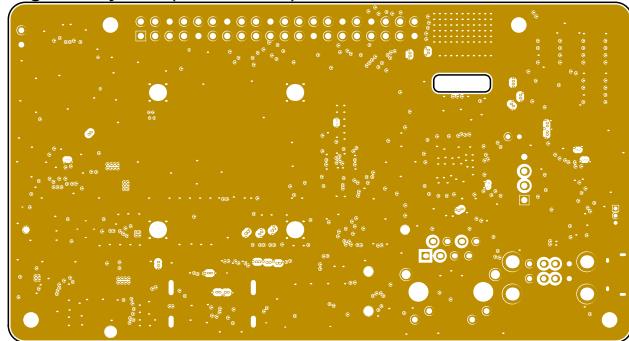
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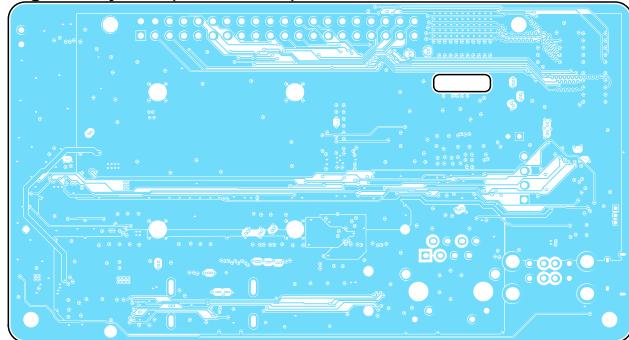
Top Copper (Scale 0.75)



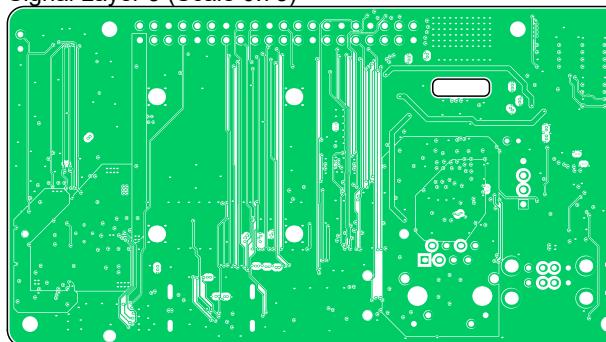
Signal Layer 1 (Scale 0.75)



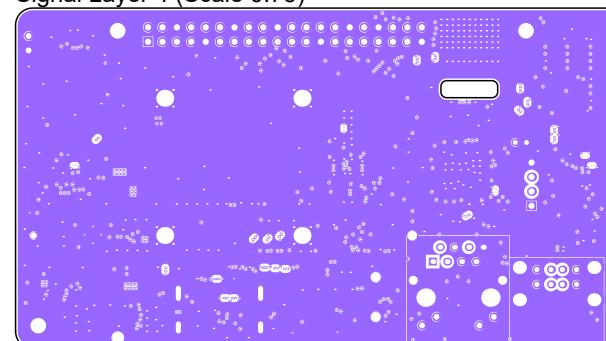
Signal Layer 2 (Scale 0.75)



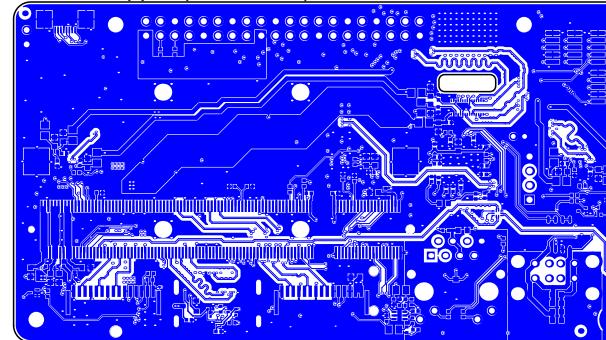
Signal Layer 3 (Scale 0.75)



Signal Layer 4 (Scale 0.75)



Bottom Copper (Scale 0.75)

**FABRICATION NOTES:**

Fabricate per IPC-6011 & IPC-6012 CLASS 2

Inspect per IPC-A-600 CLASS 2

Test per IPC-TM-650

- * PCB has 6 copper layers
- * Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- * PCB thickness: 63mil +/- 3mil
- * Min. trace width/clearance: 4/4mil
- * Min. hole drill/ring: 8mil/16mil
- * Plugging and plating is not required for via-in-pad
- * Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- * Silkscreen, non-conductive epoxy ink, color: WHITE
- * Soldermask color: BLACK
- * Remove silkscreen as needed to prevent ink on any exposed copper
- * Surface finish: ENIG
- * Hole dimensions are finished size, +/-3mil
- * Linear board dimension tolerance: +/-10mil
- * Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- * PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- * PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- * All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: **BW1097**Number: D0000196 Revision: R2M2
E3

Date: 12/3/2019 Sheet: 1 of 3

Drawn by: Brian Weinstein

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Layer Stack Legend

	Layer	Thickness	Type	Gerber	Df	Dk
1	Top Overlay	0.59mil(0.015mm)	Legend	GTO		
	Top Mask	1.38mil(0.035mm)	Solder Mask	GTS	3.8	
	Top Copper	3.94mil(0.100mm)	Signal	GTL		
	Signal Layer 1	0.69mil(0.017mm)	Dielectric		4.05	
	Signal Layer 2	22.24mil(0.565mm)	Signal	G1		
	Signal Layer 3	0.69mil(0.017mm)	Dielectric		4.5	
	Signal Layer 4	5.00mil(0.127mm)	Signal	G2		
	Bottom Copper	0.69mil(0.017mm)	Dielectric		4.25	
2	Bottom Mask	3.94mil(0.100mm)	Signal	G3		
	Bottom Overlay	1.38mil(0.035mm)	Dielectric		4.5	
		0.59mil(0.015mm)	Signal	GBL		
			Solder Mask	GBS	3.8	
			Legend	GBO		

Total thickness: 64.05mil(1.627mm)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	106	8.00mil(0.203mm)	Plated	None
✳	673	10.00mil(0.254mm)	Plated	None
☒	2	19.69mil(0.500mm)	Plated	None
☒	2	21.65mil(0.550mm)	Plated	None
△	3	27.56mil(0.700mm)	Plated	None
◆	2	33.86mil(0.860mm)	Plated	None
☆	8	35.04mil(0.890mm)	Plated	None
○	4	35.43mil(0.900mm)	Plated	None
✳	8	36.22mil(0.920mm)	Plated	None
☒	6	40.16mil(1.020mm)	Plated	None
☆	44	43.31mil(1.100mm)	Plated	None
▲	1	43.31mil(1.100mm)	Plated	+/-3.94mil(0.100mm)
◆	2	62.99mil(1.600mm)	Plated	None
✳	1	62.99mil(1.600mm)	Plated	+/-3.94mil(0.100mm)
◇	2	66.93mil(1.700mm)	Non-Plated	None
□	1	78.74mil(2.000mm)	Non-Plated	None
✳	4	90.55mil(2.300mm)	Plated	None
◆	4	108.27mil(2.750mm)	Plated	None
○	4	118.11mil(3.000mm)	Plated	None
✚	2	127.95mil(3.250mm)	Plated	None
879 Total				

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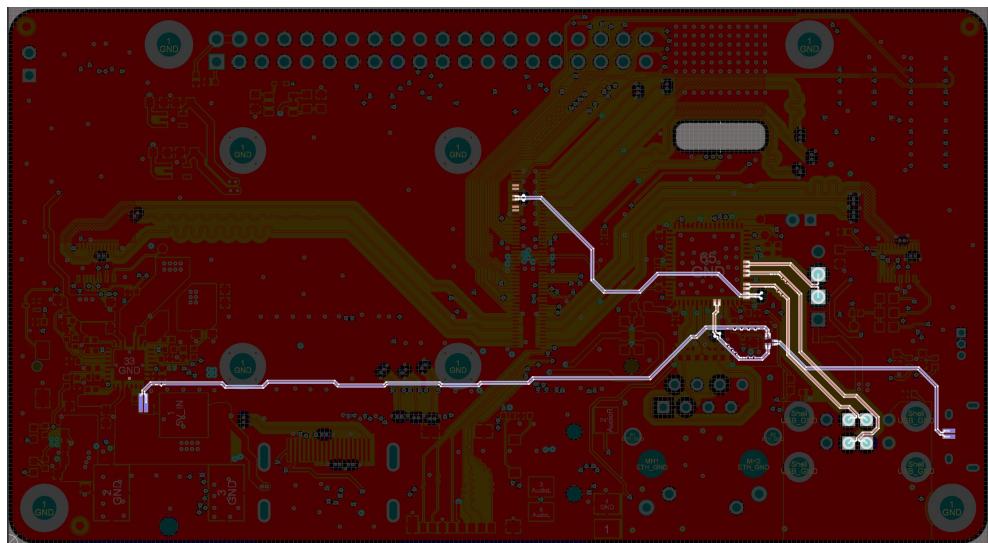
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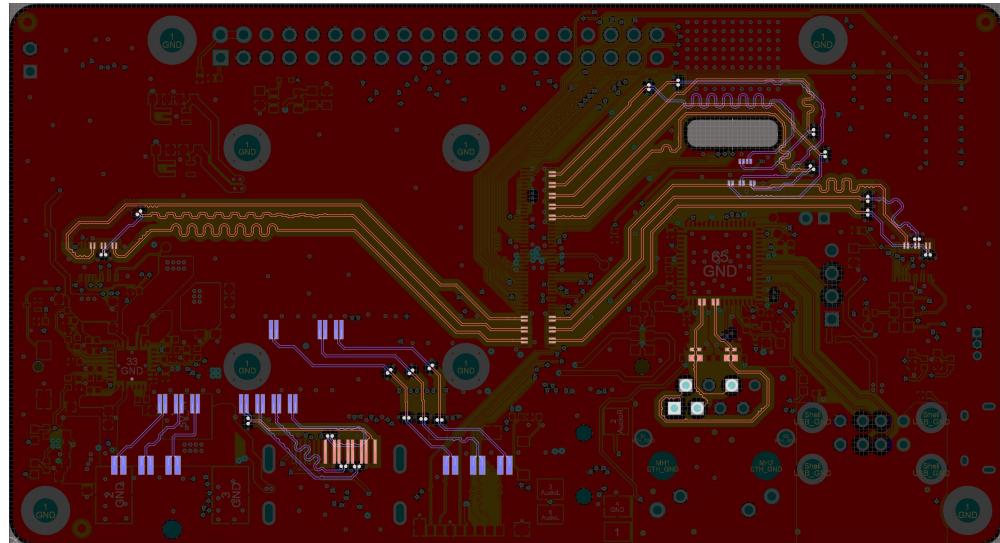
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90 OHM (+/-10%) DIFF PAIRS



100 OHM (+/-10%) DIFF PAIRS

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers	Substack
1	Edge-Coupled Coated Microstrip	100	99.68	Top Copper	0.10mm	0.10mm	0.13mm	Signal Layer 1	Board Layer Stack
2	Edge-Coupled Coated Microstrip	90	89.99	Top Copper	0.13mm	0.13mm	0.13mm	Signal Layer 1	Board Layer Stack
3	Edge-Coupled Coated Microstrip	100	99.68	Bottom Copper	0.10mm	0.10mm	0.13mm	Signal Layer 4	Board Layer Stack
4	Edge-Coupled Coated Microstrip	90	89.99	Bottom Copper	0.13mm	0.13mm	0.13mm	Signal Layer 4	Board Layer Stack

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