Birla Institute of Technology & Science, Pilani
Hyderabad Campus

SECOND SEMESTER 2024-2025

Course Handout Part II

Date: 06-01-2025

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : CS/ECE/EEE/INSTR F241
Course Title : Microprocessors and Interfacing
Instructor-in-Charge : Prof. Chetan Kumar V
Team of Lecture Instructors : Prof. Chetan Kumar V, Prof. Kanika Monga, Prof. Anakhi Hazarika.
Team of Tutorial Instructors : Prof. Soumya J, Prof. Subhradeep Pal, Prof. Chetan Kumar V, Prof. Kanika Monga, Prof. Anakhi Hazarika,
Team of Practical Instructors: Prof. Kanika Monga, Prof. Anakhi Hazarika,Dr. Ravikiran Yeleswarapu, Ms.Amrutha Lahari Sree Rama, Mr. Ritesh Kumar Singh, Mr. Gowthampolumati, Mr. Kurakula Anudeep, Ms. Vanmathi S, Ms. Keerthi C J, Mr. Sohel Siraj, Ms. Krishnapriya G B, Mr. Yuvraj Maphrio Mao, Ms. Thalla Narasimha Swetha, Ms. Isha Basumatary, Mr. Karri Y K G R Srinivasu, Ms. Abbidi Shivani Reddy, Mr. Nongthombam Joychandra Singh, Ms. Avula Brahma Tejaswini, Ms. M S Vaishnavi.

Scope and Objective of the Course:

The objective of this course is to become familiar with the processor internal architecture and its operation within the area of manufacturing and performance. This course will provide the instruction set of an Intel microprocessor 8086 – 80486, programmers model of processor, demonstration of the modular assembly programming using the various addressing modes, data transfer instructions, subroutines, macros etc.; Timing diagrams; Concept of interrupts: hardware & software interrupts, Interrupt handling techniques, Interrupt controllers; Types of Memory & memory interfacing; Programmable Peripheral devices and I/O Interfacing; DMA controller and its interfacing: Design of processor based system. This course familiarizes the students with the programming and interfacing of microprocessors, which will help in solving basic binary math operations using the microprocessor and provide a strong foundation for designing real world applications using microprocessors.

Textbooks:

1. **T1**: Barry B. Brey, The Intel Microprocessors: Architecture, Programming and Interfacing, Pearson, 8th Edition, 2009.

Reference books

1. **R1:** D. V. Hall, Microprocessor and Interfacing, Tata McGraw Hill, 2nd Edition.
2. **R2:** L. B. Das, The x86 Microprocessors, 2nd Edition, Pearson.

Course Plan:

Lec. No.	Learning objectives	Topics to be covered	Chapter in the Text Book
1	Introduction to microprocessor and microcomputers	Introduction to microprocessors, Historical background, Basics of computer architecture, Memory & I/O organization.	T1: Chap. 1 R1: Chap. 1
2-5	Architecture of 8086	Detailed architecture of 8086, Pin configurations of 8086, Modes of Operation, Clocking and Buses, Memory Banks	T1: Chap. 2 and 9 R1: Chap. 2
6-8	Assembly Language Programming: Part I	Addressing Modes, Data transfer, logical, arithmetic; Instruction formats	T1: Chap. 3
9-12	Assembly Language Programming: Part II	Instruction set of 8086: Data transfer, logical, arithmetic, flag manipulation, control transfer, rotate, string, processor control instructions. Instruction Formats	T1: Chap. 4-8 R2: Chap. 13
13-16	Assembly Language Programming: Part III	ALP Examples and practical examples of usage of 8086	T1: Chap. 4-8 R2: Chap. 14
17-20	Memory Interface	Pin configurations of 8086, Physical Memory Organization of 8086, Memory Devices, Address Decoding, Memory Interface: Interfacing RAM and EPROM using logic gates/ decoder ICs.	T1: Chap. 10 R2: Chap.16
21-24	I/O Interface	Basic I/O, I/O Instructions, I/O mapped and memory mapped I/O, Interfacing with 8-bit I/O devices, I/O port address decoding	T1: Chap. 11 R2: Chap. 16
25-28	Interrupts	Types of 8086 interrupts, vector table, priority among 8086 interrupts, interrupt service routine, practical examples	T1: Chap. 12 R2: Chap. 15
29-34	Programmable Peripheral Devices	8255: General purpose PPI 8254: Programmable Interval Controller 8259: Programmable Interrupt Controller ADCs and DACs	T1: Chap. 11 T1: Chap. 12
35-37	DMA Controller	8237: Basic Operation, Pin Details, Features, Architecture, DMA Initialization, Operation with 8086	T1: Chap. 13 R2: Chap. 7
38	Bus Interface	ISA, PCI, USB etc	T1: Chap. 15
39	System Design	Processor based System Design	T1: Chapter 15
40	Advanced Processor Part I	80286-80486	T1: Chap. 16,17 R1: Chap. 15,16

Evaluation Scheme:

Sl. No.	Component	Duration	Weightage (%)	Marks	Date & Time	Nature of Component
1.	Mid-Term Examination	90 mins.	25%	75	04/03 4.00 - 05.30PM	Closed Book
2.	Tutorial Evaluations (Quizzes)	TBA	10%	30	TBA	Open Book
3.	Regular Lab Evaluations	120 mins. / week	15%	45	As per timetable	Open Book
4.	Lab Exam	TBA	10%	30	TBA	Closed Book
5.	Comprehensive Examination	3 hours	40%	120	05/05AN	Closed Book

Minimum Criterion for awarding valid grade:
A student should obtain 10% of the maximum marks to clear the course and get a valid grade. If any student gets the marks lower than the prescribed standard mentioned above, he/she may be awarded NC.

Chamber Consultation Hour: This will be announced in the class.

Notices: All notices will be displayed via LMS only.

Make-up Policy:

1. **Regular lab evaluations will strictly follow the (n-1) scheme.**
2. **The Tutorial evaluations (quizzes) will be conducted in every alternative tutorials. Theis component will strictly follow (n-2) scheme.**
3. **The course will follow a zero-make-up policy for the tutorial evaluations (quizzes) and regular lab evaluations.**
4. **Makeup will be allowed for mid-term and end-term examinations only on the basis of genuine medical grounds with prior intimation and proper submission of correct and necessary documents.**

Academic Honesty and Integrity Policy:

Academic honesty and integrity are to be maintained by all the students throughout the semester; no academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE
Chetan Kumar V