11주차

2016. 11. 09.

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- 실험 – 외부 인터럽트 와 LED 제어 실습
- 레포트

후반부 강의 계획

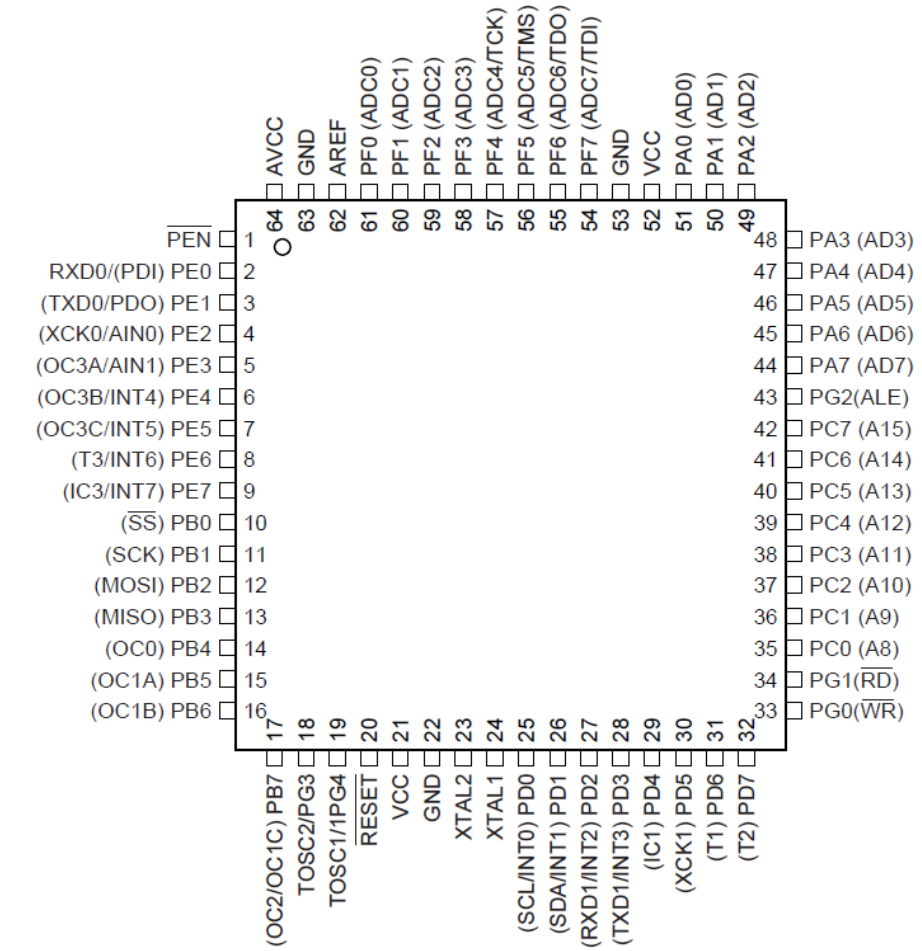
9	마이크로프로세서 개요1 C언어	C언어 강의	보드 납땜 (컨트롤러부, LED)
10	마이크로프로세서 개요2 GPIO 1	마이크로프로세서란? Atmega128의 구조와 기능 Firmware ? GPIO ? LED 제어	C언어 Quiz
11	Interrupt GPIO 2	Interrupt 이해 및 실습	C언어 Quiz
12	타이머/카운터	타이머/카운터 이해 및 실습 + LED	C언어 Quiz
13	주변장치 제어1	인터럽트와 4x4 keypad 제어	4x4 Keypad
14	주변장치 제어2	인터럽트와 타이머/카운터를 이용한 7-Segment 제어	7-Segment
15	주변장치 제어3	디지털 시계 / 스톱워치	
16	기말고사	기말고사 (이론 + 실기)	

ATMEGA128의 주요 특징

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 128K Bytes of In-System Reprogrammable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 4K Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 4K Bytes Internal SRAM
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
  - Output Compare Modulator
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega128L
  - 4.5 - 5.5V for ATmega128
- Speed Grades
  - 0 - 8 MHz for ATmega128L
  - 0 - 16 MHz for ATmega128

Figure 1. Pinout ATmega128



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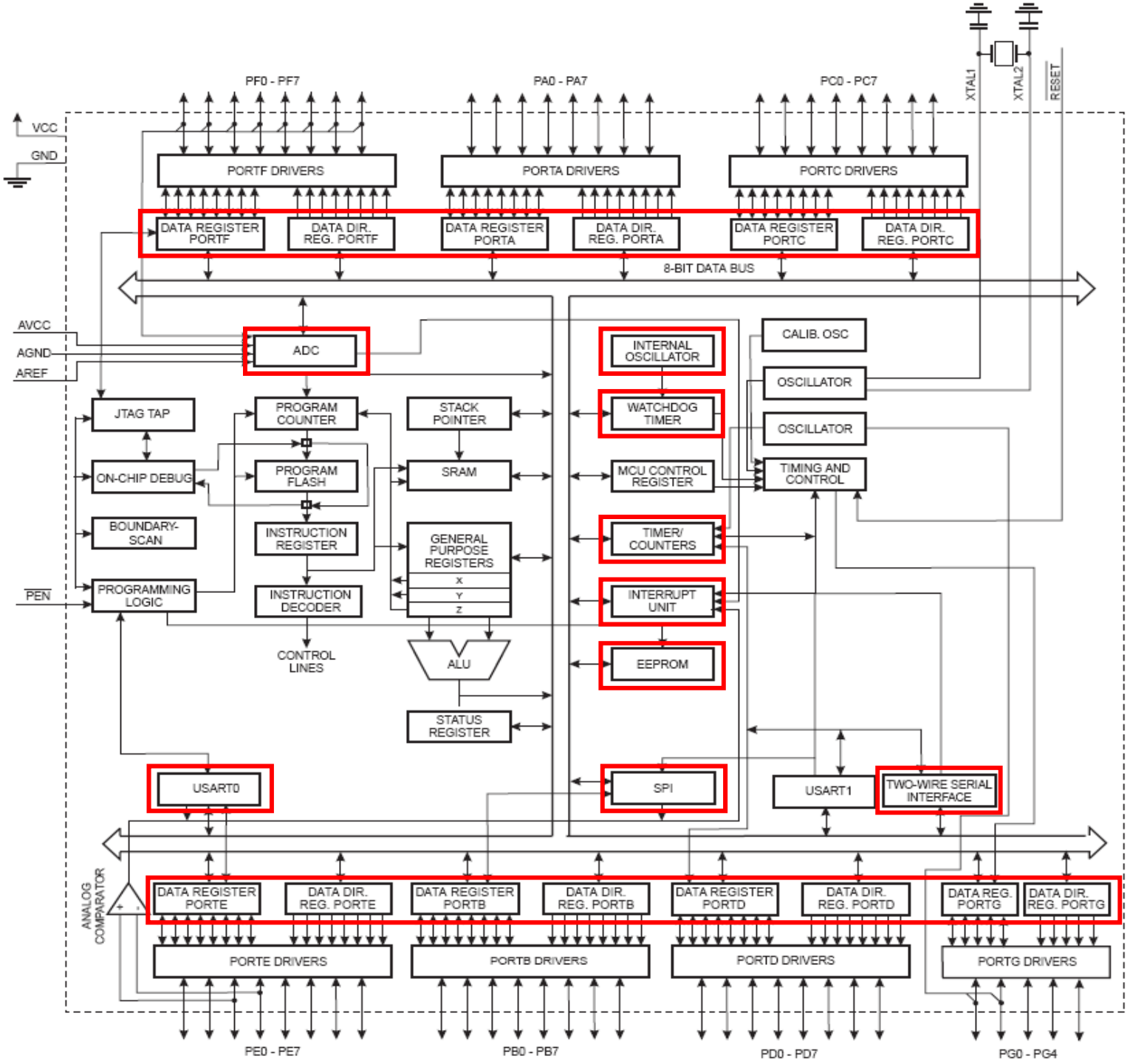
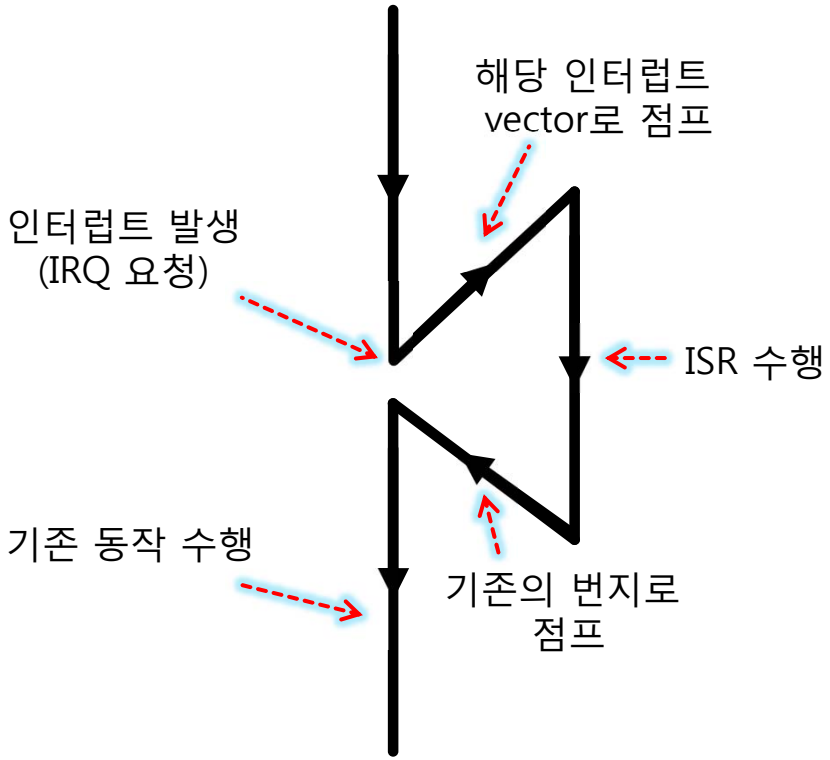

PF0 - PF7
PA0 - PA7
PC0 - PC7
XTAL1
XTAL2
RESET
VCC
GND
PORTF DRIVERS
PORTA DRIVERS
PORTC DRIVERS
DATA REGISTER PORTF
DATA DIR. REG. PORTF
DATA REGISTER PORTA
DATA DIR. REG. PORTA
DATA REGISTER PORTC
DATA DIR. REG. PORTC
8-BIT DATA BUS
AVCC
AGND
AREF
ADC
INTERNAL OSCILLATOR
CALIB. OSC
OSCILLATOR
OSCILLATOR
JTAG TAP
PROGRAM COUNTER
STACK POINTER
WATCHDOG TIMER
ON-CHIP DEBUG
PROGRAM FLASH
SRAM
MCU CONTROL REGISTER
TIMING AND CONTROL
BOUNDARY-SCAN
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTERS
X
Y
Z
TIMER/ COUNTERS
PEN
PROGRAMMING LOGIC
INSTRUCTION DECODER
INTERRUPT UNIT
CONTROL LINES
ALU
EEPROM
STATUS REGISTER
USART0
SPI
USART1
TWO-WIRE SERIAL INTERFACE
ANALOG COMPARATOR
DATA REGISTER PORTE
DATA DIR. REG. PORTE
DATA REGISTER PORTB
DATA DIR. REG. PORTB
DATA REGISTER PORTD
DATA DIR. REG. PORTD
DATA REG. PORTG
DATA DIR. REG. PORTG
PORTE DRIVERS
PORTB DRIVERS
PORTD DRIVERS
PORTG DRIVERS
PE0 - PE7
PB0 - PB7
PD0 - PD7
PG0 - PG4

인터럽트 (Interrupt)

- 주변장치의 service 요청에 CPU가 가장 빠르게 대응할 수 있는 방법
  : 주변장치의 service 발생 시기를 예측하기 어려운 비동기적인 event에 대한 효율적 처리 방법



단일 인터럽트의 동작 개념

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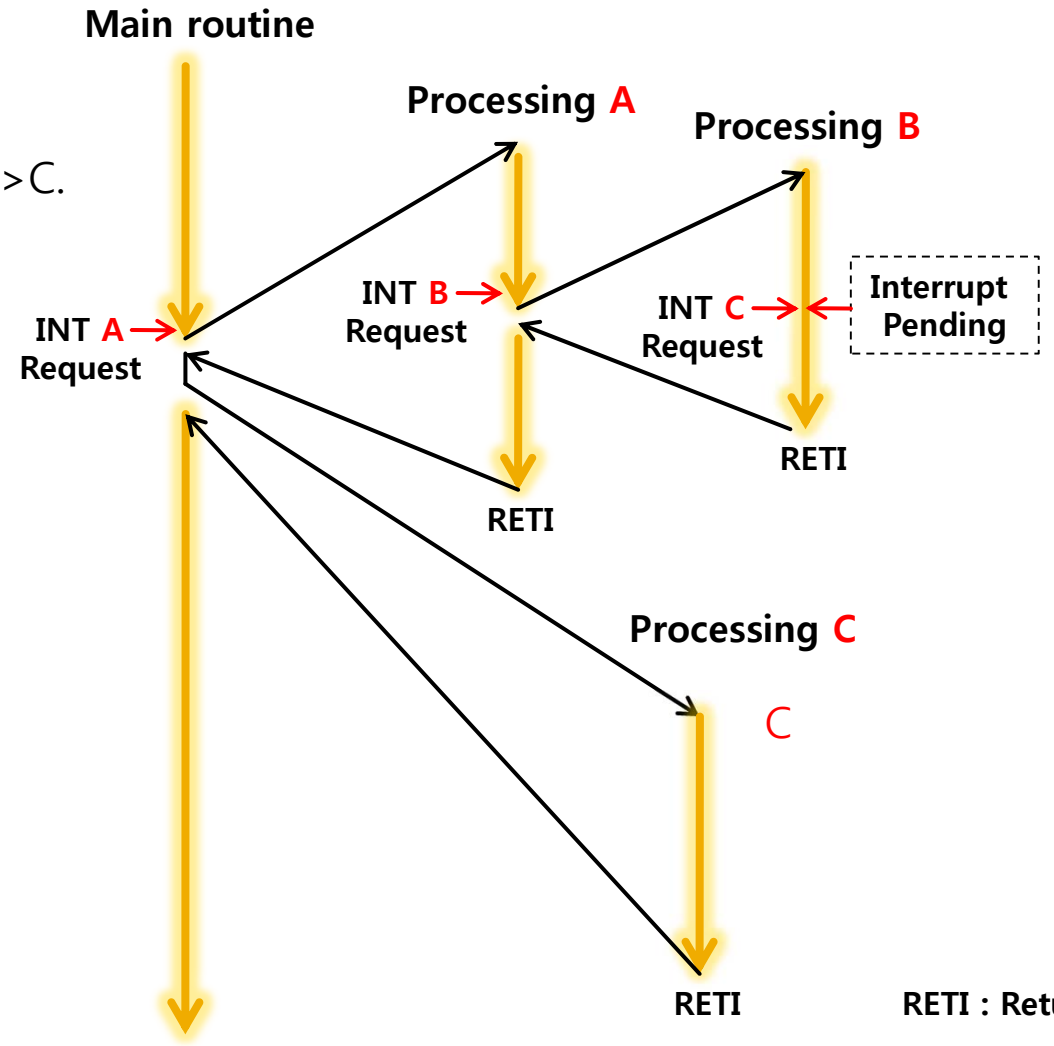
다중 인터럽트 발생 (Multiple interrupt processing)

Where priority is B>A>C.



다중 인터럽트의 동작 개념

- 벡터(vector)형

: IRQ발생시 해당 IRQ의 ISR의 시작 번지(vector)를 CPU에 전송

① 인터럽트의 응답시간이 빠르다.
② 주변장치의 개수와 상관없다.
③ 우선순위는 고정된다.
④ 대부분이 이 방식을 채택하고 있다.

- 조사(polling)형

: IRQ발생시 이것이 어떤 주변장치로부터 발생했는지 각 주변 장치를 소프트웨어적으로 조사(polling)하고 처리하는 방법

① 검출은 특정 레지스터의 비트를 scan한다.
② 주변장치수가 많아지면 응답시간이 느려질 수 있다.
③ 우선순위는 polling순서에 의하므로 소프트웨어 적임 (즉, 가변 가능).

인터럽트 벡터 테이블(Interrupt Vector Table)

- AVR 계열의 인터럽트 처리 방식은 인터럽트 이벤트에 분기하여 실행할 어드레스를 미리 테이블에 저장하는 벡터방식.
- ATmega128의 인터럽트 벡터 테이블

Table 23. Reset and Interrupt Vectors

Vector No.	Program Address(2)	Source	Interrupt Definition
1	$0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	$0002	INT0	External Interrupt Request 0
3	$0004	INT1	External Interrupt Request 1
4	$0006	INT2	External Interrupt Request 2
5	$0008	INT3	External Interrupt Request 3
6	$000A	INT4	External Interrupt Request 4
7	$000C	INT5	External Interrupt Request 5
8	$000E	INT6	External Interrupt Request 6
9	$0010	INT7	External Interrupt Request 7
10	$0012	TIMER2 COMP	Timer/Counter2 Compare Match
11	$0014	TIMER2 OVF	Timer/Counter2 Overflow
12	$0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	$0018	TIMER1 COMPA	Timer/Counter1 Compare Match A
14	$001A	TIMER1 COMPB	Timer/Counter1 Compare Match B
15	$001C	TIMER1 OVF	Timer/Counter1 Overflow
16	$001E	TIMER0 COMP	Timer/Counter0 Compare Match
17	$0020	TIMER0 OVF	Timer/Counter0 Overflow
18	$0022	SPI, STC	SPI Serial Transfer Complete
19	$0024	USART0, RX	USART0, Rx Complete
20	$0026	USART0, UDRE	USART0 Data Register Empty
21	$0028	USART0, TX	USART0, Tx Complete
22	$002A	ADC	ADC Conversion Complete
23	$002C	EE READY	EEPROM Ready
24	$002E	ANALOG COMP	Analog Comparator
25	$0030(3)	TIMER1 COMPC	Timer/Countre1 Compare Match C
26	$0032(3)	TIMER3 CAPT	Timer/Counter3 Capture Event
27	$0034(3)	TIMER3 COMPA	Timer/Counter3 Compare Match A
28	$0036(3)	TIMER3 COMPB	Timer/Counter3 Compare Match B
29	$0038(3)	TIMER3 COMPC	Timer/Counter3 Compare Match C
30	$003A(3)	TIMER3 OVF	Timer/Counter3 Overflow

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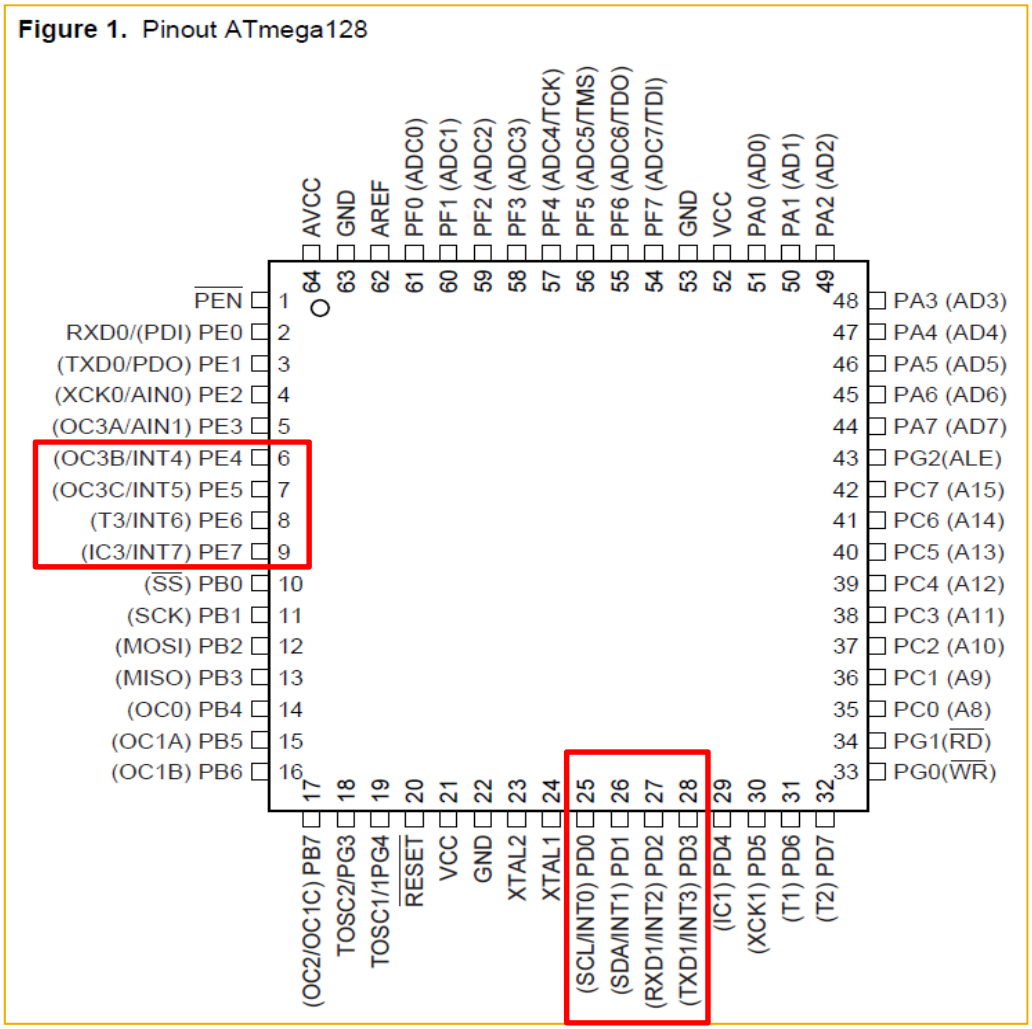
외부 인터럽트 (External interrupt)



External interrupt pins

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PORTs Alternate functions

Table 27. Port A Pins Alternate Functions

Port Pin	Alternate Function
PA7	AD7 (External memory interface address and data bit 7)
PA6	AD6 (External memory interface address and data bit 6)
PA5	AD5 (External memory interface address and data bit 5)
PA4	AD4 (External memory interface address and data bit 4)
PA3	AD3 (External memory interface address and data bit 3)
PA2	AD2 (External memory interface address and data bit 2)
PA1	AD1 (External memory interface address and data bit 1)
PA0	AD0 (External memory interface address and data bit 0)

Table 30. Port B Pins Alternate Functions

Port Pin	Alternate Functions
PB7	OC2/OC1C(1) (Output Compare and PWM Output for Timer/Counter2 or Output Compare and PWM Output C for Timer/Counter1)
PB6	OC1B (Output Compare and PWM Output B for Timer/Counter1)
PB5	OC1A (Output Compare and PWM Output A for Timer/Counter1)
PB4	OC0 (Output Compare and PWM Output for Timer/Counter0)
PB3	MISO (SPI Bus Master Input/Slave Output)
PB2	MOSI (SPI Bus Master Output/Slave Input)
PB1	SCK (SPI Bus Serial Clock)
PB0	$\overline{SS}$ (SPI Slave Select input)

Table 33. Port C Pins Alternate Functions

Port Pin	Alternate Function
PC7	A15
PC6	A14
PC5	A13
PC4	A12
PC3	A11
PC2	A10
PC1	A9
PC0	A8

Table 36. Port D Pins Alternate Functions

Port Pin	Alternate Function
PD7	T2 (Timer/Counter2 Clock Input)
PD6	T1 (Timer/Counter1 Clock Input)
PD5	XCK1(1) (USART1 External Clock Input/Output)
PD4	IC1 (Timer/Counter1 Input Capture Trigger)
PD3	INT3/TXD1(1) (External Interrupt3 Input or UART1 Transmit Pin)
PD2	INT2/RXD1(1) (External Interrupt2 Input or UART1 Receive Pin)
PD1	INT1/SDA(1) (External Interrupt1 Input or TWI Serial DAta)
PD0	INT0/SCL(1) (External Interrupt0 Input or TWI Serial CLock)

Table 39. Port E Pins Alternate Functions

Port Pin	Alternate Function
PE7	INT7/IC3[1] (External Interrupt 7 Input or Timer/Counter3 Input Capture Trigger)
PE6	INT6/ T3[1] (External Interrupt 6 Input or Timer/Counter3 Clock Input)
PE5	INT5/OC3C[1] (External Interrupt 5 Input or Output Compare and PWM Output C for Timer/Counter3)
PE4	INT4/OC3B[1] (External Interrupt4 Input or Output Compare and PWM Output B for Timer/Counter3)
PE3	AIN1/OC3A [1] (Analog Comparator Negative Input or Output Compare and PWM Output A for Timer/Counter3)
PE2	AIN0/XCK0[1] (Analog Comparator Positive Input or USART0 external clock input/output)
PE1	PDO/TXD0 (Programming Data Output or UART0 Transmit Pin)
PE0	PDI/RXD0 (Programming Data Input or UART0 Receive Pin)

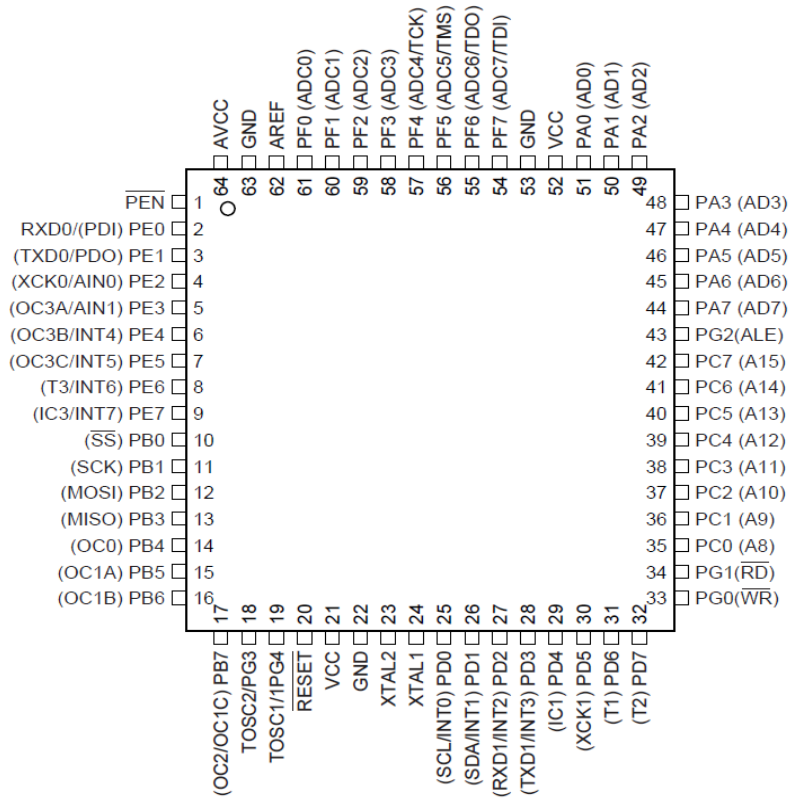
Table 42. Port F Pins Alternate Functions

Port Pin	Alternate Function
PF7	ADC7/TDI (ADC input channel 7 or JTAG Test Data Input)
PF6	ADC6/TDO (ADC input channel 6 or JTAG Test Data Output)
PF5	ADC5/TMS (ADC input channel 5 or JTAG Test Mode Select)
PF4	ADC4/TCK (ADC input channel 4 or JTAG Test ClocK)
PF3	ADC3 (ADC input channel 3)
PF2	ADC2 (ADC input channel 2)
PF1	ADC1 (ADC input channel 1)
PF0	ADC0 (ADC input channel 0)

Table 45. Port G Pins Alternate Functions

Port Pin	Alternate Function
PG4	TOSC1 (RTC Oscillator Timer/Counter0)
PG3	TOSC2 (RTC Oscillator Timer/Counter0)
PG2	ALE (Address Latch Enable to external memory)
PG1	$\overline{RD}$ (Read strobe to external memory)
PG0	$\overline{WR}$ (Write strobe to external memory)

Figure 1. Pinout ATmega128



- External Interrupt Control Register A / B

Bit	7	6	5	4	3	2	1	0	
	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

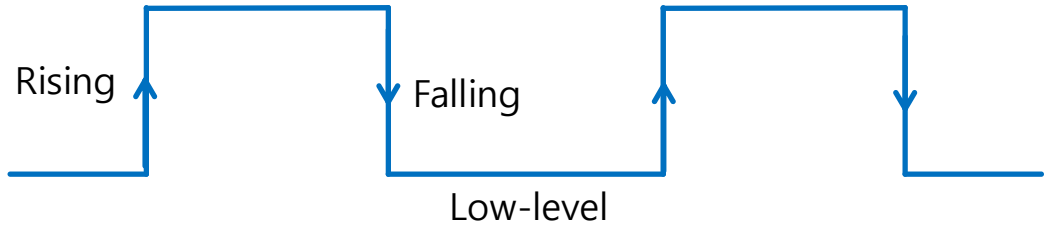
Table 48. Interrupt Sense Control(1)

ISCn1	ISCn0	Description
0	0	The low level of INTn generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INTn generates asynchronously an interrupt request.
1	1	The rising edge of INTn generates asynchronously an interrupt request.

Bit	7	6	5	4	3	2	1	0	
	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	EICRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 50. Interrupt Sense Control(1)

ISCn1	ISCn0	Description
0	0	The low level of INTn generates an interrupt request.
0	1	Any logical change on INTn generates an interrupt request
1	0	The falling edge between two samples of INTn generates an interrupt request.
1	1	The rising edge between two samples of INTn generates an interrupt request.



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- External Interrupt Mask Register (EMISK)

Bit	7	6	5	4	3	2	1	0	
	INT7	INT6	INT5	INT4	INT3	INT2	INT1	IINT0	EIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- External Interrupt Flag Register (EIFR)

Bit	7	6	5	4	3	2	1	0	
	INTF7	INTF6	INTF5	INTF4	INTF3	INTF2	INTF1	IINTF0	EIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Status Register (SREG)

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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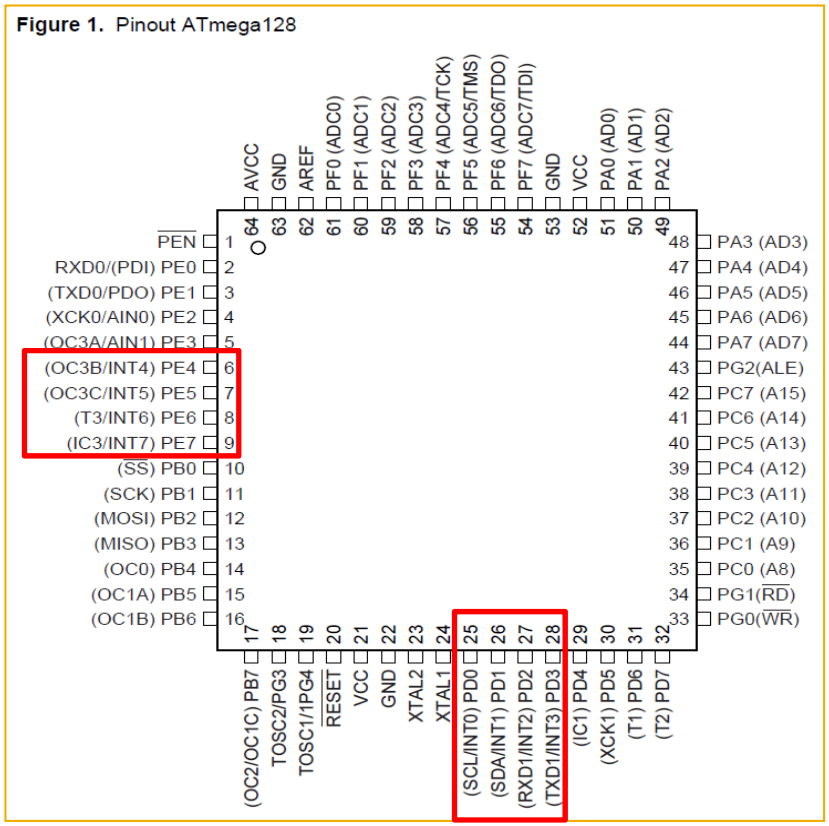
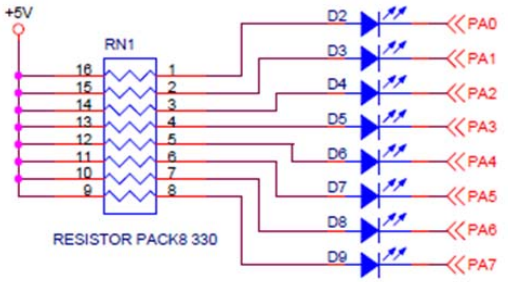
Experiments – External Interrupt & LED

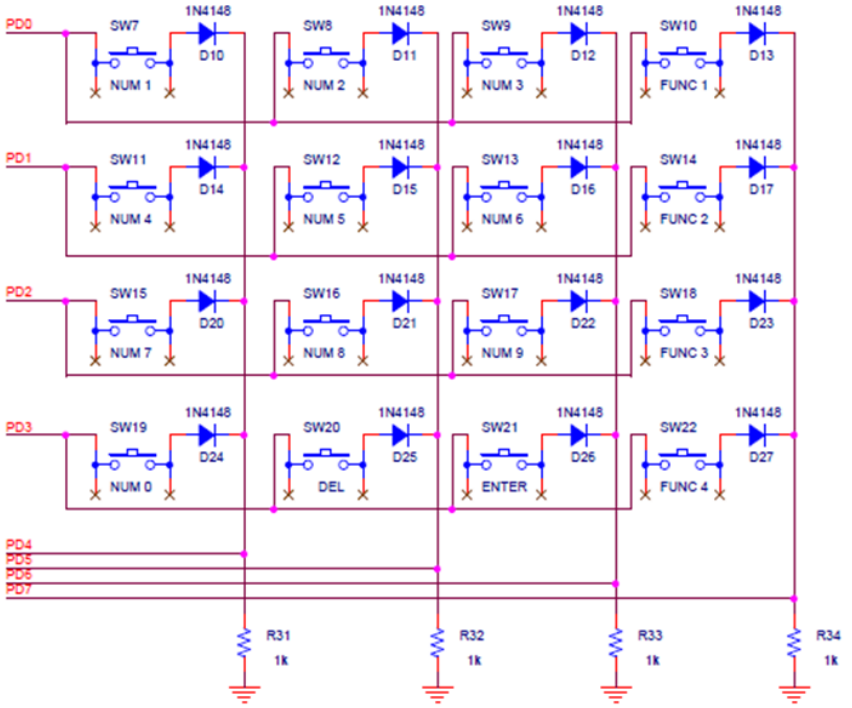
- 실험 전 절차

1. 외부 인터럽트 실습을 위하여 스위치는 SW7, SW8, R31, R32 만 납땜할 것
2. Chapter 5 의 예제 1, 3, 4 실습 시 Main board 의
   PD4 와 PE4 를 서로 연결할 것 그리고 PD5 와 PE5 도 서로 연결할 것





KEY-PAD



- **실습 (오실로스코프 확인 필수!!!)**

1. 지난 시간 예제
   1-1. LED 전체를 1초씩 점멸
   1-2. 켜져 있는 LED 1개를 위쪽으로 이동 , 이동시간은 0.5초
   (위쪽 끝 도달 이후 아래쪽 부터 순환반복)
   1-2. 꺼져 있는 LED 1개를 아래쪽으로 이동, 이동시간은 0.4초
   (아래쪽 끝 도달 이후 위쪽 부터 순환반복)
   1-3. 아래쪽 LED 4개가 ON 일 때 위쪽 LED 4개는 OFF 점멸시간은 각 1초
   1-4. 켜져 있는 LED 1개가 맨 아래쪽 부터 시작하여, 맨 위쪽으로 움직이면
   다시 아래로 움직이고 이를 반복, 이동시간은 0.6초

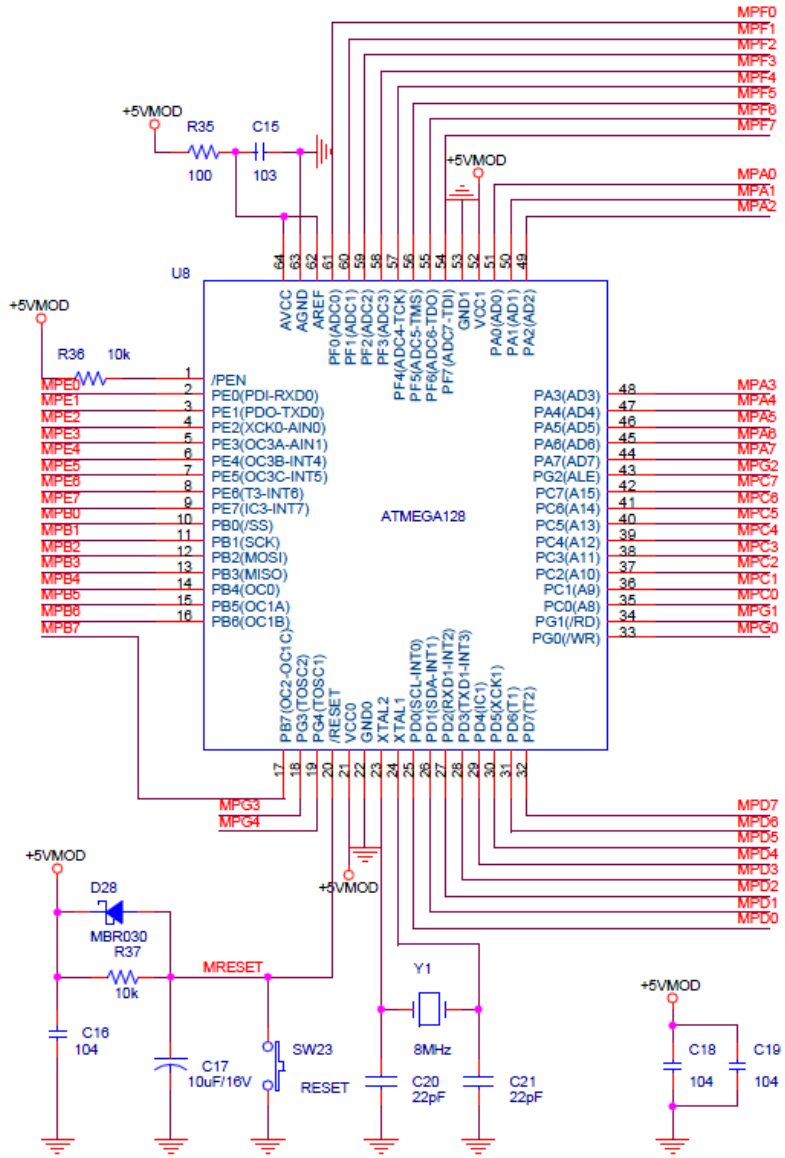
2. 자신만의 LED ON/OFF idea를 구현...

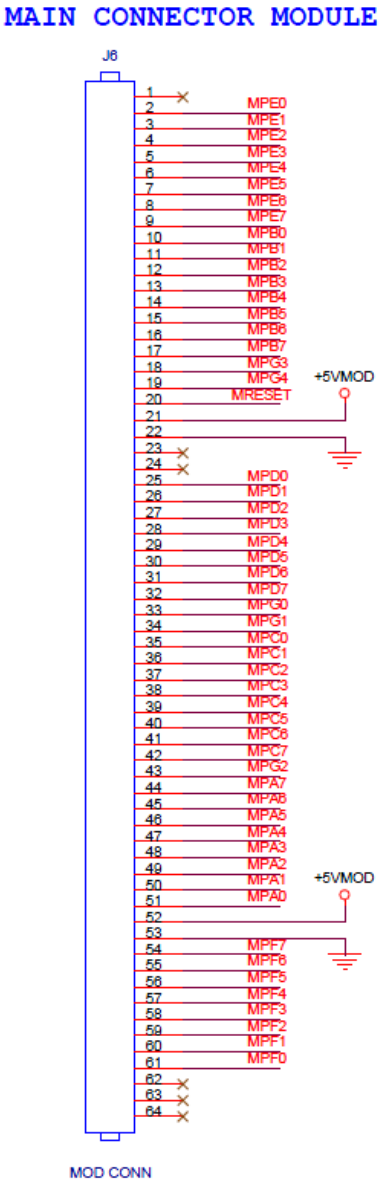
3. Chapter 4 예제 1~5

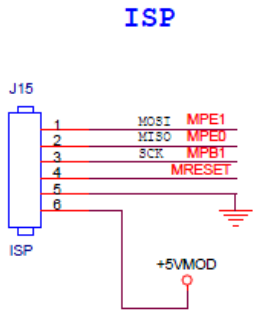
4. Chapter 5 예제 1, 3, 4

★반드시 코드를 이해하고 오실로스코프를 통하여 확인할 것!!!

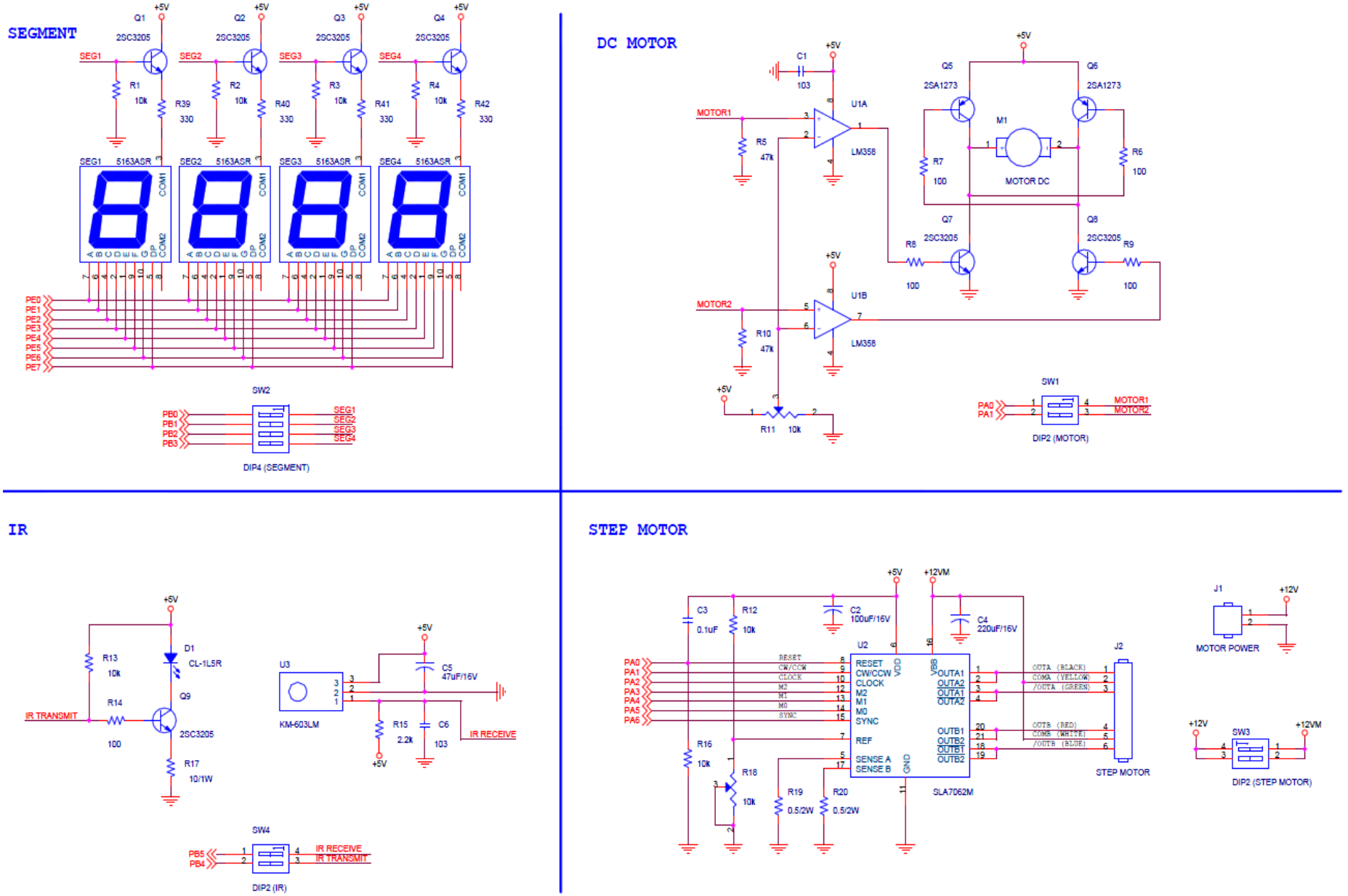
실험 Control Board



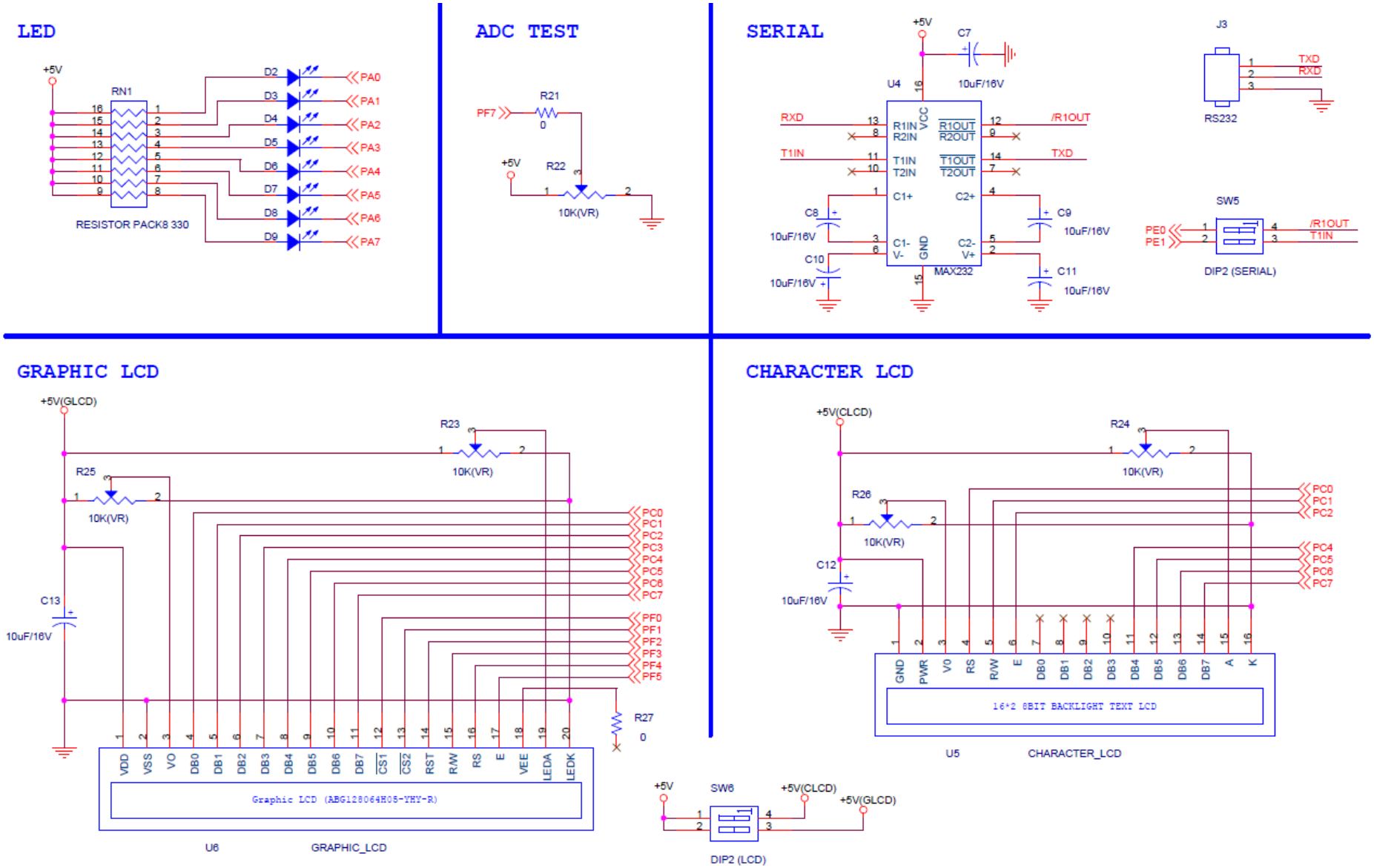




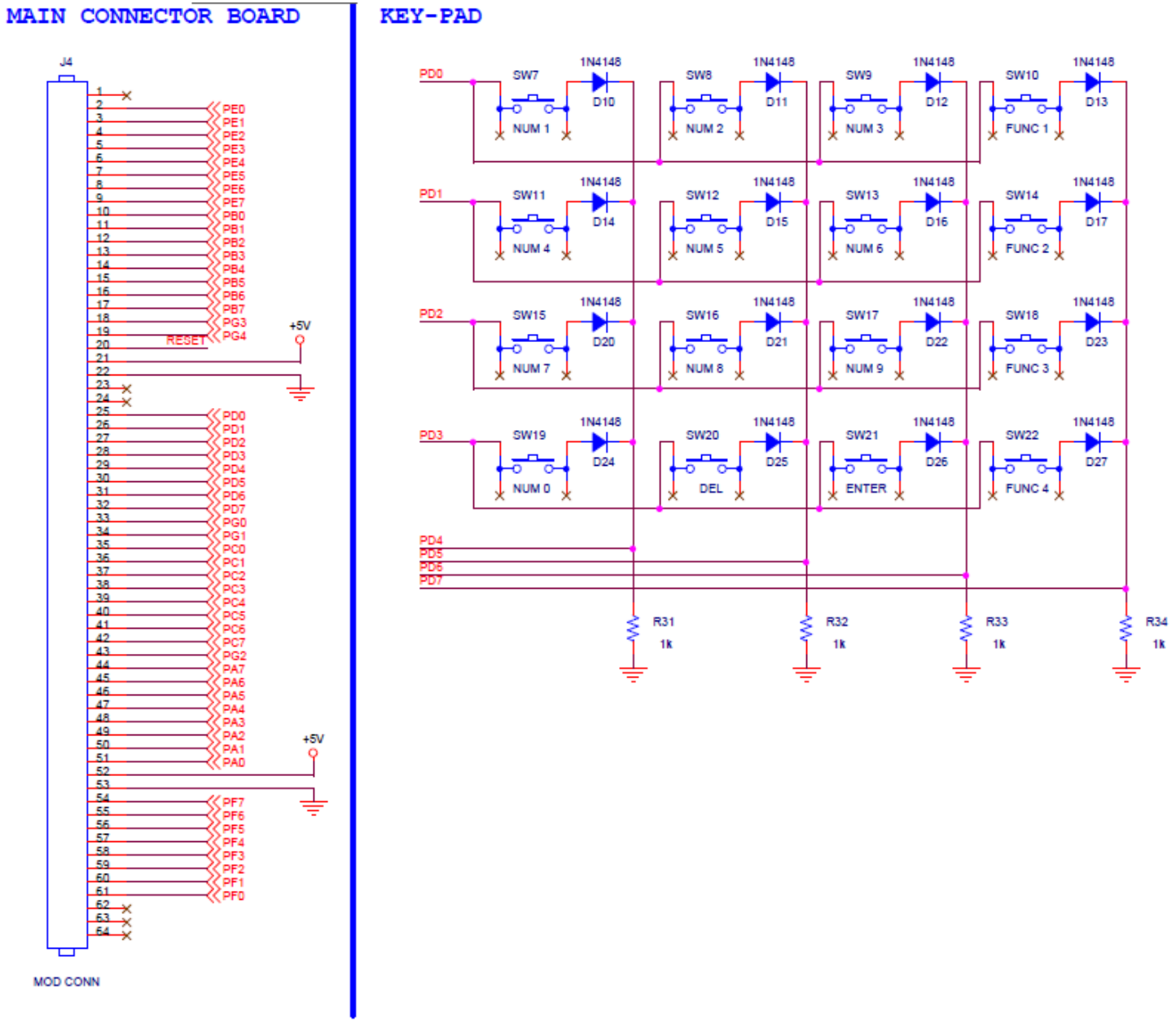
실험 Main Board 1



실험 Main Board 2



실험 Main Board 3



레포트

1. 실습 예제 구현

2. C언어 퀴즈 준비

3. 인터럽트에 대한 복습

4. Pulse Width Modulation (PWM)이란?

5. - Atmega8의 Timer / Counter 0와 1에 대하여 조사
   - Timer 란? Counter 란?
   - 4가지 동작 모드에 대하여 요약 정리

(Normal Mode, CTC Mode, Phase Correct PWM Mode, Phase and frequency correct PWM Mode)