15주차

2015. 12. 9.

후반부 강의 계획

9	마이크로프로세서 개요1 C언어	C언어 강의	보드 납땜 (컨트롤러부, LED)
10	마이크로프로세서 개요2 GPIO 1	마이크로프로세서란? Atmega128의 구조와 기능 Firmware ? GPIO ? LED 제어	C언어 Quiz
11	Interrupt GPIO 2	Interrupt 이해 및 실습	C언어 Quiz
12	타이머/카운터	타이머/카운터 이해 및 실습 + LED	C언어 Quiz
13	주변장치 제어1	인터럽트와 4x4 keypad 제어	4x4 Keypad
14	주변장치 제어2	인터럽트와 타이머/카운터를 이용한 7-Segment 제어	7-Segment
15	주변장치 제어3	디지털 시계 / 스톱워치	7-Segment + 4x4 Keypad
16	기말고사	기말고사 (실기)	

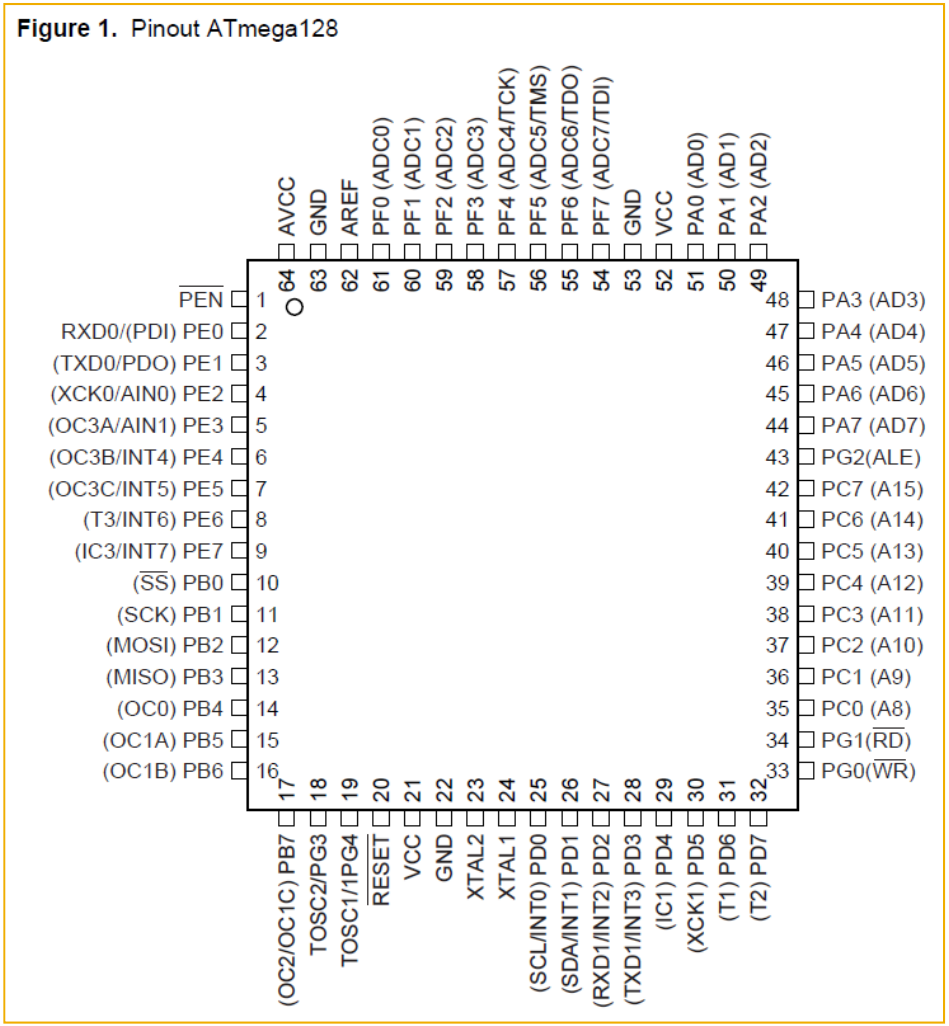
ATMEGA128의 주요 특징

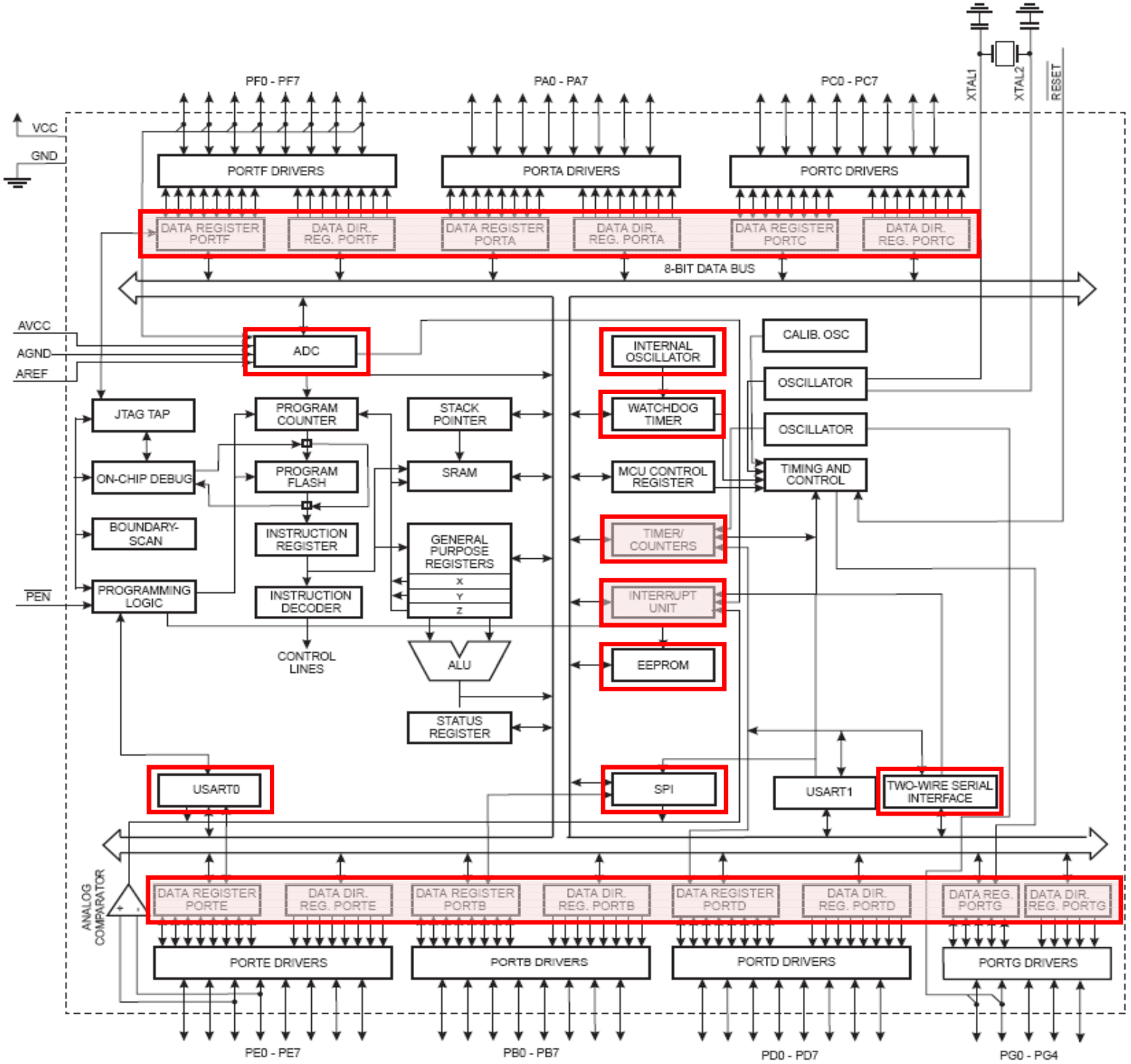
- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 128K Bytes of In-System Reprogrammable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 4K Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 4K Bytes Internal SRAM
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
  - Output Compare Modulator
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega128L
  - 4.5 - 5.5V for ATmega128
- Speed Grades
  - 0 - 8 MHz for ATmega128L
  - 0 - 16 MHz for ATmega128

교재 15-20 페이지 참고

Figure 1. Pinout ATmega128




PF0 - PF7
PA0 - PA7
PC0 - PC7
XTAL1
XTAL2
RESET
VCC
GND
PORTF DRIVERS
PORTA DRIVERS
PORTC DRIVERS
DATA REGISTER PORTF
DATA DIR. REG. PORTF
DATA REGISTER PORTA
DATA DIR. REG. PORTA
DATA REGISTER PORTC
DATA DIR. REG. PORTC
8-BIT DATA BUS
AVCC
AGND
AREF
ADC
INTERNAL OSCILLATOR
CALIB. OSC
OSCILLATOR
OSCILLATOR
JTAG TAP
PROGRAM COUNTER
STACK POINTER
WATCHDOG TIMER
ON-CHIP DEBUG
PROGRAM FLASH
SRAM
MCU CONTROL REGISTER
TIMING AND CONTROL
BOUNDARY-SCAN
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTERS
X
Y
Z
TIMER/ COUNTERS
PEN
PROGRAMMING LOGIC
INSTRUCTION DECODER
INTERRUPT UNIT
CONTROL LINES
ALU
EEPROM
STATUS REGISTER
USART0
SPI
USART1
TWO-WIRE SERIAL INTERFACE
ANALOG COMPARATOR
DATA REGISTER PORTE
DATA DIR. REG. PORTE
DATA REGISTER PORTB
DATA DIR. REG. PORTB
DATA REGISTER PORTD
DATA DIR. REG. PORTD
DATA REG. PORTG
DATA DIR. REG. PORTG
PORTE DRIVERS
PORTB DRIVERS
PORTD DRIVERS
PORTG DRIVERS
PE0 - PE7
PB0 - PB7
PD0 - PD7
PG0 - PG4

System Reset

- Power on Reset, External Reset, Brown Out Reset, Watch Dog Reset

Figure 22. Reset Logic

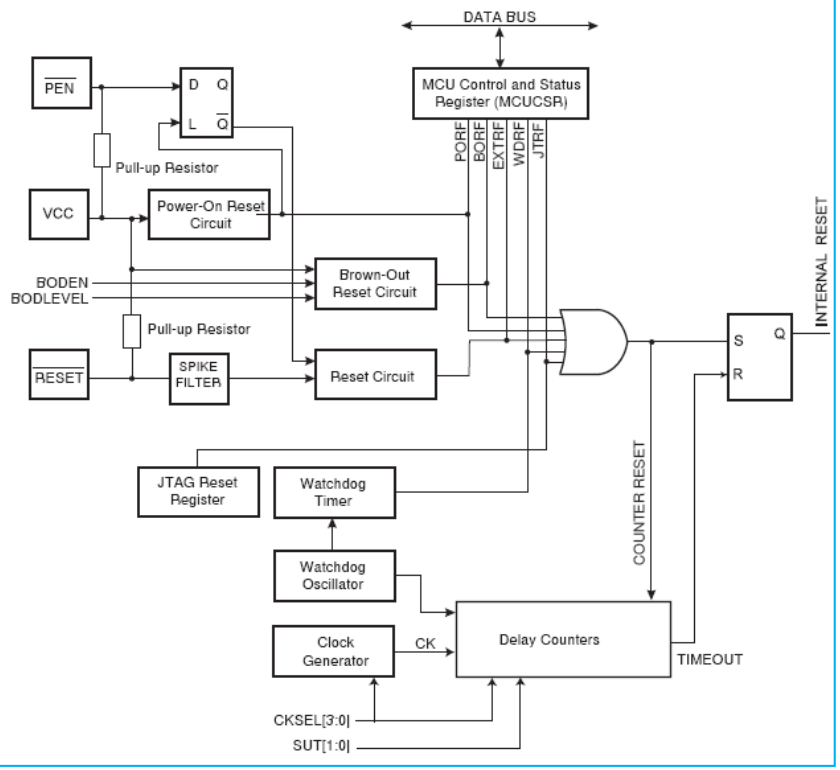


Table 19. Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT}	Power-on Reset Threshold Voltage (rising)			1.4	2.3	V
	Power-on Reset Threshold Voltage (falling)(1)			1.3	2.3	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.2 V_{CC}		0.85 V_{CC}	V
t_{RST}	Minimum pulse width on $\overline{\text{RESET}}$ Pin			50		ns
V_{BOT}	Brown-out Reset Threshold Voltage(2)	BODLEVEL = 1	2.5	2.7	3.2	V
		BODLEVEL = 0	3.7	4.0	4.5	
t_{BOD}	Minimum low voltage period for Brown-out Detection	BODLEVEL = 1		2		µs
		BODLEVEL = 0		2		µs
V_{HYST}	Brown-out Detector hysteresis			50		mV

Notes: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling)

- Power on Reset (POR)

Figure 23. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}.

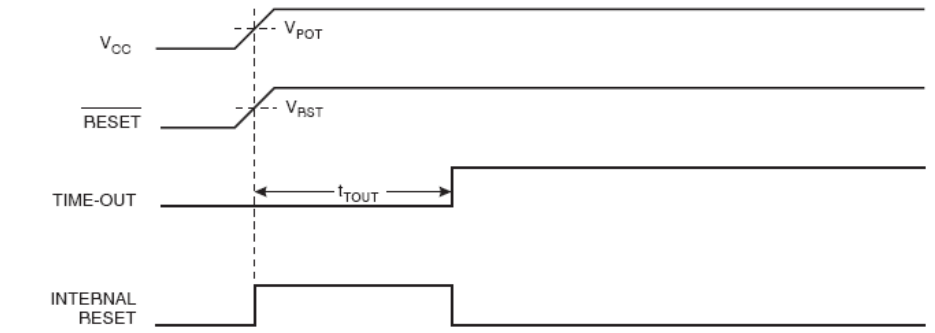
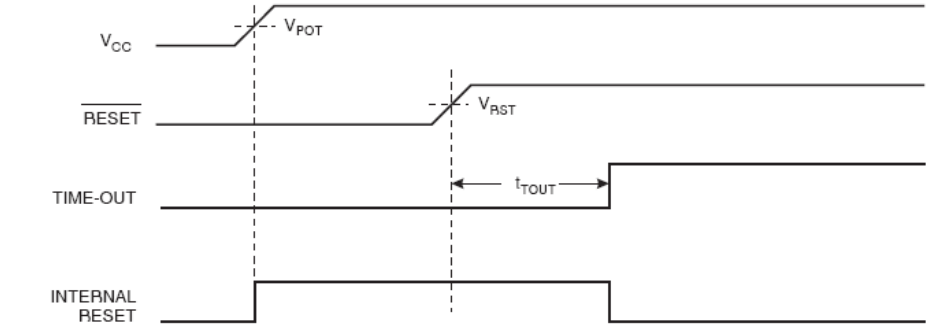
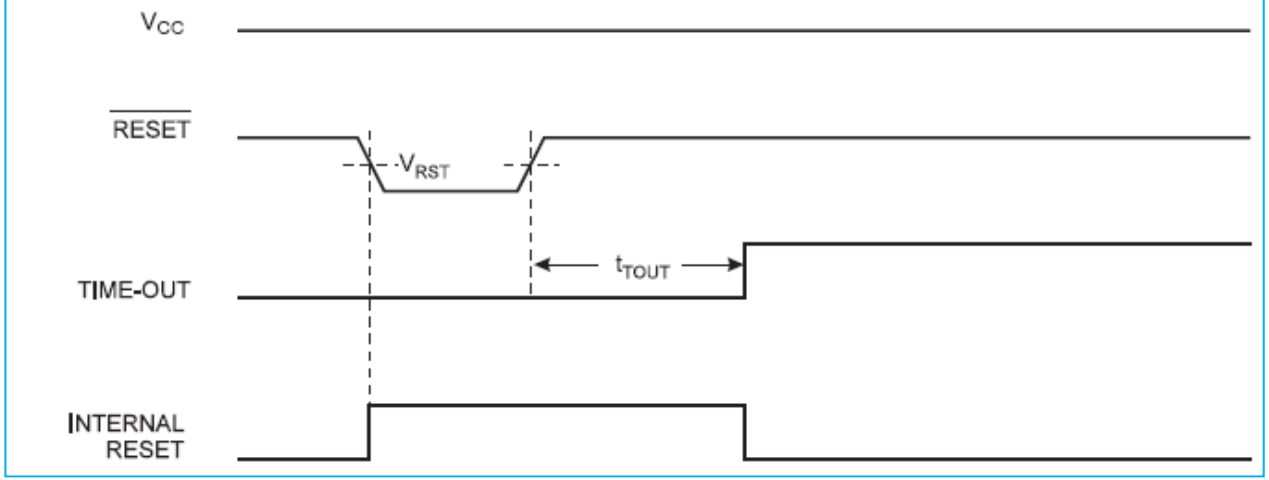


Figure 24. MCU Start-up, $\overline{\text{RESET}}$ Extended Externally



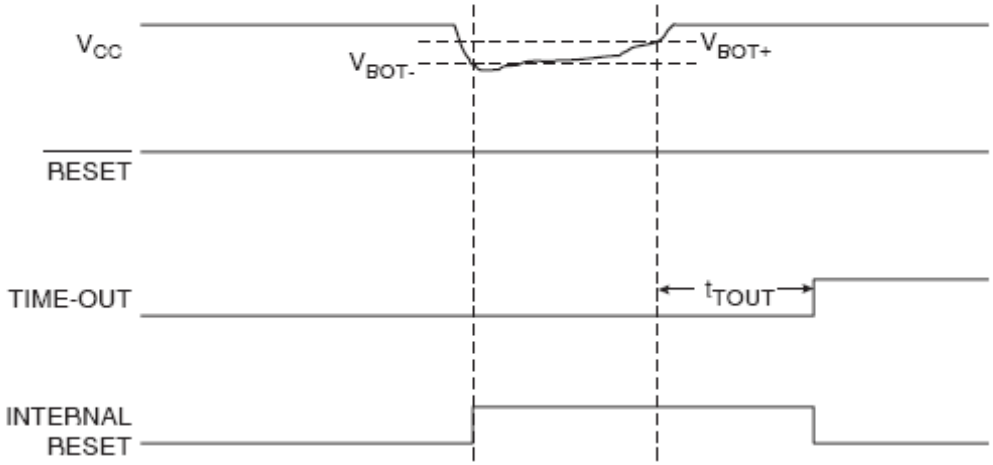
- External Reset

Figure 25. External Reset During Operation



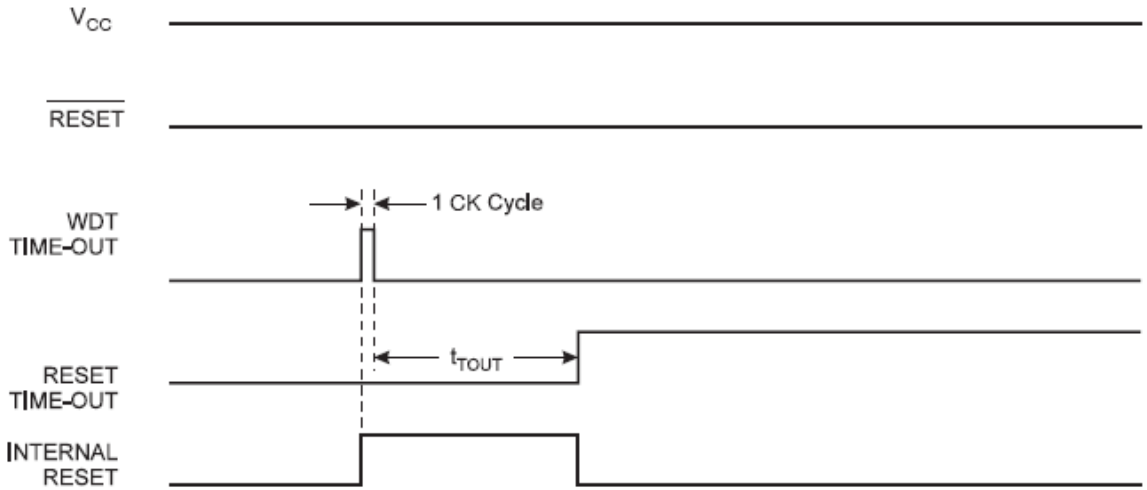
- Brown Out Reset

Figure 26. Brown-out Reset During Operation



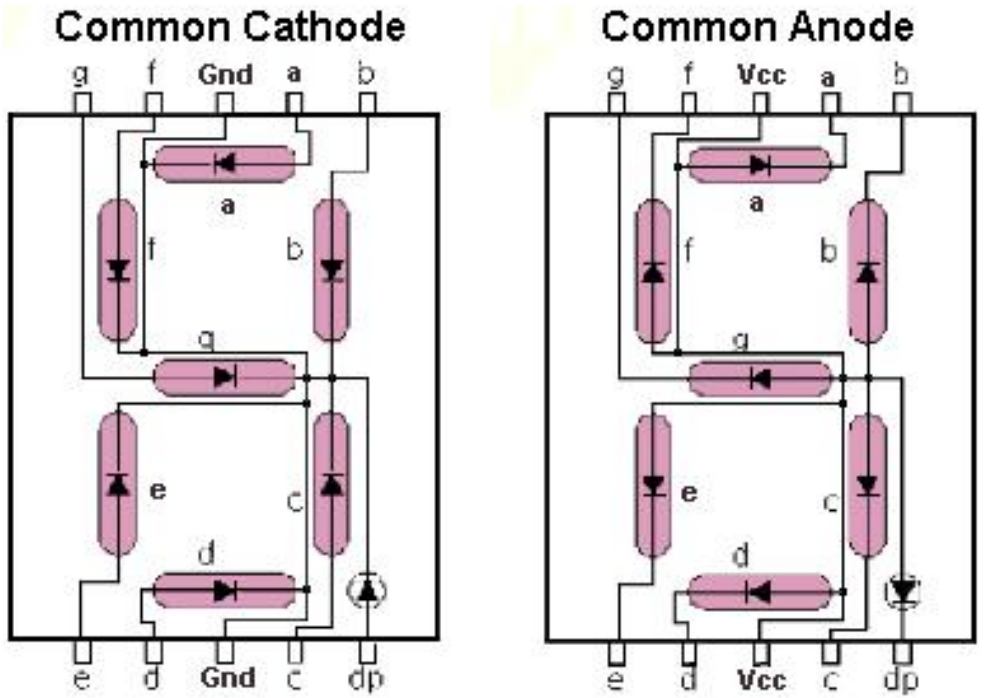
- Watch Dog Reset

Figure 27. Watchdog Reset During Operation



7-Segment

- FND(Flexible Numeric Display)
  = 7-segment



타이머 이용

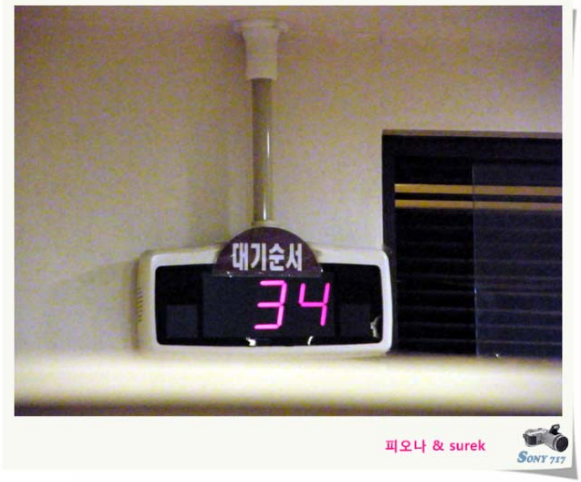
ATMEGA128

카운터 이용

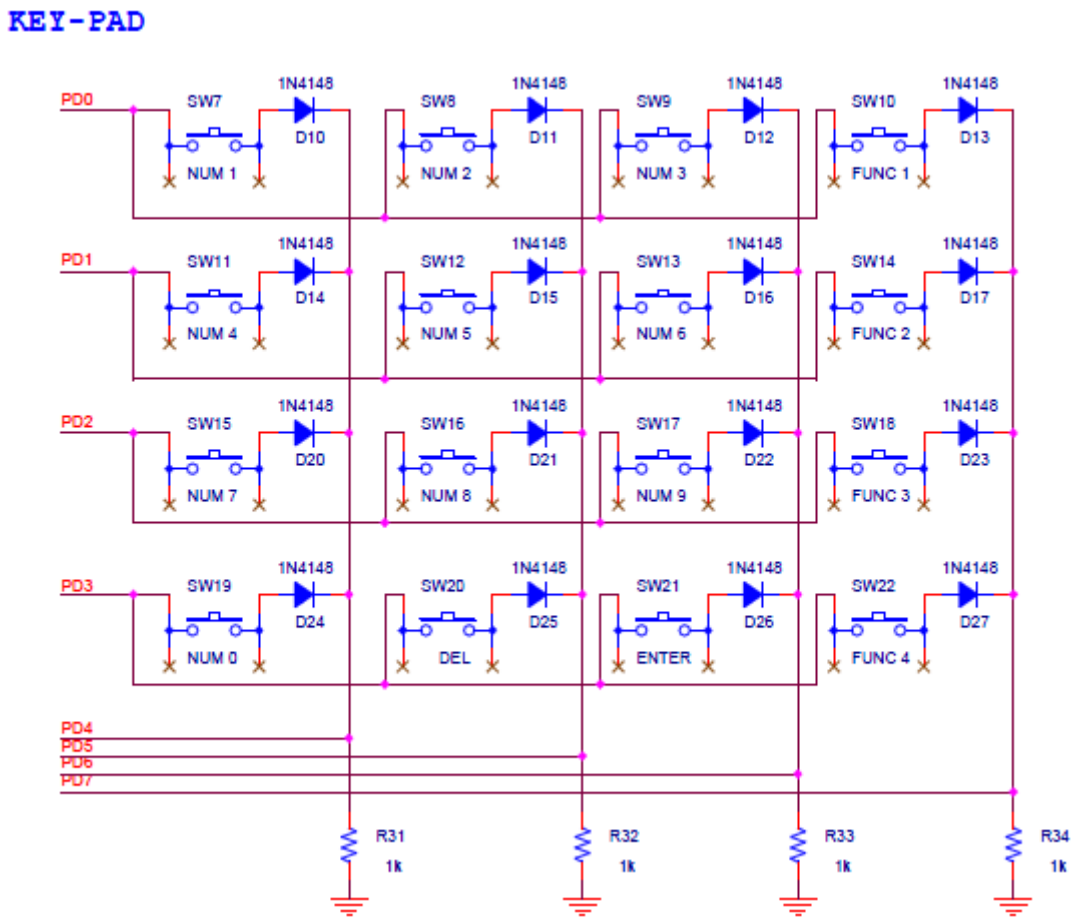
Function Generator

TTL

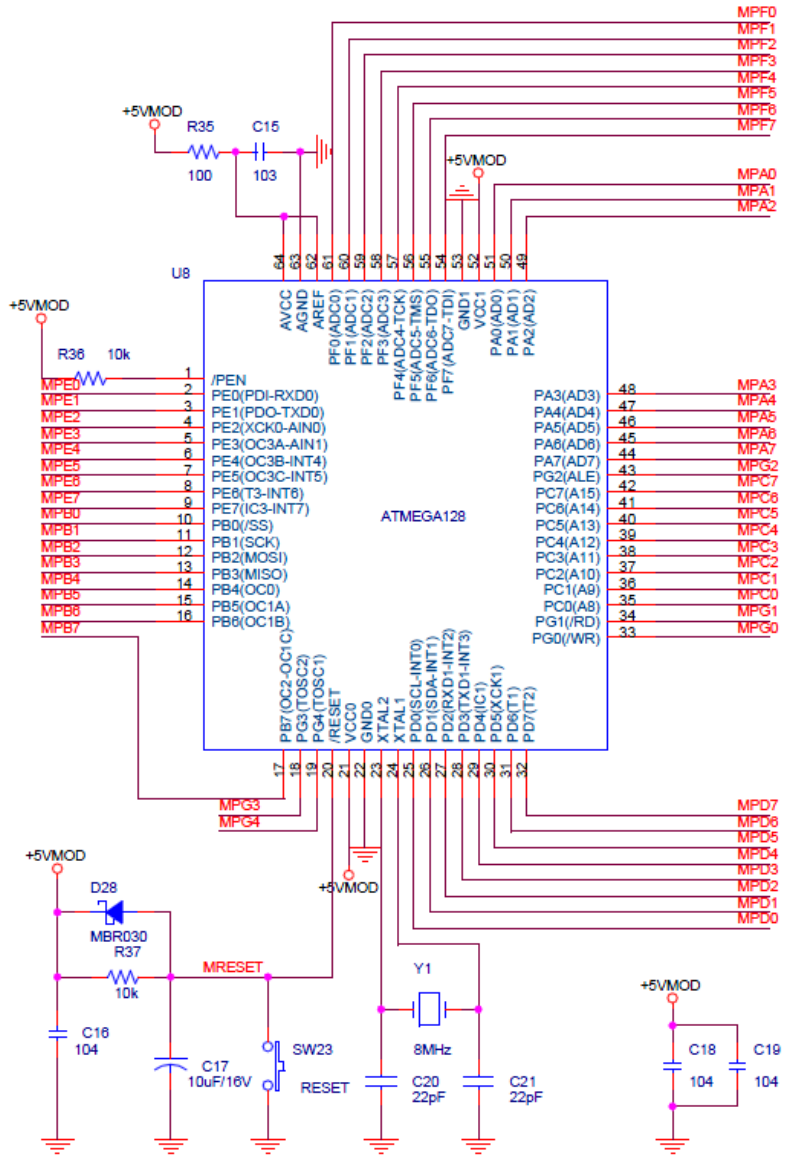
ATMEGA8

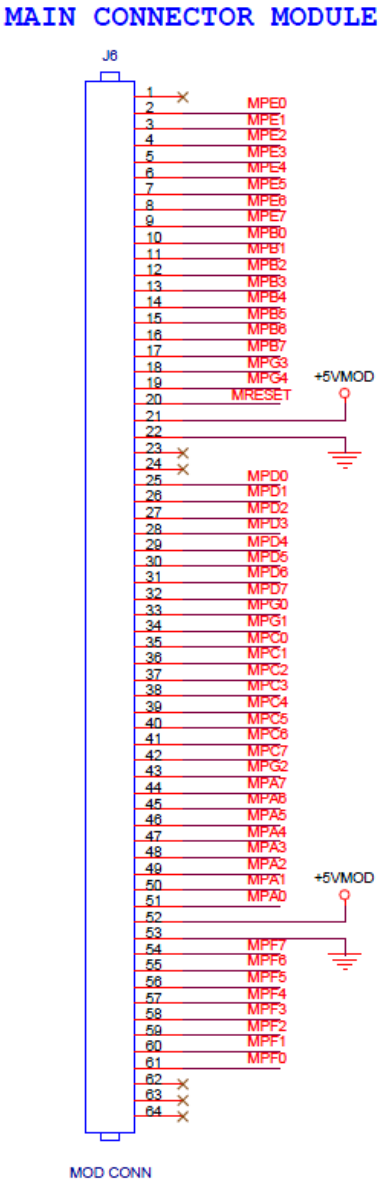


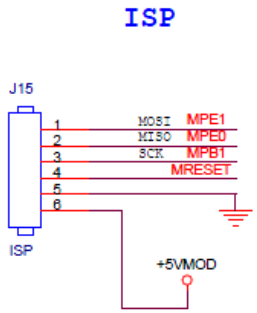
GPIO Control – 4x4 key matrix



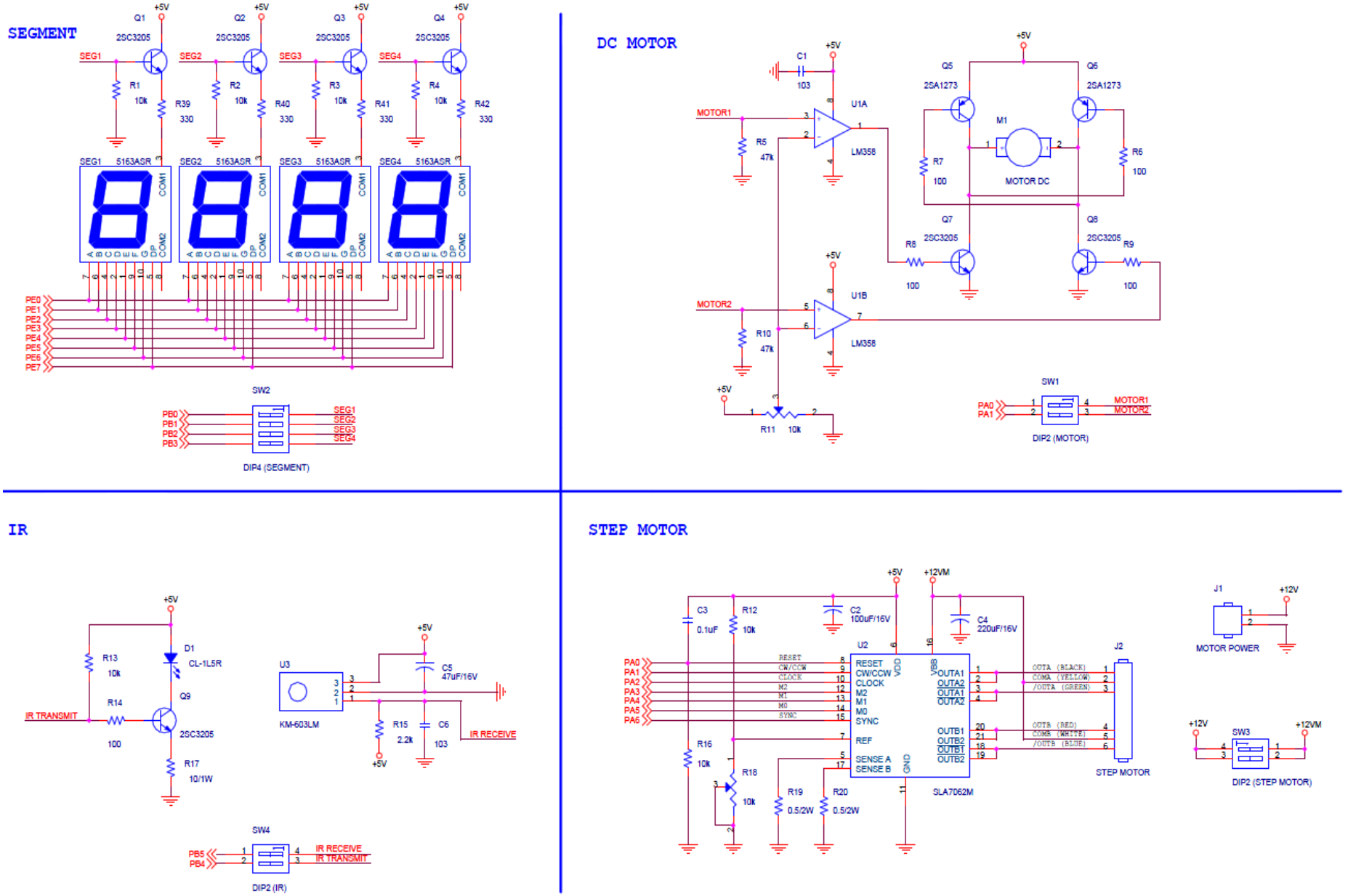
실험 Control Board



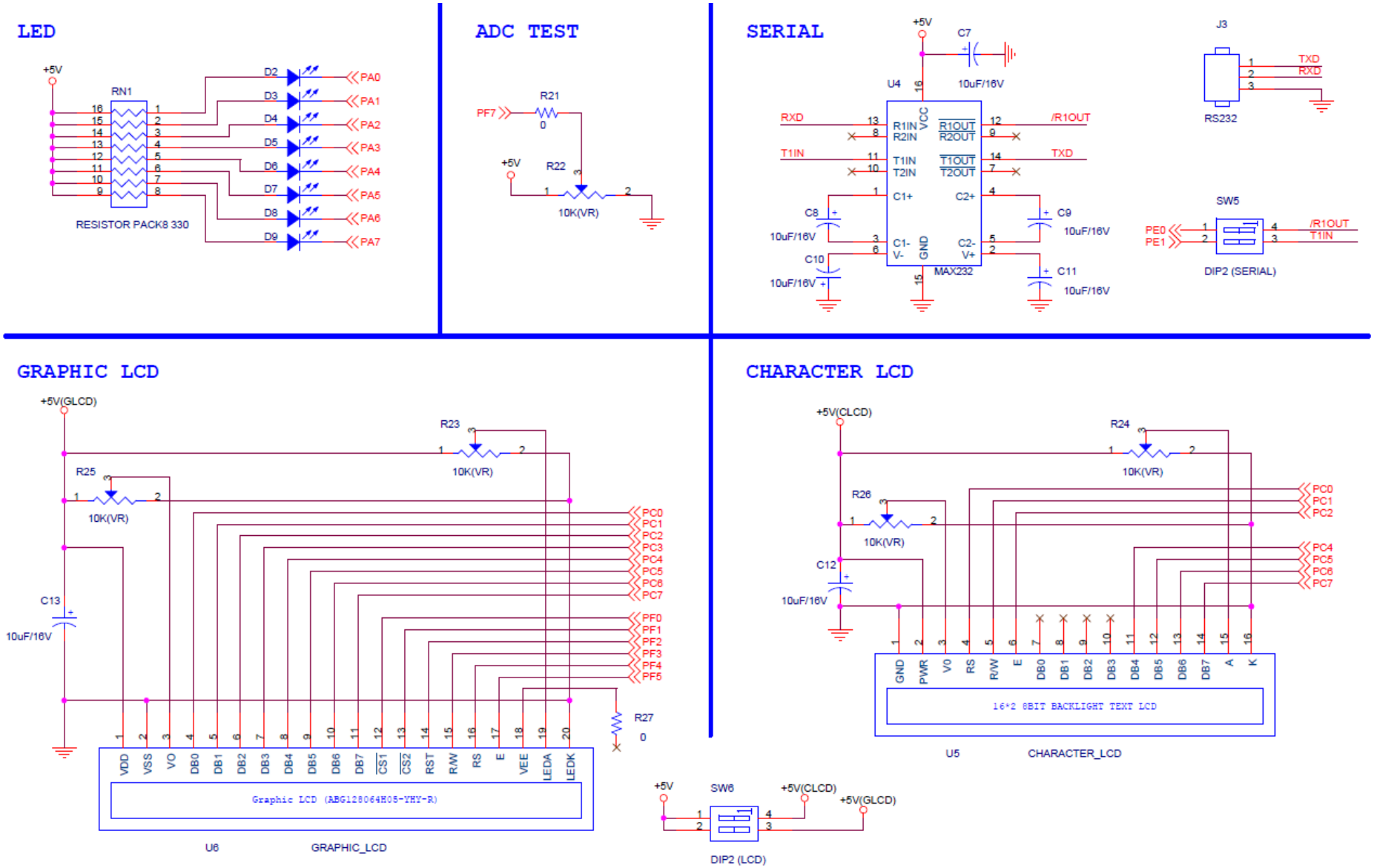




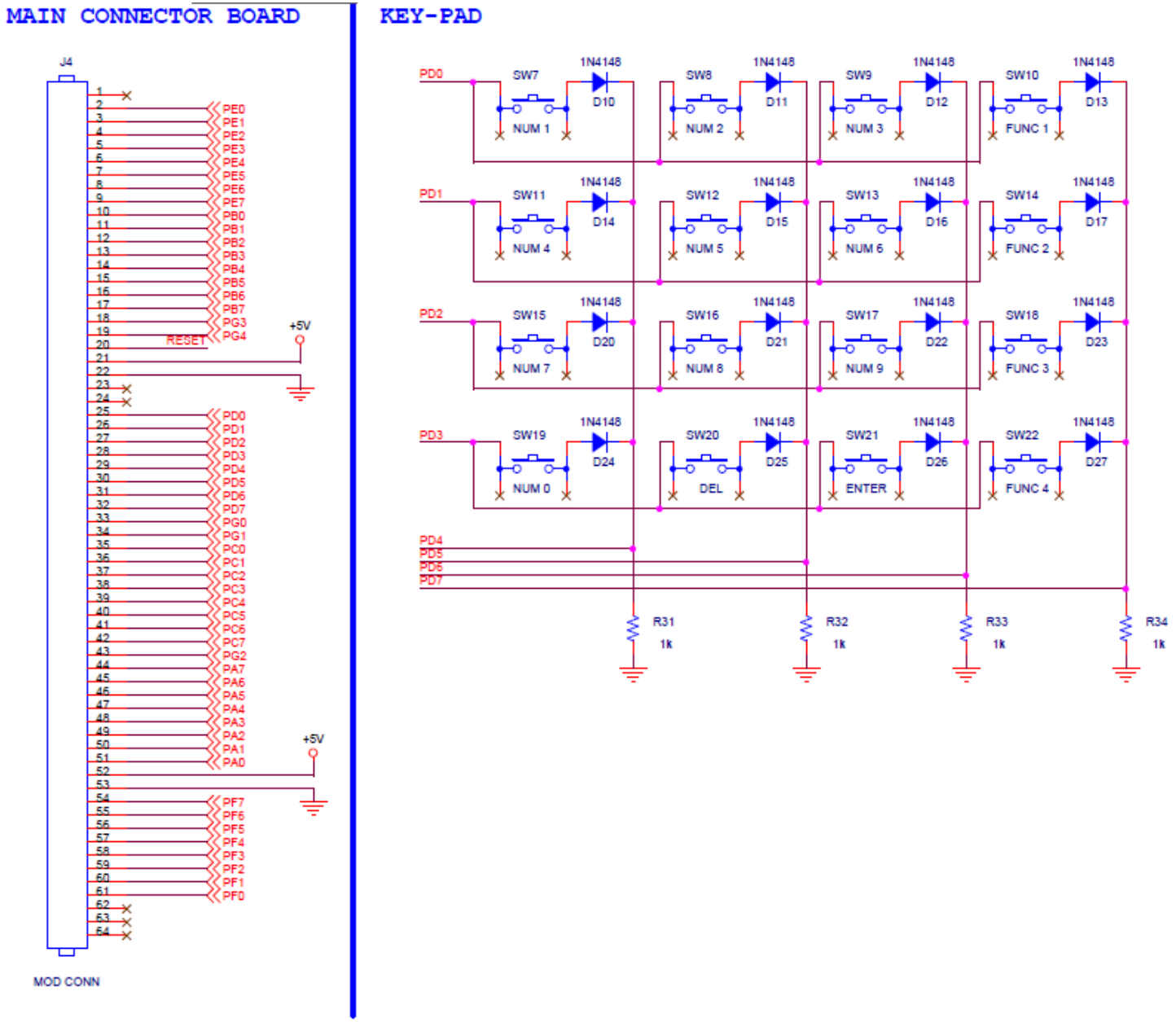
실험 Main Board 1



실험 Main Board 2



실험 Main Board 3



레포트

1. 실험 완료 할 것

반드시 동작을 이해할 것!!!

2. Mission

2-1. (7-Segment 4개와 timer/counter 이용)

앞의 두 자리는 분(00~59), 두의 두 자리는 초(00~59) 를 표시하는 디지털 시계 코딩

2-2. (7-Segment 4개, timer/counter, 4x4 키패드 이용)

앞의 두 자리는 초(00~59), 두의 두 자리는 milli 초(00~59) 를 표시

임의의 버튼 1을 누르면 시작/멈춤

임의의 버튼 2를 누르면 00:00 으로 reset

3. 기말고사

- 실기, open book(단 실험 교재와 강의파일 만 허용)
- 범위
  : C언어 firmware coding
  : GPIO, External Interrupt, Timer/Counter
  : LEDs, 7-Segment, 4x4 Keypad
  : 책의 예제, Mission 들 참고할 것
- 12/16(수) 저녁 7시30분~9시30분, 의생대 401호
- 개인 노트북, 기본 소스코드 ok