Roland Coeurjoly, MSc.

rolandcoeurjoly@gmail.com +34 676 70 40 51

Profile

Software Engineer with critical software and hardware development experience in Finance, Military, Aerospace, Medical and Industrial sectors, able to work in multidisciplinary and international teams.

Attributes

- Initiative and problem solving expertise.
- Highly organized.
- Quick learner.

Skills

- Most comfortable with: C/C++, Nix, Python, Bash, GNU/Linux, git, CMake, gdb, TDD, BDD, Coq, doctest, unittest, MySQL, Verilog, LaTex, MongoDB, CMake.
- Have worked with: VHDL, Dafny.

History

- Software Engineer, BME (acquired by SIX) (Las Rozas, Madrid) - July 2019 to present
  - Design, development, testing and support of low latency trading applications, including OMS (Order Management System), risk management, portfolio management and market access drivers.
    Technologies used: multi-threaded C++, FIX, BDD, TDD, STL, CMake, gdb, doctest, CI, git, rr, Boost.
  - Propose, design and implement BDD workflow as a development methodology.
    Achievements: brought onboard team (PO, QA and devs), implemented workflow in OMS, algorithmic trading robot and market access drivers.
    Skills used: multi stakeholder technical presentations and discussions, DevOps.
    Technologies used: C++, CMake, Docker, gitlab.
  - Propose, design and implement Nix build system.
    Achievements: upgrade from C++11 to C++20 (GCC 4.8.5 to GCC 13.2), reduce compile times ~30%
    Technologies used: nix flakes, CMake

  - Propose, design and implement automatic tool to migrate to Google logging library.
    Achievements: Migration of 10k+ LOC from ACE to glog, reducing technical debt.
    Technologies used: Python, regex, unittest, black-box testing, C++.

- Electronics Engineer, GMV (Tres Cantos, Madrid) - November 2018 to May 2019

  - Design and prototype automatic tool for testing motor driver PBA used in military avionics.
    Achievements: Drastically improve coverage compared to manual test procedure.
    Technologies used: C/C++, Mixed signal circuit design, Altium.

  - Architect, design, implement and operate automatic functional verification environment used in qualification tests of hybrid (GNSS and IMU) military navigation product.
    Achievements: Successful operation during vibration and environmental tests.
    Technologies used: Embedded Linux, Python, bash, CAN, TCP/IP, PyQt, multithreading.

- Electronics Engineer, SEDECAL (Algete, Madrid) - September 2015 to November 2018

  - Propose, design, and implement automatic tool for testing docking station for X-ray detectors.
    Achievements: Design weaknesses found, helping improve product reliability.
    Technologies used: C/C++, Hardware design.

  - Design Interface PBA used in X-ray generators.
    Achievements: Improvements in reliability and serviceability.
    Technologies used: Altium.

  - Automate product tree generation for X-ray systems.
    Achievements: Process streamlined, improving reliability and speed.
    Technologies used: VBA.

  - Automate migration of electronic components data-sheets.
    Achievements: Reduce time of implementation 95% (from 200 to 10 hours).
    Technologies used: Bash.

- Laboratory engineer, GE Power Controls (Móstoles, Madrid) - October 2013 to June 2015

  - Support Transfer of Work (TOW) process of electronic modules for contactors used in the railroad industry.

Achievements: Propose and implement solution to improve product life. Bronze award for solving critical component shortages.

Education

- Inter-University Master's Degree in Formal Methods in Computer Science and Engineering, UCM-UPM-UAM - September 2020 to July 2022

  - **Electives**
    Formal Methods for Testing, Formal Model-Driven Software Development, Computer-Aided Program Verification, Design of Correct-by-Construction Systems, Quantum Computing

  - **Thesis**: DDC: a declarative debugger for C++
    Technologies used: Coq, Nix, C++, Python, GDB, rr

- Bachelor's Degree in Industrial Electronics and Automation, UC3M - 2009 to 2015

  - **Electives:**
    Digital integrated circuit design (VHDL), Power electronic systems, Analog electronics II

  - Thesis based on my work at GE Power Controls

- Exchange student with scholarship, RMIT (Melbourne, Australia) - July 2012 to December 2012

  - **Electives:**
    Computer architecture, Network Technologies, English language and Australian culture

Natural languages

English: full professional proficiency
Spanish: native fluency
French, Mandarin Chinese: advanced proficiency
Willing to learn others.

Open source contributions

- Export highlights to JSON in KOReader

  - **Skills:** Android development, Lua

Hobbies and Interests

I love reading and traveling. The highlights of my reading can be found here.