Features

- Bluetooth v4.2 specification compliant, supports BR/EDR
- Bluetooth radio includes integrated balun
- Support A2DP 1.3.1, HFP 1.5 and AVRCP 1.6.1
- Up to 178 MHz RISC MCU and 178 MHz Voice Co-Processor(VoC) DSP core
- Internal MCU ROM and RAM, VoC memory and in-package serial flash memory.
- Various serial interfaces: UART, I2C Master and SPI Master, SD Card Interface, IR receiver
- Support analog key
- Up to 4 PWM output
- Independent powered Real-Time Clock
- Two channel 24 bits voice ADC and 24 bits stereo DAC, supports sample rate of 8, 11.025, 12, 16, 22.05, 32, 44.1, 48 and 96 KHz
- Audio interfaces: PCM/I2S, analog stereo line in
- Support MP3/SBC/WMA/ACC decoder
- Support audio playback from SD card
- Support one Line in and one analog/ digital MIC
- Support mix of Line in and MIC input with wide range of programmable analog gain settings
- Debug host interface allowing non-intrusive in depth investigation GDB debugger
- Internal 32K OSC for standby, shutoff and sleep state
- Integrated LDO
- Low power consumption in both active and sleep mode, less than 20mA when playing music

RDA5856ESE

High performance, highly integrated multi-media system-on-chip solution with Bluetooth connectivity

General Description

RDA5856ESE is a high performance, highly integrated multi-media system-on-chip solution with Bluetooth connectivity, which specialized in music and audio applications.

Integrating all essential electronic components, including baseband, Bluetooth transceiver, power management onto a single system on chip, RDA5856ESE offers best in class bill of materials, space requirement and cost/feature ratio for Bluetooth music and audio application.

Applications

- Bluetooth speakers
- Bluetooth music box
- Bluetooth headset or headphone

The up to 178 MHz Voice Co-Processor supports various audio applications. The integrated audio codec supports two channels DAC and one channel ADC. Playback form SD card is also supported.

Table of Contents

1. Product Details

Bluetooth Radio

- Fully compliant with Bluetooth radio specification 4.2 including basic rate and EDR.
- On-chip Balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA.

Microcontrollers

- RDA proprietary 16/32 bit processor
- Reduced Instruction Set Architecture
- Efficient 6-stage instruction pipeline

Voice Co-Processor

- RDA Internal designed Voice DSP core
- Two 16x16 -> 32 Multipliers
- Bi-MAC (two accumulations on the same register per cycle)
- Eight 16 bit general purpose registers and four 32 bit general purpose registers

Audio Interface

- Audio codec with 24 bits stereo DAC and two channel 24 bits ADC
- Support sample rate of 8, 11.025, 12, 16, 22.05, 32, 44.1, 48 and 96 KHz.
- Support Dual Analog MIC and Dual Digital MIC or one Analog MIC + one Digital MIC

Peripheral and Interfaces

- Debug host for debug and normal UART
- UART interface
- SDMMC controller for SD card
- I2C master for external modules access
- SPI master for external modules access
- I2S interface which is compatible with PCM interface, support configurable MCLK output
- Up to 6 GPIOs
- IR receiver

Integrated Power Management

- Multiple LDOs
- Low power mode supported

Package Options

- HSOP16

2. Package and Pinout

2.1. Pin Assignment

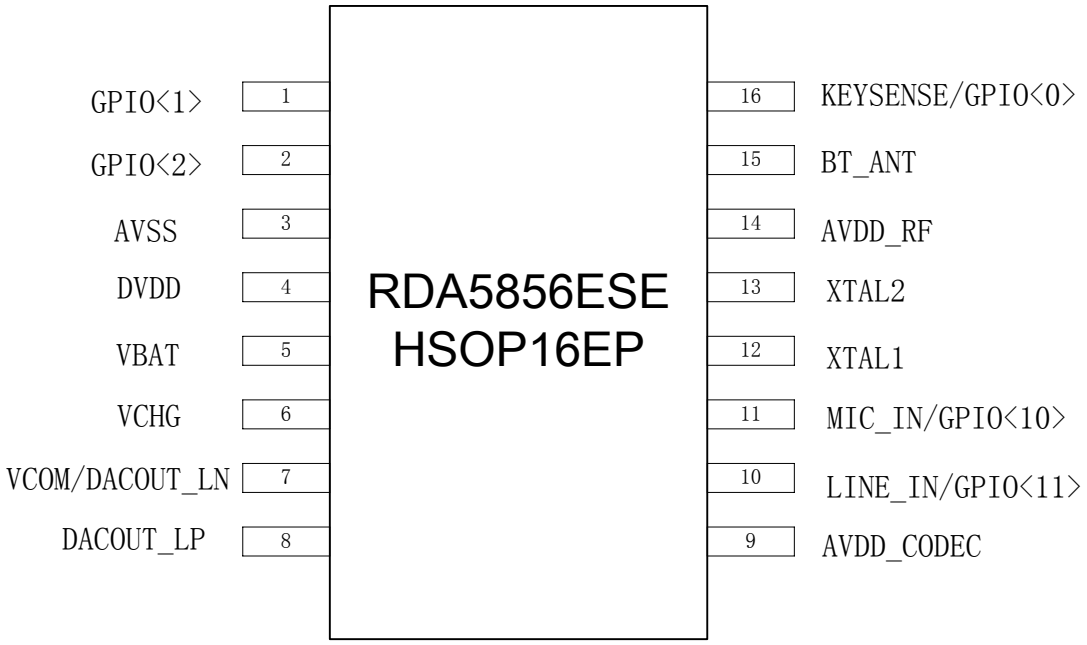


Figure 1 Pin Assignment

2.2. Pin Description

Table 1 Pin Types

Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
PWR	Power
GND	Ground

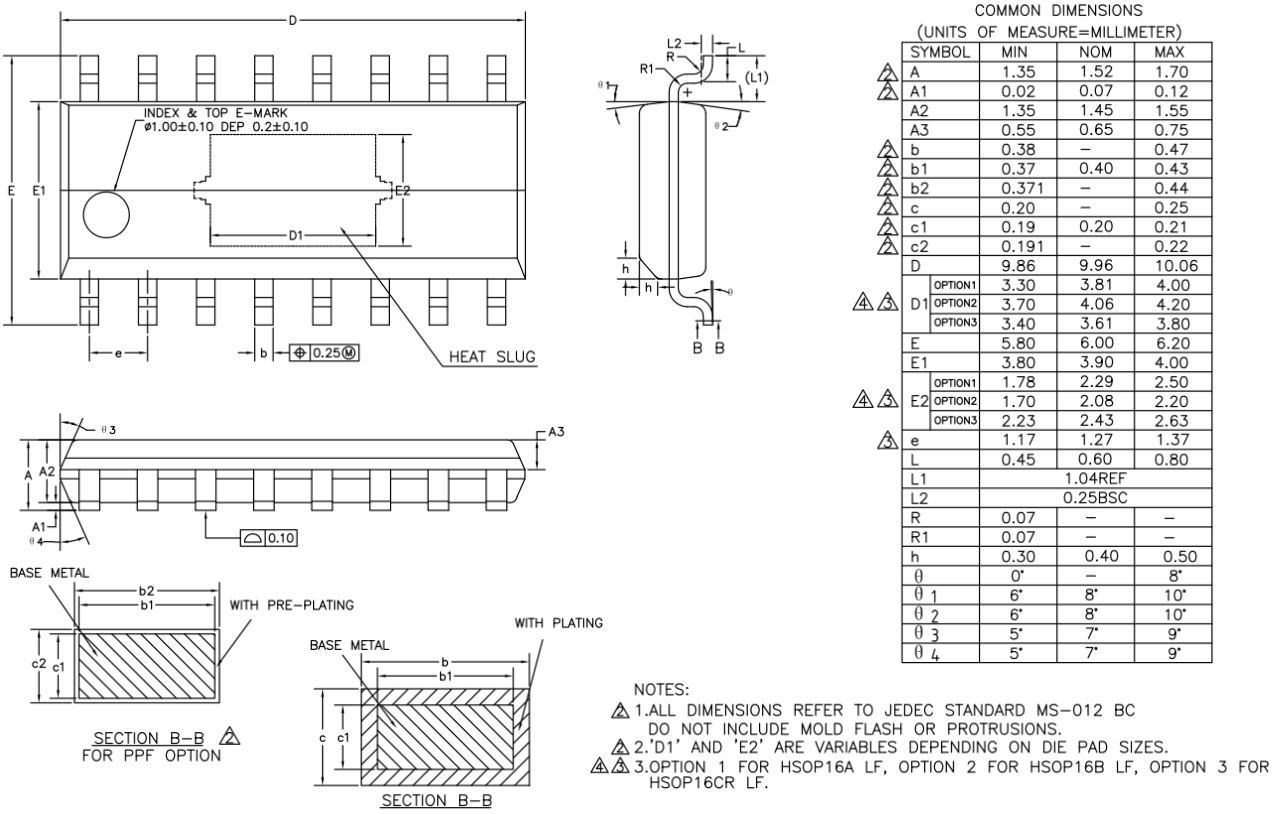
Table 2 Pin Description

PIN NO	NAME	TYPE	DESCRIPTION
1	GPIO<1>	I/O	Multiple functions configured by GPIO<1> func_sel. 0: I2C slave clock input 1: General purpose input/output 2: I2C master clock 3: UART TXD 4: SD clock 5: IR RXD 6: SPI clock 7: PWM output 3 8: I2S BCLK 9: Debug host TXD 11: GPIO interrupt input 3
2	GPIO<2>	I/O	Multiple functions configured by GPIO<2> func_sel. 0: I2C slave data 1: General purpose input/output 2: I2C master clock 3: UART RXD 4: SD command 5: IR RXD 6: SPI DCX 7: PWM output 0 8: I2S master clock

			9: Debug host RXD 11: GPIO interrupt input 4
3	AVSS	GND	Analog Ground
4	DVDD	PWR	Power of digital core
5	VBAT	PWR	Battery power supply
6	VCHG	PWR	Charger power supply
7	VCOM/DACOUT_LN	A, O	Common mode voltage/DAC output left negative
8	DACOUT_LP	A, O	DAC output left positive
9	AVDD_CODEC	PWR	Power of analogue CODEC
10	LINE_IN/GPIO<11>	A, I or I/O	Multiple functions configured by GPIO<11> func_sel. 0: Debug host TXD 1: General purpose input/output 2: I2C master data 3: UART TXD 4: SD data 0 5: PDM data 6: SPI chip select 1 7: PWM output 3 8: I2S BCLK 10: LINE_IN 11: GPIO interrupt input 11
11	MIC_IN/GPIO<10>	A, I or I/O	Multiple functions configured by GPIO<10> func_sel. 0: Debug host RXD 1: General purpose input 2: I2C master clock 3: UART RXD 4: SD data 1 5: PDM clock 6: SPI DIO 7: PWM output 2 8: I2S LRCLK 10: MIC_IN 11: GPIO interrupt input 10
12	XTAL1	A, I	XTAL input
13	XTAL2	A, O	XTAL output
14	AVDD_RF	PWR	Power of analogue RF
15	BT_ANT	A, I/O	Bluetooth transmitter output/receiver input
16	KEYSENSE/GPIO<0>	A, I or I/O	Multiple functions configured by GPIO<0> func_sel and keysense_enb in PMUC. keysense_enb = 1'b0 – Keysense keysense_enb = 1'b1 – 0: General purpose input/output 1: Debug host TXD 2: I2C master clock 3: UART RXD 4: SD data 3 5: IR RXD 6: SPI clock 7: PWM output 1 8: I2S data input 11: GPIO interrupt input 0

Table 3 Pin Description

2.3. Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		1.35	1.52	1.70
A1		0.02	0.07	0.12
A2		1.35	1.45	1.55
A3		0.55	0.65	0.75
b		0.38	–	0.47
b1		0.37	0.40	0.43
b2		0.371	–	0.44
c		0.20	–	0.25
c1		0.19	0.20	0.21
c2		0.191	–	0.22
D		9.86	9.96	10.06
D1	OPTION1	3.30	3.81	4.00
	OPTION2	3.70	4.06	4.20
	OPTION3	3.40	3.61	3.80
E		5.80	6.00	6.20
E1		3.80	3.90	4.00
E2	OPTION1	1.78	2.29	2.50
	OPTION2	1.70	2.08	2.20
	OPTION3	2.23	2.43	2.63
e		1.17	1.27	1.37
L		0.45	0.60	0.80
L1		1.04REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
h		0.30	0.40	0.50
θ		0°	–	8°
θ1		6°	8°	10°
θ2		6°	8°	10°
θ3		5°	7°	9°
θ4		5°	7°	9°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 BC
   DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.
3. OPTION 1 FOR HSOP16A LF, OPTION 2 FOR HSOP16B LF, OPTION 3 FOR HSOP16CR LF.

3. Function Block Diagram

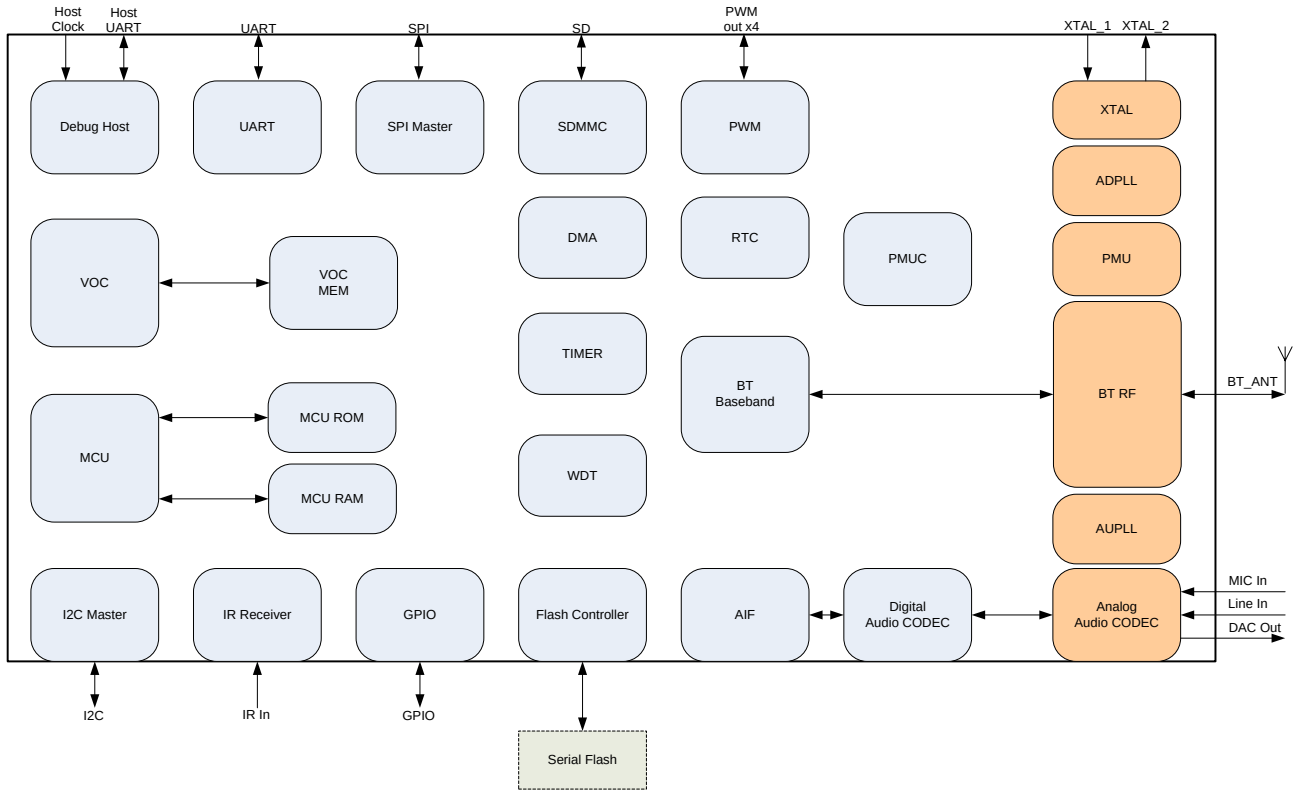


Figure 2 RDA5856ESE Block Diagram

4. Clock and Reset

RDA5856ESE has a reference clock input from either a crystal or an external clock source. There are two internal PLLs which use XTAL clock as reference. They are used for system and audio applications.

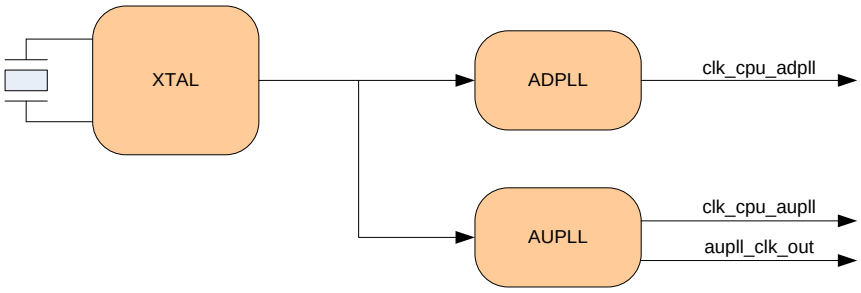


Figure 3 Clock Structure

RDA5856ESE has several reset sources, as following:

- POR
  Entire SoC is reset after power supply ramping from 0v to VBAT.
- External Pin Reset
  Entire SoC is reset except PMU.
- Warm Reset
  - ✓ Global soft reset
    DBB can be reset by set soft reset register in system control register map.
  - ✓ Watch Dog Reset
    DBB will be reset when watch dog timer expired.
  - ✓ Debug Reset
    DBB will be reset through debug host set its internal register.

5. MCU

RDA RISC is a 16/32-bits processor which using a Reduced Instruction Set Architecture, an efficient 6-stage instruction pipeline, it provides high performance to the system.

- RDA RISC Core.
  - ✓ 32x32-bit Multiplier.
  - ✓ 32x32-bit -> 64-bit Multiplier Accumulator (MAC) in 2 cycles (pipelined).
  - ✓ Read / Write Buffer.
  - ✓ 16/32 bit instruction set.
- 32 interrupt sources.
- TCM interface for ROM read

6. VoC

The VoC is designed to process different vocoders. It is developed as a target-specific DSP core, including basic function-call support. It executes the code with very little control intervention from the MCU. It is controlled and configured by the MCU through the AMBA bus.

- Bi-MAC, single test/logic Computational Unit with two 16x16 -> 32-bit multipliers
- Eight 16-bit general purpose registers that can be combined in four 32-bit general purpose registers.

- All 16-bit registers can be used as pointers; four of them are incremental (for easy array addressing).
- Four 32-bit general purpose registers.
- Double stack with random access: for 32-bit & 16-bit values (push, pop).
- Functions call support (jal, return).
- Two zero-cycle loop counters.
- Pointer & Direct addressing modes.
- DMA sub-module for block transfers between external memory and VoC memories.

7. Flash Controller

The Flash controller provides instruction/data management on serial Flash devices. A command poll is used to support variable commands for variable flash devices. Flash devices are supported using Standard, Dual or Quad SPI. Besides the normal Flash read mode using register address through RX FIFO, the Flash controller provides an XIP mode, in which CPU can read Flash address range as RAMs.

- Standard, Dual, Quad SPI.
- Command poll to support variable Flash commands, including advanced read commands.
- Normal Read & XIP mode.

8. DMA

RDA5856ESE supports various DMA functions. It supports memory to memory, memory to peripheral, peripheral to memory transfers. For transfers between memory and peripheral, hardware handshake is supported and multiple DMA channels shared with peripherals.

- Support for linear memory transfers.
- Multiple DMA channels
- Support for word, half-word and byte aligned addresses.
- Burst transfer supported
- Interrupt generation at completion of the transaction.
- Can fill a part of the memory with a 32-bit pattern.
- Frame Check Sequence computation

9. AIF

The Audio Interface (AIF) module is the audio interface between the system and internal/external audio codec.

- Common features
  - ✓ All common DTMF and Comfort Tones can be generated and gained from -15 dB to 0 dB
  - ✓ Side Tone fully configurable: Mute or amplification from -36 dB to +6 dB
  - ✓ Loop back capabilities for test purposes.
- Serial Interfaces.
  - ✓ MSB/LSB configurable.
  - ✓ Configurable as master or slave.
  - ✓ LRCK/BCLK ratio from 16 to 31.
  - ✓ Supports multiple sample rates (8 kHz; 11.025 kHz; 12 kHz; 16 kHz; 22.05 kHz; 24 kHz; 32 kHz; 44.1 kHz; 48 kHz; 96 kHz).
  - ✓ Fully configurable clock polarity.

- ✓ Configurable TX/RX data delays.
- ✓ Support Audio Mode: I2S compatible
- ✓ Support Voice Mode: One cycle strobe pulse at the beginning of each new sample.

- Parallel Interface
  - ✓ Separate TX and RX strobe lines for synchronization.

10. SDMMC Controller

This module connects inner bus and outer SD or MMC card. It receives the inner command and data, transfers it to outer SD or MMC card, and transfer response or data back.

- SD Card Specification Version 2.0
- SDIO Version 1.10
- MMC specification Version 3.1
- Hot insertion and removal of media cards will be considered by GPIO module

11. Timer

There are three different timers.

- 1 24-bit decremental timer for OS, ticks of 16384Hz.
- 1 32-bit incremental hardware delay timer, ticks of 16384Hz.
- 1 24-bit decremental watchdog timer, ticks of 32768Hz.
- Multiple IRQ sources: timers wrap, interval arrives.

12. GPIO

GPIO module has configurable number of General Purpose Input or Output ports (GPIO).

- Up to 6 GPIOs configurable as input or output.
- Up to 6 GPIOs can generate interrupt.
- Various interrupt triggered mode.
  - ✓ Rising/Falling edge.
  - ✓ High/Low level.

13. UART

RDA5856ESE includes UART which can be used as a serial interface or as an IrDA interface.

- Smooth stop feature (the UART stops after the end of the current word transfer).
- Break generation and detection.
- Supports Automatic Flow Control (CTS and RTS lines).
- Supports low speed IrDA 1.0 SIR mode by adding external hardware.
- DMA capabilities to allow fully automated data transfers.
- Wide selection of programmable interrupts to allow interrupt driven data transfer management.
- Loop Back capabilities for test purposes.

14. Debug Host

Debug Host module contains 1 normal Universal Asynchronous Receiver Transmitter channels (UART) and 1 Debug UART. The two UARTs share the same TX/RX engines, which sends and receives byte data from serial interface. Each UART has its own control sub-module and own APB interface. Debug Host module parses the incoming data from serial interface to switch between the normal UART and the Debug UART.

- Normal UART

The normal UART can be used for traces and other purposes. For APB interface, it is exactly the same to the other UARTs in the system. However, if Debug UART is enabled, it should have the same serial interface configuration as the Debug UART. Some of its configuration options will be masked in this case. To adapt different clock frequency, the normal UART uses asynchronous FIFO, which uses gray code to represent the read and write pointer positions.

- Debug UART

The Debug UART is specially designed for communicating debug information with a PC host. The serial interface of Debug UART is a simplified version of the normal UART and is less configurable. Each sample is sent serially, has 1 start bit (always zero), 8 data bits, and 1 stop bits (always one). Breaks (data line held low) can be generated and detected allowing resynchronizing the two devices.

15. SPI Master

This module is a master interface for a synchronous serial link, it can be configured to be compatible with Motorola SPI or to comply with some various synchronous serial protocols.

- Multiple chip selects and selectable data input.
- Programmable clock polarity.
- Programmable data frame size (from 4 to 32 bits).
- Programmable delay options (time between CS, clocks and data).
- Received pattern matching before filling RX FIFO (SD-MMC read block feature)
- Transmit zero when TX FIFO empty (for generating dummy data during pattern matching read)
- Direct pin control to force value to 0, 1 or input.
- Special read mode with output enable control of the DO pin (selected input should be multiplexed with DO pin to use this feature).

16. I2C Master

RDA5856ESE has I2C master which supports 100Kbps and 400Kbps.

- Compatible with Philips I2C standard
- Multi Master Operation
- Software programmable clock frequency
- Clock stretching and wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 and 10 bit addressing mode
- Operates from a wide range of input clock frequencies

17. IR Receiver

The IR receiver module performs serial-to-parallel conversion on received data from a peripheral device. It supports NEC, RC-5 and Philips 9012 mode.

- Support 3 IR modes, NEC, RC-5 and Philips 9012

- Store data code and user code
- Support data code and user code verify
- Enable interrupt when data received
- Configurable frame time, bit time, high-time and low-time

18. Calendar

The calendar module provides date and time information. It works on the 32.768 KHz oscillator with independent power supply. In addition to provide timing data, alarm interrupt is generated and it is also used to power-up the baseband core by sending wakeup signal.

- Independent power supply.
- Counters for second, minute, hour, day, month, year and day of week.
- Maxim day of each month stored in module, leap year supported.
- Alarm generate, wakeup triggered by alarm. Alarm IRQ.
- Periodical IRQ for certain intervals.

19. PWM

The PWM module generates 4 independent PWM outputs, utilizing 3 specialized modulation schemes. All PWM outputs can be configured to PWL, PWT and LPG mode.

- Pulse Width Tone (PWT)
  - ✓ Generates square wave output capable of driving piezo electric speaker
  - ✓ Variable frequency between 349Hz and 5276Hz with 12 half-tone frequencies per octave
  - ✓ Volume control
- Light Pulse Generation (LPG)
  - ✓ Adjustable PWM frequency is from 0.01Hz ~ 6.5MHz
  - ✓ Adjustable on-time/off-time is from 0.77us to 50s.
  - ✓ Customized output mode for square wave
- Pulse Width Light (PWL)
  - ✓ Pseudo random bit sequence with output on-time proportional to a programmed threshold value
  - ✓ Minimizes flicker

20. Audio Codec

The audio codec has dual channel voice ADC and audio DAC, which supports stereo voice input and stereo audio output. It also has flexible mixing and loopback paths to support variable scenario requirements, such as side tone and etc.

- Dual channel 24 bits ADC and 24 bits stereo DAC
- Support dual digital MIC
- Stereo input for voice and audio band, input resistance is typically 4KΩ.
- Integrated mic bias which don’t need external load capacitor with configurable output voltage
- Stereo outputs are supported, could drive 16Ω/32Ω headphone, or act as line-out.
- Support sample rate of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 KHz.
- Configurable gain for audio input and output path, gains control is implemented in both digital and analog.
- Flexible audio/voice path mixing/loopback.

21. Power Management

RDA5856ESE uses battery as power source, and PMU integrated multiple LDOs.

PMU performs a POR once battery is connected which resets all components in chip. A dedicated pin is allocated to support external global reset function. PMU can be configured to use DIP switch or press button as power switch.

To achieve low power target in various scenarios, PMU supports quick enter to deep sleep mode from active mode and quick wakeup from deep sleep mode to active mode.

22. Bluetooth Transceiver

RDA5856ESE integrates Bluetooth baseband and radio which has been designed to provide low power, low cost and robust communications for Bluetooth application. It is fully compliant with Bluetooth radio specification 4.2 including BR, EDR up to 3Mbps. RDA5856ESE contains an on-chip Balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA.

- Baseband
  The BT baseband core handles packet and bit stream processing including packing/unpacking for different packet types, error checking, whitening/de-whitening, error correction, and encryption/decryption and so on.
  - ✓ Compliant with Bluetooth 4.2 + EDR specification
    - Support BR, EDR 2M/3M
    - Support SCO/eSCO
  - ✓ Bluetooth Piconet and Scatternet support
  - ✓ Low power support and optimization
    - Support AFH
    - Sniff Subrating
    - Enhance Inquiry Response
    - Sleep on 32.768KHz clock
  - ✓ Test Mode support
    - BR/EDR Transmitter test and Loopback test
    - Fixed pattern, PRBS-9, PRBS-15 or user defined pattern
- RF Receiver
  The receiver features a low-IF architecture that enables the channel select filters to be integrated onto the die. The down converted signal is digitalized by a high performance ADC and further processed by a digital demodulator. The receiver path provides a low noise figure, a high degree of linearity and an extended dynamic range.
- RF Transmitter
  The transmitter features a direct IQ modulator to minimize frequency drift during a packet, which results in a well-controlled modulation index. The digital modulator performs the data modulation and filtering required for the Bluetooth signal. The internal PA has a programmable output power that meets Class1, Class 2 and class3 Bluetooth radio requirements without an external RF PA.
- RF Synthesizer

The radio synthesizer is fully integrated onto the die with no requirement for external LC resonators or loop filter. The synthesizer provides fast frequency locking and low phase noise to meet Bluetooth specification.

23. Electrical Characteristics

23.1. BT RF Specifications

Receiver Characteristics --- Basic Data Rate (VBAT = 4.0 V, TA = +27℃, unless otherwise specified)

Symbol	*Parameter*	*Condition*	*Min*	*Typ.*	*Max*	*Unit*
General Specification						
Sensitivity @ 0.1% BER			/	-91	/	dBm
Maximum input @ 0.1% BER			0	/	/	dBm
C/I co-channel			/	/	9	dB
Adjacent channel selectivity C/I		F = F0 + 1 MHz	/	/	-12	dB
		F = F0 – 1 MHz	/	/	-10	dB
		F = F0 + 2 MHz	/	/	-40	dB
		F = F0 – 2 MHz	/	/	-40	dB
		F = F0 + 3 MHz	/	/	-45	dB
		F = F0 – 3 MHz	/	/	-45	dB
		F = F_image	/	/	-10	dB
Out-of-band blocking		30MHz–2000MHz	-10	/	/	dBm
		2000MHz–2400MHz	-20	/	/	dBm
		2500MHz–3000MHz	-20	/	/	dBm
		3000MHz–12.5GHz	-10	/	/	dBm
Inter-modulation			-34	/	/	dBm

Transmitter Characteristics --- Basic Data Rate (VBAT = 4.0 V, TA = +27℃, unless otherwise specified)

Symbol	**Parameters**	**Condition**	**Min**	**Typ.**	**Max**	**Unit**
General Specification						
Max RF output power			/	4	/	dBm
Power control step			/	3	/	dB
20dB bandwidth			/	0.92	/	MHz
Adjacent channel transmitter power		|M – N| = 2 MHz	/	/	-52	dBm
		|M – N| >= 3 MHz	/	/	-55	dBm
Δf1avg Maximum modulation			/	152	/	kHz
Δf2avg/Δf1avg			/	0.97	/	/
ICFT			/	/	10	kHz
Drift (1 slot packet)			/	10	/	kHz
Drift (5 slot packet)			/	10	/	kHz

Receiver Characteristics --- Enhanced Data Rate (VBAT = 4.0 V, TA = +27℃, unless otherwise specified)

Symbol	**Parameter**	**Condition**	**Min**	**Typ.**	**Max**	**Unit**
π/4 DQPSK						

Sensitivity @0.01% BER		/	-90.5	/	dBm
Maximum input @ 0.1% BER		-3	/	/	dBm
C/I co-channel		/	/	10	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	/	/	-10	dB
	F = F0 – 1 MHz	/	/	-8	dB
	F = F0 + 2 MHz	/	/	-39	dB
	F = F0 – 2 MHz	/	/	-39	dB
	F = F0 + 3 MHz	/	/	-45	dB
	F = F0 – 3 MHz	/	/	-45	dB
	F = F_image	/	/	-8	dB
8DPSK					
Sensitivity @0.01% BER		/	-82.5	/	dBm
Maximum input @ 0.1% BER		-5	/	/	dBm
C/I co-channel		/	/	20	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	/	/	-2	dB
	F = F0 – 1 MHz	/	/	0	dB
	F = F0 + 2 MHz	/	/	-28	dB
	F = F0 – 2 MHz	/	/	-28	dB
	F = F0 + 3 MHz	/	/	-38	dB
	F = F0 – 3 MHz	/	/	-38	dB
	F = F_image	/	/	0	dB

Transmitter Characteristics --- Enhanced Data Rate (VBAT = 4.0 V, TA = +27℃, unless otherwise specified)

Symbol	***Parameter***	***Condition***	***Min***	***Typ.***	***Max***	***Unit***
General Specification						
Max RF output power			/	4	/	dBm
Relative transmit power			/	-1.5	/	dB
π/4 DQPSK max w0			/	-5	/	kHz
π/4 DQPSK max wi			/	20	/	kHz
π/4 DQPSK max |wi + w0|			/	17	/	kHz
8DPSK max w0			/	-2	/	kHz
8DPSK max wi			/	17	/	kHz
8DPSK max |wi + w0|			/	17	/	kHz
π/4 DQPSK Modulation Accuracy		RMS DEVM	/	10	/	%
		DEVM < 30%	/	100	/	%
		Peak DEVM	/	/	24	%
8DPSK Modulation Accuracy		RMS DEVM	/	10	/	%
		DEVM < 30%	/	99.8	/	%
		Peak DEVM	/	/	22	%

π/4 DQPSK In-band spurious emissions	|M – N| =1 MHz	/	/	-38	dBc
	|M – N| =2 MHz	/	/	-37	dBm
	|M – N| >= 3 MHz	/	/	-41	dBm
8DPSK In-band spurious emissions	|M – N| =1 MHz	/	/	-37	dBc
	|M – N| =2 MHz	/	/	-36	dBm
	|M – N| >= 3 MHz	/	/	-40	dBm
EDR Differential Phase Coding		/	100	/	%

23.2. Audio Characteristics

MICBIAS						
Parameter	***Symbol***	***Test conditions***	***Min***	***Typ***	***Max***	***Unit***
Bias Voltage	$V_{MICBIAS}$	0.1V/step	1.8		2.1	V
Maximum Current	I_{BIAS}				2	mA
Output Noise Level	V_N			5		uV
Capacitive Load		Ibias<2mA			20	pF

MICPGA + ADC							
	Parameter	***Symbol***	***Test conditions***	***Min***	***Typ***	***Max***	***Unit***
Differential Input Mode	Full Scale Input Signal	V_{MAX}	Input Gain = 0dB Input Gain = 21dB Digital Output Level = -1dBFS		2.3 0.24		Vpp
	Input Resistor	R_{IN}		4.5	6	7.5	KΩ
	Signal to Noise Ratio	SNR	Input Gain = 0dB, fs≤48KSPS fs=96KSPS Input Gain = 21dB, fs≤48KSPS fs=96KSPS A-Weighting, 0 ~ fs/2		87 84 84 81		dB
	Total Harmonic Distortion plus Noise	THD+N	Digital Output Level = -2dBFS		-85		dBc
	Input Referred Noise Level	$V_{IN,REF}$	Input Gain = 21dB, fs≤48KSPS fs=96KSPS A-Weighting, 0 ~ fs/2		5.3 7.4		uV
	Channel Separation				80		dB
	Full Scale Input Signal	V_{MAX}	Input Gain = 0dB Input Gain = 21dB Digital Output Level = -7dBFS		1.2 0.12		
	Input Resistor	R_{IN}		4.5	6	7.5	KΩ
	Signal to Noise Ratio	SNR	Input Gain = 0dB		86		dB

Single-Ended Input Mode			Input Gain = 21dB A-Weighting, 0 ~ fs/2		84		
	Total Harmonic Distortion plus Noise	THD+N	Input Gain = 0dB Input Gain = 21dB Digital Output Level = -8dBFS		-78 -80		dBc
	Input Referred Noise Level	$V_{IN,REF}$	Input Gain = 21dB A-Weighting, 0 ~ fs/2		5.7		uV
	Channel Separation				80		dB

DAC						
Parameter	***Symbol***	***Test Conditions***	***Min***	***Typ***	***Max***	***Unit***
Full-scale Output Signal	V_{MAX}	0dB $Gain_{ana}$ -6dB $Gain_{ana}$		2.4 1.2		V_{pp_diff}
Output Power	P_{MAX}	Differential Output, 0dB $Gain_{ana}$, R_L = 16Ω R_L = 32Ω Differential/S.E. Output, -6dB $Gain_{ana}$, R_L = 16Ω R_L = 32Ω THD<1%, 1KHz		31 23 11 5.5		mW
Signal to Noise Ration	SNR	0dB $Gain_{ana}$ -6dB $Gain_{ana}$ A-Weighted, 48KSPS		97 94		dB
Total Harmonic Distortion	THD+N	0dB $Gain_{ana}$ -6dB $Gain_{ana}$ -1dBFS, 48KSPS		-90 -90		dBc
Output Noise Level	V_N	0dB $Gain_{ana}$ -6dB $Gain_{ana}$ A-Weighted, 48KSPS		12 8		uV
Digital Gain		0.5dB/step	-25.5		5.5	dB
Analog Gain		3dB/step	-21		6	dB

23.3. Recommended Operating Conditions

Operating Condition	***Min***	***Typ***	***Max***	***Unit***
Operating Temperature Range	-20	20	65	℃
VBAT	2.4	3.7	4.35	V
VCHG	4.6	5	5.75	V
VIO	3/2.25/1.62	3.3/2.5/1.8	3.6/2.75/1.98	V

23.4. GPIO Driver Current

Min	***Typ***	***Max***	***Unit***
7.8	11.9	12.8	mA

24. Software

The software development of RDA5856ESE is support by RDA R-IOT SDK.

R-IoT is the IOT development platform of RDA, it composed of SDK, Eclipse IDE and some other auxiliary tools for debugging and audio calibration, etc. The SDK provides all the necessary components and standard APIs for the platform. The SDK is based on Eclipse which includes the cross-compile tools, connector to deploy and debug your software on the chip, basic library and sample code needed for embedded software development.

RDA has a variety of IoT chips for different requirements and scenarios. It has single Bluetooth, WIFI chip; also it has SoC combined with Bluetooth, WIFI and GSM for wireless network connection, and GPIO, I2C and etc. pins to connect sensor and peripheral device. What's more, RDA IoT chip supports co-exist technology which allows Bluetooth and WIFI work simultaneously. Via HAL (hardware abstract layer) R-IoT provides the support of all RDA IoT chips.

Meanwhile, R-IoT offers "micro-services" style architecture to facilitate software development and maintenance. IoT applications are based on these "micro-services", for instance, if we build a Bluetooth music player, we need to program with "BT micro-services". In most cases, these "micro-services" running in its own COS task and communicating with other services by sending or receiving COS event. The COS (Common OS) is an OS wrapper over C interface, it provides developers unified API so that developers could program with such interface without having to consider the native OS details.

Below is the diagram of R-IoT software architecture:

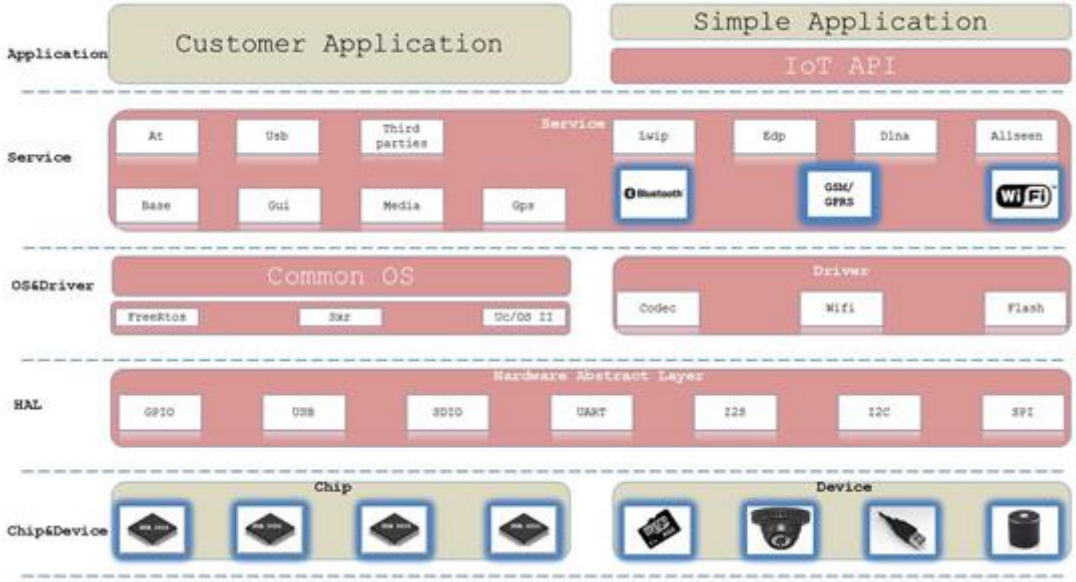


Figure 4 R-IoT Software Architecture

There are 5 layers:

- Chip and Device Layer
- HAL Layer

HAL is the module to configure chip and device; it tries to be common for all chips and devices, so the configuration must be very similar.

- OS and Driver Layer

R-IoT tries to support more OSes like RT-Thread, etc. without jeopardizing high layer service and application by introducing Common OS wrapper. Drivers are all external chip driver as opposed to chip drivers.

- Service Layer

These services are small building blocks, highly decoupled and provide user interface to application layer.

- Application Layer

In conclusion, R-IoT is almost a “turn-key” platform for IoT application development. The original SDK already had rich features for many mainstream IoT applications including home appliances and automation, asset tracking systems and consumer electronics devices, this enables the customer to rapid delivery its unique product to the market. Beyond that, its modularized and scalable software architecture makes it easier to support more OSes, chip, micro-services and cloud vendors, all these bring not only technical advantages but cost advantages as well.

For more information, please refer to RDA IOT SDK Development Manual and RDA IOT BT Development Manual.

25. Revision History

Revision	Date	Description
1.0	2017/02/04	Initial draft
1.1	2017/05/19	1. Update “Package and Pinout” 2. Add “GPIO Drive Current”
1.3	2017/12/06	Add Electrical Characteristics of BT and Audio

