

PRELIMINARY DATA SHEET

Revision: 1.2

Release date: 10 Dec 2017

RDA5995 WLAN SOC

Supports USB2.0 & SDIO for Connecting WLAN Activity to the host processor

1. General Description

RDA5995 highly integrates IEEE802.11b/g/n MAC/PHY/radio, power amplifier and antenna switch into one chip, specifically supports generic interfaces including USB2.0 and SDIO for connecting WLAN activity to the host processor. TCP/IP protocols along with SSL are included, providing improved link robustness, extended range, and increased performance. For the highest integration level, the required board space has been minimized and customer cost has been reduced. Manufacturers can easily and fast integrate RDA5995 on their product to enable a rapid time to market.

RDA5995 uses a compact 5×5mm² QFN package, 0.4mm pitch QFN-40.

1.1 Features

- CMOS single-chip fully-integrated radio, PHY and MAC
- 2.4GHz IEEE 802.11b/g/n
- Internal PA, LNA
- Data rates up to 150Mbps with 20/40 MHz bandwidth
- Dynamic TX power saving
- Low power listen mode
- Fast AGC control
- Support WPS,WMM

- Support WPA, WPA2, WEP, TKIP, CCMP
- Support STA, softAP, P2P, STA+softAp, STA+P2P
- Support A-MPDU, A-MSDU, HT-BA
- Light Weight TCP/IP protocol
- SDIO / SPI / UART/ USB2.0 interface allows simple interfacing to host device

1.2 Applications

- Tablet
- TV
- IP Camera
- AR/VR devices
- Mobile handset
- OTT set-top box
- Wi-Fi dongle
- Other multimedia devices

2. Block Description

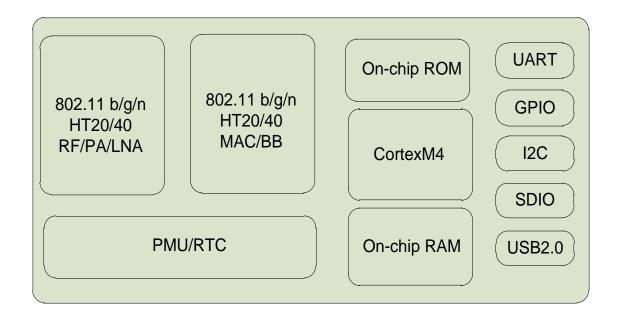


Figure 2-1 RDA 5995 Block Diagram

3. Functional Description

3.1 UART Interface Characteristics

RDA5995 supports 2 UARTs with configurable baud rate from 1200bps to 4Mbps.

3.2 I2C Interface Characteristics

RDA5995 supports 1 I2C standard interface. It supports master or slave I2C operation and 3 standard speed modes:

- 1. Standard mode (<100Kb/s)
- 2. Fast mode (<400Kb/s)
- 3. High-speed mode (<3.4Mb/s)

3.3 USB Interface Characteristics

RDA5995 supports USB2.0 interface.

4. General Specification

4.1 WLAN Section Electrical Characteristic

Table 4-1 DC Electrical Specification (Recommended Operation Conditions)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage from battery or LDO	3.3	4.0	5.0	V
T_{amb}	Ambient Temperature	-20	27	+70	$^{\circ}$
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V _{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
I _{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		VIO+0.3	V
V _{lna}	LNA Input Level			+10	dBm

4.2 Receive Performance Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		2412	-	2484	GHz
	1 Mbps DSSS		-92		dBm
Rx Sensitivity	2 Mbps DSSS		-90		dBm
802.11b @ 8% PER	5.5 Mbps DSSS		-88		dBm
	11 Mbps DSSS		-86		dBm
	6 Mbps OFDM		-90		dBm
	9 Mbps OFDM		-88		dBm
	12 Mbps OFDM		-86		dBm
Rx Sensitivity	18 Mbps OFDM		-85		dBm
802.11g @ 10% PER	24 Mbps OFDM		-82		dBm
	36 Mbps OFDM		-78		dBm
	48 Mbps OFDM		-76		dBm
	54 Mbps OFDM		-74		dBm
Rx Sensitivity	MCS0		-88		dBm
(802.11n, 20M)	MCS1		-85		dBm
@ 10% PER	MCS2		-83		dBm

	MCS3	-80	dBm
	MCS4	-77	dBm
	MCS5	-73	dBm
	MCS6	-71	dBm
	MCS7	-69	dBm
	MCS0	-87	dBm
	MCS1	-84	dBm
Des Compitinites	MCS2	-82	dBm
Rx Sensitivity	MCS3	-79	dBm
(802.11n, 40M) @ 10% PER	MCS4	-76	dBm
@ 10% FER	MCS5	-72	dBm
	MCS6	-70	dBm
	MCS7	-68	dBm
	11 Mbps (802.11b)	-3	dBm
Maximum Receive Level	54 Mbps (802.11g)	-8	dBm
	MCS7 (802.11n)	-8	dBm

4.3 Transmitter Performance Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range		2412	-	2484	MHz
	802.11b		18		dBm
Output Dawas	802.11g		15		dBm
Output Power	802.11n		14		dBm
	802.11n (HT40)		14		dBm
	802.11b		-20		dB
@ EVM	802.11g		-28		dB
W EVIVI	802.11n		-28		dB
	802.11n (HT40)		-28		dB

4.4 Power Consumption

PARAMETER	MIN	TYP	MAX	UNIT
WIFI OFF		22		uA
Deep Sleep		700		uA
RX mode		80		mA
TX mode (MCS7, duty ratio=100%)		220		mA

5. PINS Description

Table 5-1 Pin Types

Pin Type	Description
I/O	Digital input/output
Ι	Digital input
0	Digital output
A,I	Analog input
A,O	Analog output
A,I/O	Analog input/output
PWR	Power
GND	Ground

Table 5-2 RDA5995 Pins Description

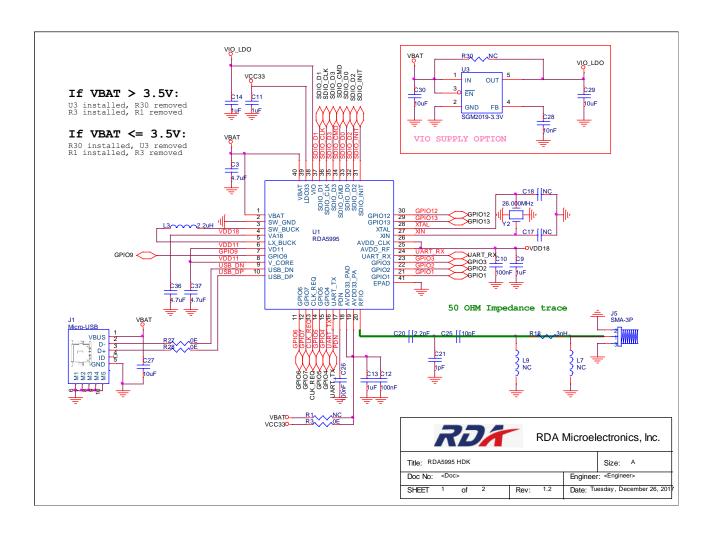
PIN	NO.	TYPE	DESCRIPTION
VBAT	1	PWR	buck power supply
SW_GND	2	GND	buck ground
SW_Buck	3	PWR	Switching node of buck
VA18	4	PWR	1.8V power output
LX_Buck	5	PWR	Switching output
VD11	6	PWR	1.1V power output
GPIO9	7	I/O	General purpose input/output
V_CORE	8	PWR	Digital core power in
USB_DN	9	I/O	USB negative signal
USB_DP	10	I/O	USB positive signal
GPIO6	11	I/O	General purpose input/output
GPIO7	12	I/O	General purpose input/output
CLK_REQ	13	I/O	Clock require signal
GPIO5	14	I/O	General purpose input/output
GPIO4	15	I/O	General purpose input/output
UART_TX	16	I/O	UART_TX
PDN	17	I	Power Down signal of the chip
AVDD33_PAD	18	PWR	3.3V PA driver power in
AVDD33_PA	19	PWR	3.3V PA power in
RFIO	20	A,I/O	WIFI transmitter output/receiver input
GPIO1	21	I/O	General purpose input/output
GPIO2	22	I/O	General purpose input/output
GPIO3	23	I/O	General purpose input/output
UART RX	24	I/O	UART RX
AVDD RF	25	PWR	1.8V RF power in
AVDD_CLK	26	PWR	1.8V clock power in
XIN	27	A,I	26M crystal input
XTAL	28	A,O	26M crystal output
GPIO13	29	I/O	General purpose input/output
GPIO12	30	I/O	General purpose input/output

The information contained herein is the exclusive property of RDA and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of RDA. Page 7 of 13

SDIO_INIT	31	I/O	SDIO interrupt signal
SDIO_D2	32	I/O	SDIO_Data2
SDIO_D0	33	I/O	SDIO_Data0
SDIO_CMD	34	I/O	SDIO_CMD
SDIO_D3	35	I/O	SDIO_Data3
SDIO_CLK	36	I/O	SDIO_Clock
SDIO_D1	37	I/O	SDIO_Data1
VIO	38	PWR	I/O power supply
LDO33	39	PWR	3.3V LDO output
VBAT	40	PWR	power supply

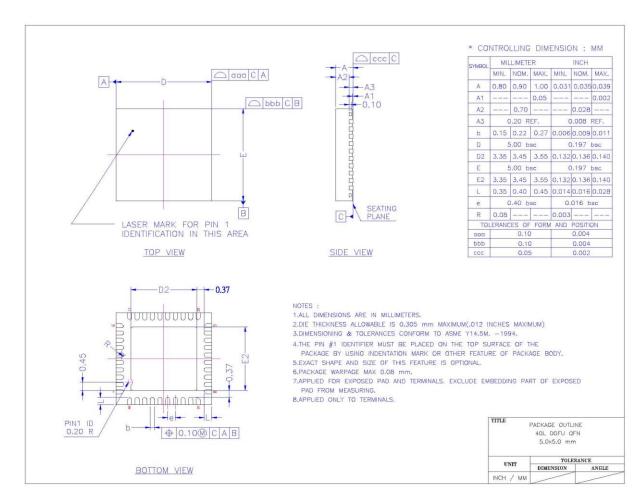
RDA5995 USB2.0 & SDIO WIFI Rev1.2

6. Application Circuit



RDA5995 USB2.0 & SDIO WIFI Rev1.2

7. Package Physical Dimension



8. Recommended Reflow Profile

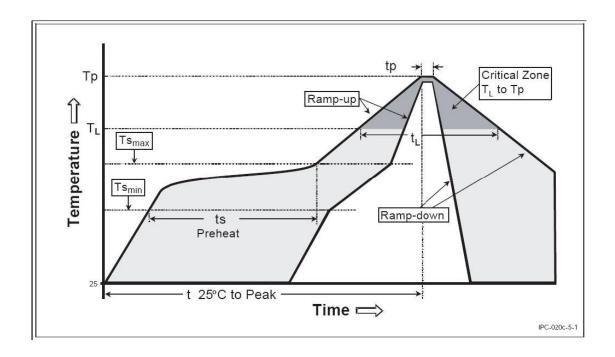


Figure.8-1 Classification Reflow Profile

Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate	3 °C/second max.	3 °C/second max.
(TSmax to Tp)		
Preheat		
-Temperature Min (Tsmin)	100 °C	150 ℃
-Temperature Max (Tsmax)	100 °C	200 °C
-Time (tsmin to tsmax)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183 °C	217℃
-Time (tL)	60-150seconds	60-150 seconds
Peak /Classification	See Table 8-2	See Table 8-3
Temperature(Tp)		
Time within 5 oC of actual Peak	10-30 seconds	20-40 seconds
Temperature (tp)		
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak	6 minutes max.	8 minutes max.
Temperature		

≥2.5mm

225 + 0/-5 °C

 Package Thickness
 Volume mm3
 Volume mm3

 <350 ≥350

 <2.5mm
 240 + 0/-5 °C
 225 + 0/-5 °C

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

225 + 0/-5 °C

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 ℃ *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 ℃ *

*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 $^{\circ}$ C. For example 260+ 0 $^{\circ}$ C) at the rated MSL Level.

Note 1: All temperature reference topside of the package. The temperature is measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 8-3.

Note 3: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package mays hill exist.

Note 5: Components intended for use in a "lead-free" assembly process shall be evaluated using the "lead free" classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

9. Change List

The following table summarizes revisions to this document.

REV	CHANGE DESCRIPTION			
Rev1.1	Preliminary version			
Rev1.2	Add general specification			

10. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and therefore is considered RoHS compliant.

11. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.

12. Disclaimer

The information provided here is believed to be reliable; RDA Microelectronics assumes no reliability for inaccuracies and omissions. RDA Microelectronics assumes no reliability for the use of this information and all such information should entirely be at the user's own risk. Specifications described and contained here are subjected to change without notice on the purpose of improving the design and performance. All of this information described herein should not be implied or granted for any third party. RDA Microelectronics does not authorize or warrant any RDA products for use in the life support devices or systems.



Copyright@2016 RDA Microelectronics Inc. All rights reserved

For technical questions and additional information about RDA Microelectronics Inc.:

Website: www.rdamicro.com Mailbox: info@rdamicro.com

RDA Microelectronics (Beijing), Inc.

Tel: +86-10-58286588 Fax: +86-10-58286599