Nishant Jindal

LOGIC GATE

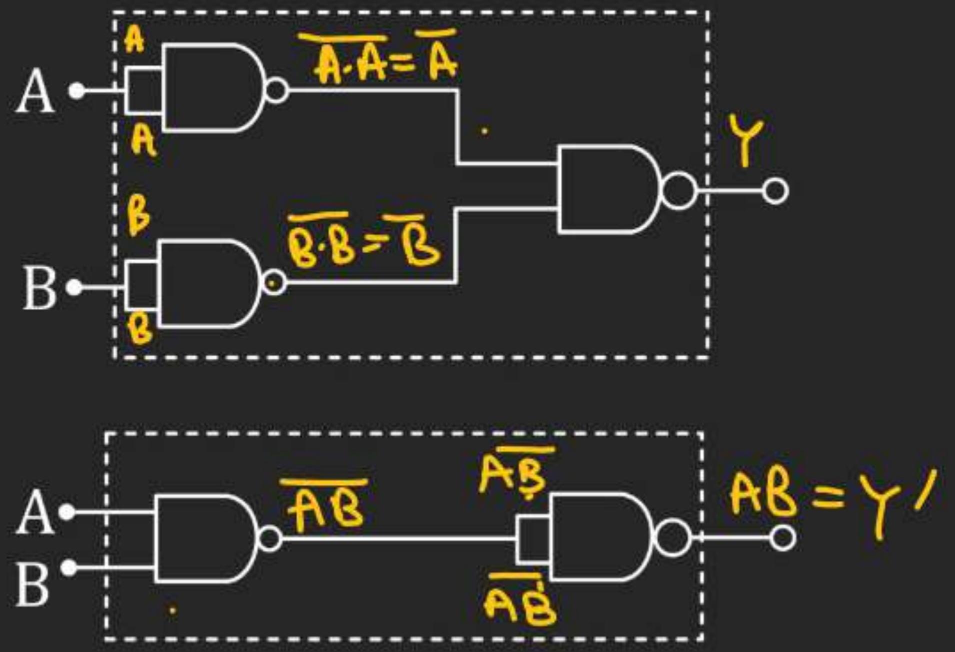
Q.8 The combination of 'NAND' gates shown here under (figure) are equivalent to

(A) An OR gate and an AND gate respectively $A \cdot A = A$

(B) An AND gate and a NOT gate respectively

(C) An AND gate and an OR gate respectively

(D) An OR gate and a NOT gate respectively.



$\overline{A \cdot B} = \bar{A} + \bar{B}$

$Y = \overline{\bar{A} \cdot \bar{B}}$

$= \bar{\bar{A}} + \bar{\bar{B}}$

$= A + B \Rightarrow$ OR gate

$Y' = AB$

(AND) gate

$\overline{\overline{AB} \cdot \overline{AB}}$

$\overline{\overline{AB}} = AB$

LOGIC GATE

Q.9 The following truth table corresponds to the logic gate where A and B represent inputs and X represents output.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(A) NAND

(B) AND

(C) XOR

(D) OR

LOGIC GATE

Q.10 For the given combination of gates, if the logic states of inputs A, B, C are as follows $A = B = C = 0$ and $A = B = 1$, $C = 0$, then the logic states of output D are

gates

(A) 0,0

(B) 0,1

(C) 1,0

~~(D) 1,1~~

$D = \overline{\underbrace{(A+B)}_{x}\cdot C}$

$D = \overline{A+B} + \overline{C}$

$D = (\overline{A}\cdot\overline{B} + \overline{C})$

$\downarrow$

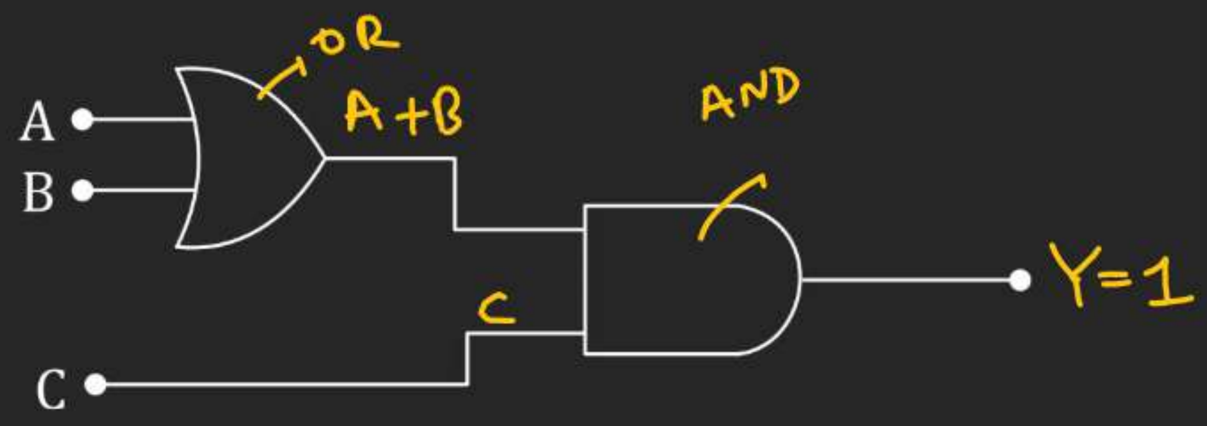
For 1st input → 1

$\overline{X\cdot C} = \overline{X} + \overline{C}$

$\overline{A+B} = \overline{A}\cdot\overline{B}$

LOGIC GATE

Q.11 To get an output 1 from the circuit shown in the figure, the input must be



(A) $A = 0, B = 1, C = 0$

(B) $A = 1, B = 0, C = 0$

(C) $A = 1, B = 0, C = 1$

(D) $A = 1, B = 1, C = 0$

$Y = \underbrace{(A+B)}_{1} \cdot C$

$1 = 1 \quad 1$

LOGIC GATE

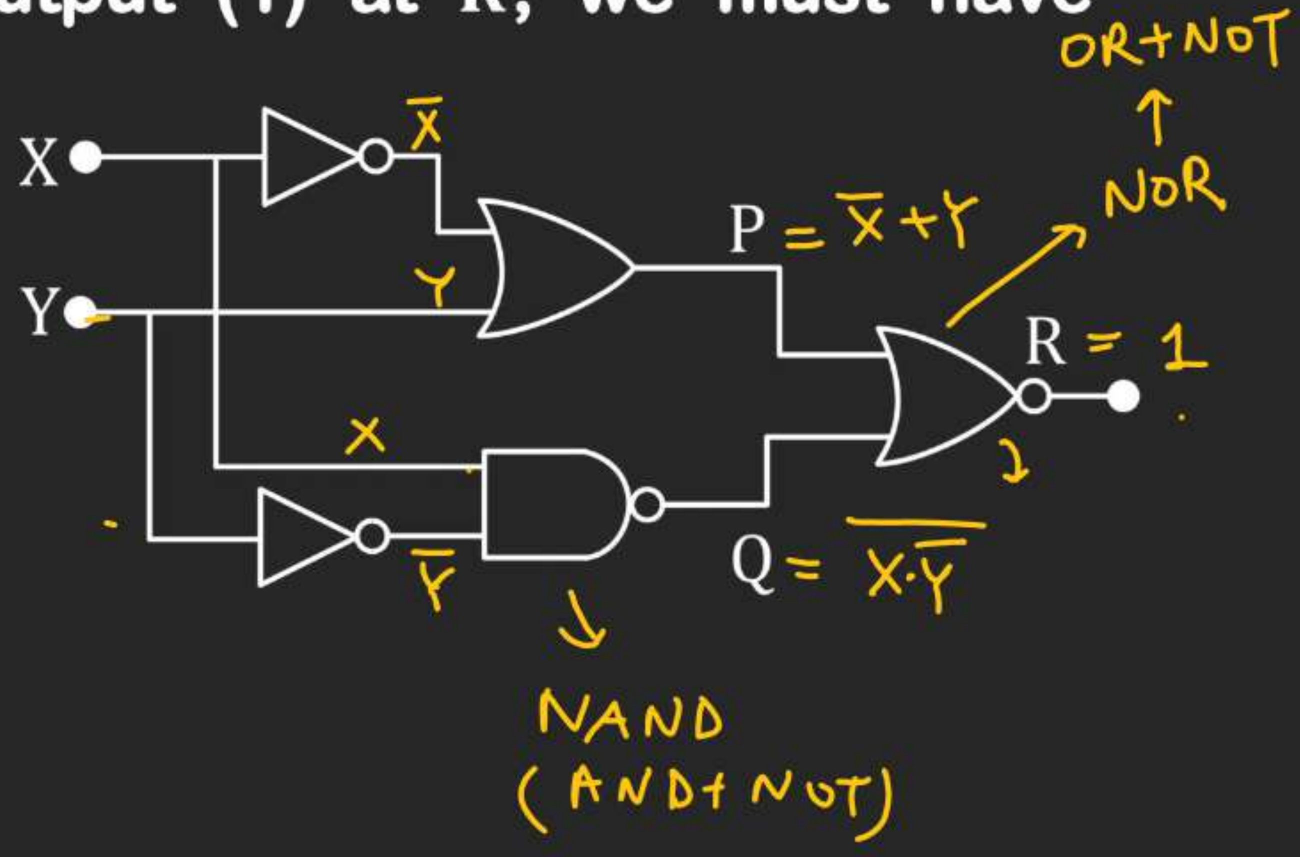
Q.12 The figure below gives a system of logic gates. From the study of truth table, it can be found that to produce a high output (1) at R, we must have

(A) $X = 0, Y = 1$

(B) $X = 1, Y = 1$

(C) $X = 1, Y = 0$

(D) $X = 0, Y = 0$



$$R = \overline{P + Q}$$

$$R = \bar{P} \cdot \bar{Q}$$

$$= \overline{(\bar{X} + Y)} \cdot \overline{\overline{(X \cdot \bar{Y})}}$$

$$= (\bar{\bar{X}} \cdot \bar{Y}) \cdot (X\bar{Y})$$

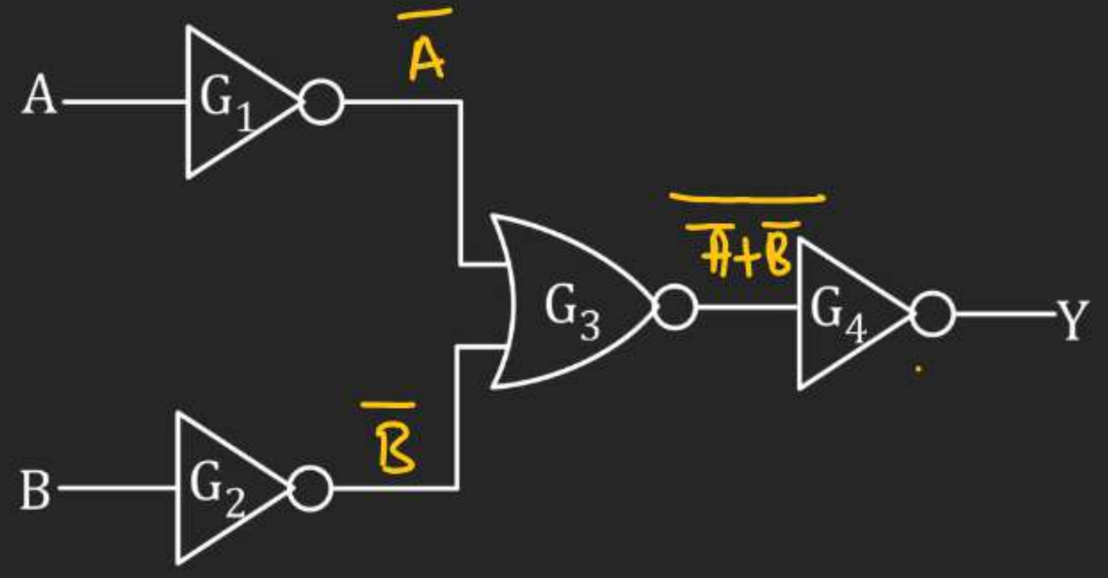
$$= (X\bar{Y}) \cdot (X\bar{Y})$$

$$R = (X\bar{Y})$$

1 0

LOGIC GATE

Q.13 The combination of gates shown below produces



(A) AND gate

(B) XOR gate

(C) NOR gate

(D) NAND gate ✓

$$Y = \overline{\overline{\bar{A}+\bar{B}}}$$

$$Y = (\bar{A}+\bar{B})$$

$$Y = \overline{A \cdot B}$$

AND + NOT

LOGIC GATE

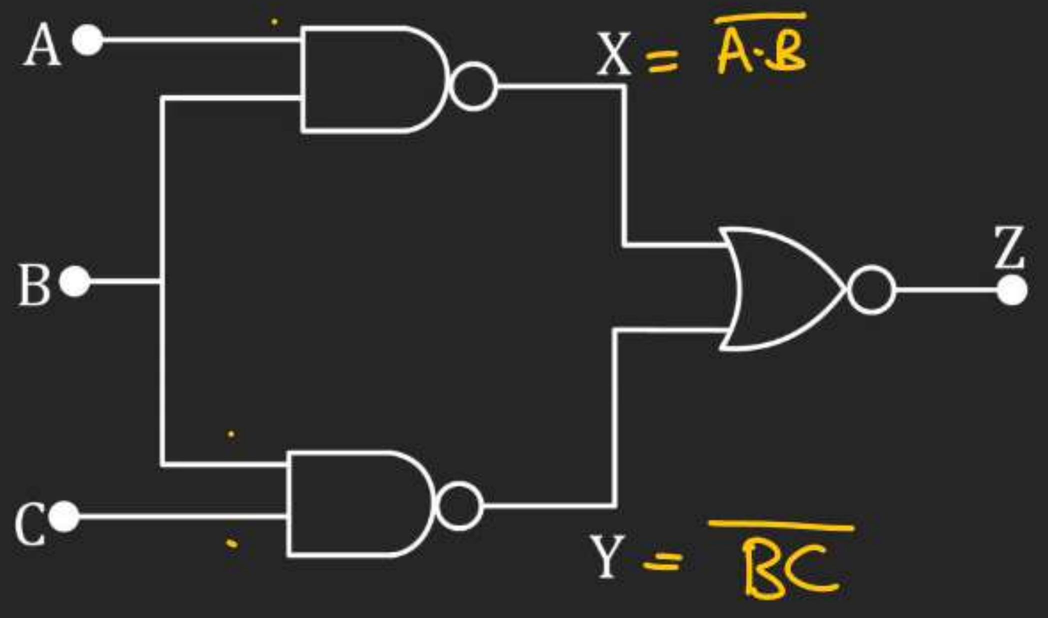
Q.14 The figure shows two NAND gates followed by a NOR gate. The system is equivalent to the following logic gate

(A) OR

(B) AND

(C) NAND

(D) None of these



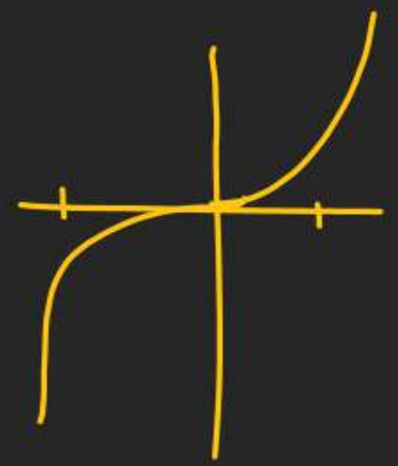
$$Z = \overline{\overline{A\cdot B} + \overline{BC}}$$

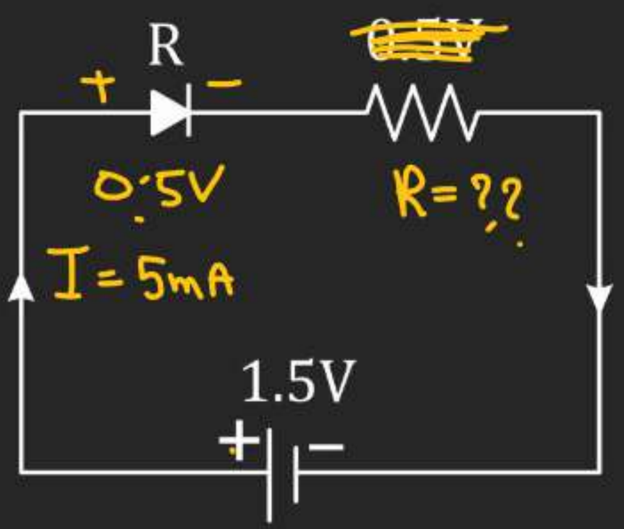
$$Z = \left(\overline{\overline{A\cdot B}}\right)\cdot\left(\overline{\overline{BC}}\right)$$

$$Z = AB\cdot BC$$

$$Z = ABC$$

Q.1 A p-n junction diode when forward biased has a drop of $0.5\ \mathrm{V}$ which is assumed to be independent of current. The current in excess of $10\ \mathrm{mA}$ through the diode produces a large Joule heating which damages (burns) the diode. If we want to use a $1.5\ \mathrm{V}$ battery to forward bias the diode, what should be the value of resistor used in series with the diode so that the maximum current does not exceed $5\mathrm{mA}$?





$$1.5 - 0.5 - iR = 0.$$

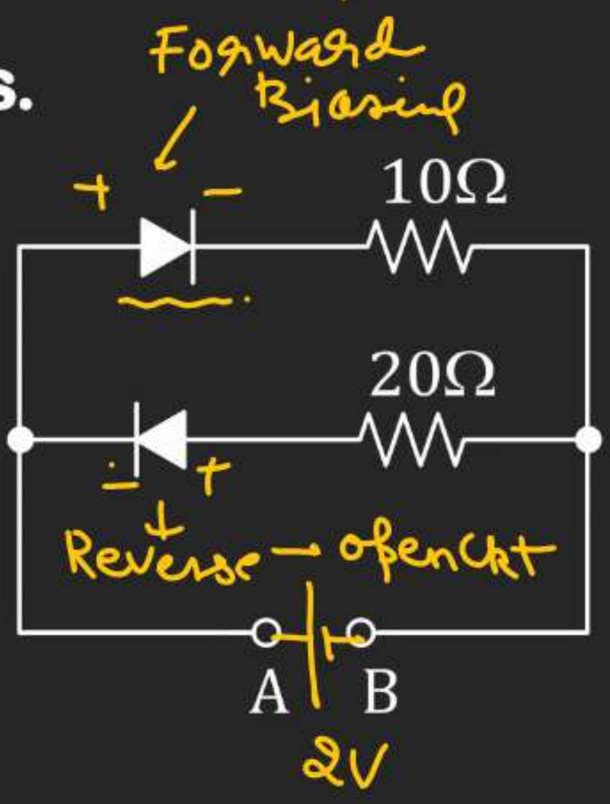
$$1 = iR$$

$$R = \frac{1}{5\times10^{-3}} = \frac{1000}{5} = 200\ \Omega$$

Q.2 A battery of 2 V may be connected across the points A and B, as shown in Fig. Find the current drawn from the battery if the positive terminal is connected to (i) the point A and (ii) the point B. Assume that the resistance of each diode is zero in forward bias and infinity in reverse bias.

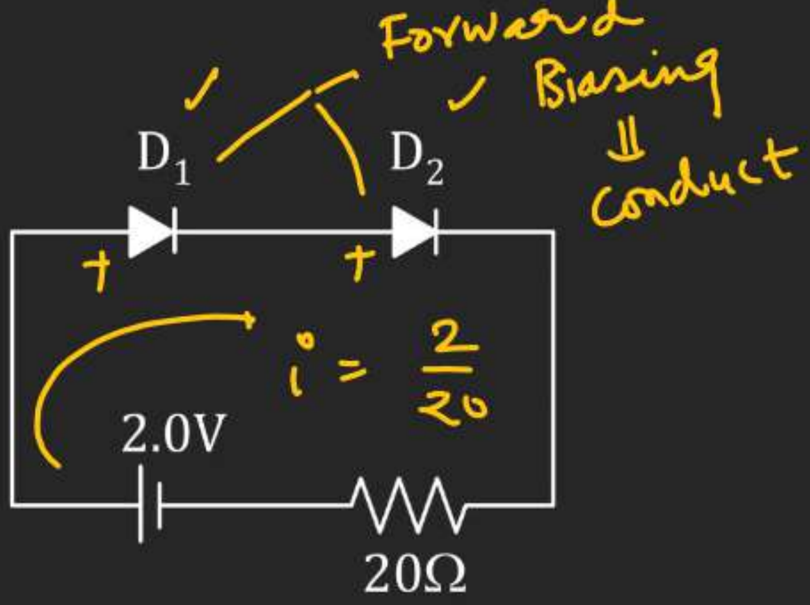
i) $I = \frac{2}{10} = \frac{1}{5} = 0.2A$

ii) $I = \frac{2}{20} = \frac{1}{10} = 0.1A$

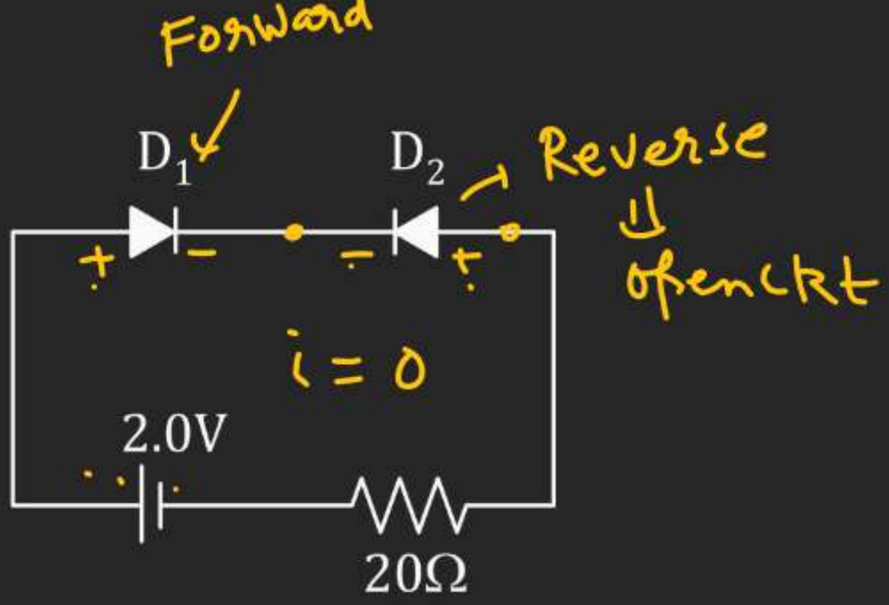


Q.3 Determine the currents through the resistances of the circuits shown in Fig.

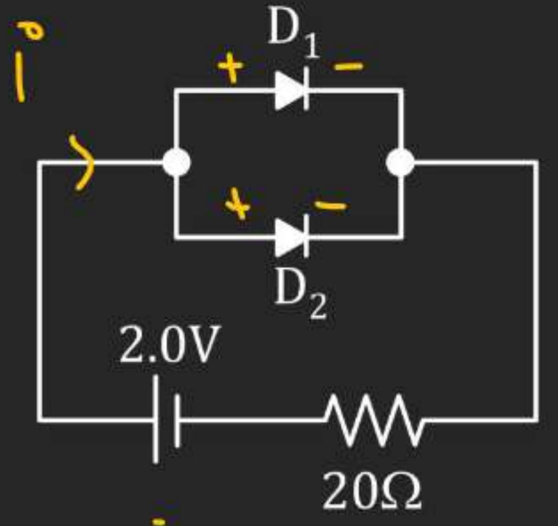
(A)



(B)

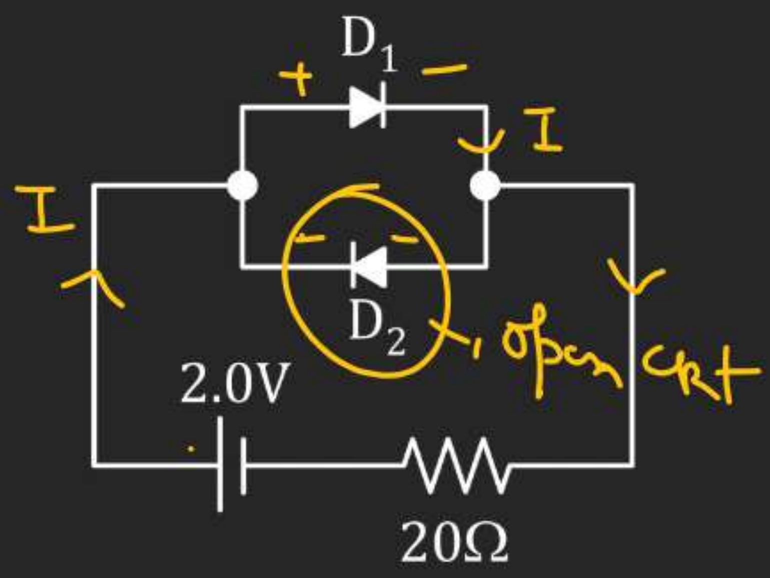


(C)



$i = \frac{2}{20}$ Amp

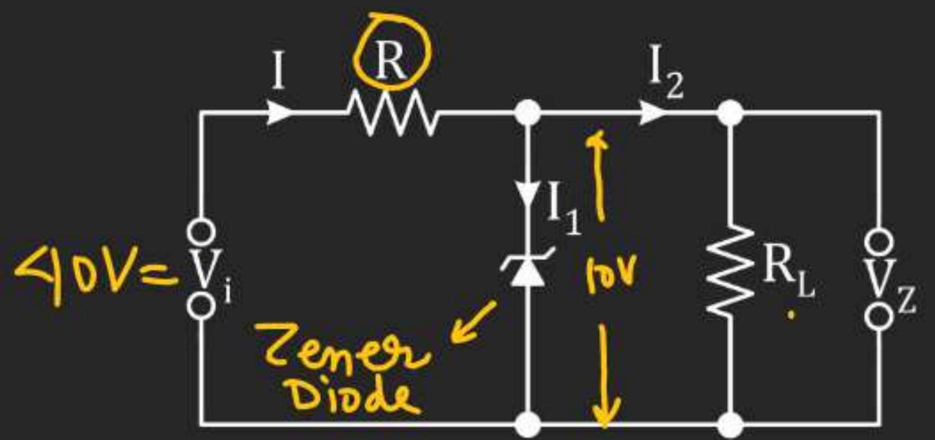
(D)



$I = \frac{2}{20}$ Amp.

Q.4 A 10 V zener diode along with a series resistance is connected across a 40 V supply. Calculate the minimum value of the resistance required, if the maximum zener current is 50 mA.

Solution. In Fig., $V_i = 40\text{ V}$, $I_1 = 50\text{ mA}$



$V_z = 10V$

$R \rightarrow R_{min}$

$I_1 \rightarrow$ Maximum

$I = I_1 + I_2'$

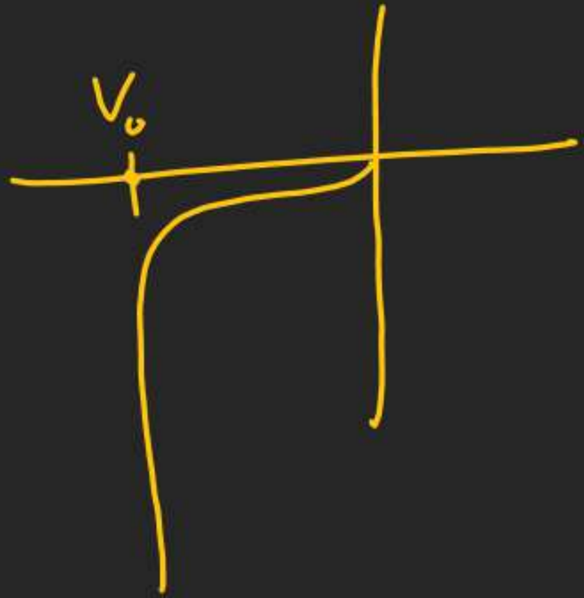
$(I_1)_{max}$ 0

$40 - 10 = IR$

$R_{min} = \dfrac{40-10}{I_{max}}$

$50mA = I = I_1$

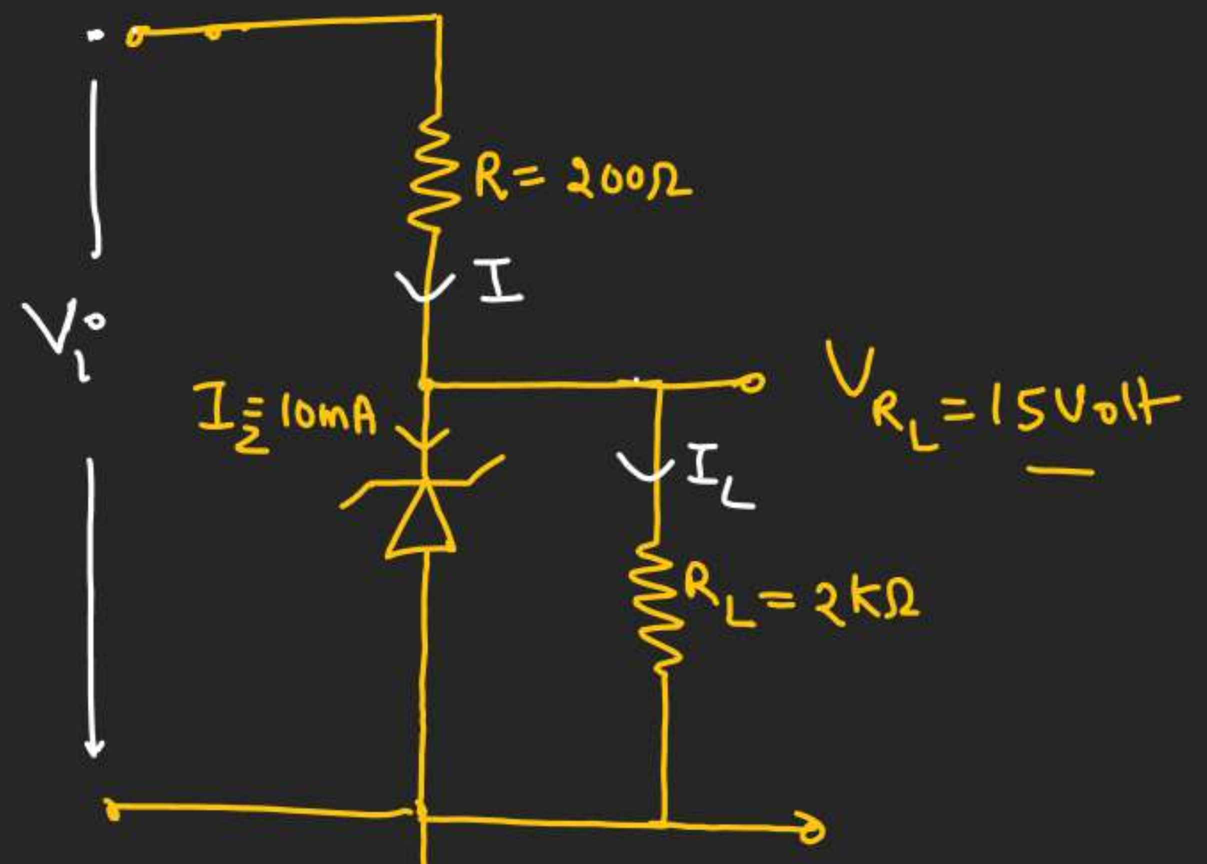
$= \dfrac{30}{50 \times 10^{-3}} = \dfrac{3}{5} \times 1000 = 600\Omega$



Q.5 In Fig. what is the voltage needed to maintain $15\,\text{V}$ across the load resistance R_L of $2\,\text{K}\Omega$ assuming that the series resistance R is 200Ω and the zener requires a minimum current of $10\,\text{mA}$ to work satisfactorily? What is the zener rating required?

$$I = I_L + I_Z$$
$$= (7.5 + 10)$$
$$= \underline{17.5\,\text{mA}}$$

$$I_L = \frac{15}{2 \times 10^3}$$
$$I_L = 7.5\,\text{mA}$$



$$V_R = I \cdot R = (17.5 \times 10^{-3} \times 200)$$
$$= 35 \times 10^{-1}$$
$$= \underline{3.5\,\text{Volt}}$$

$$V_i = (3.5 + 15)\,\text{Volt}$$
$$= \underline{18.5\,\text{Volt}}$$

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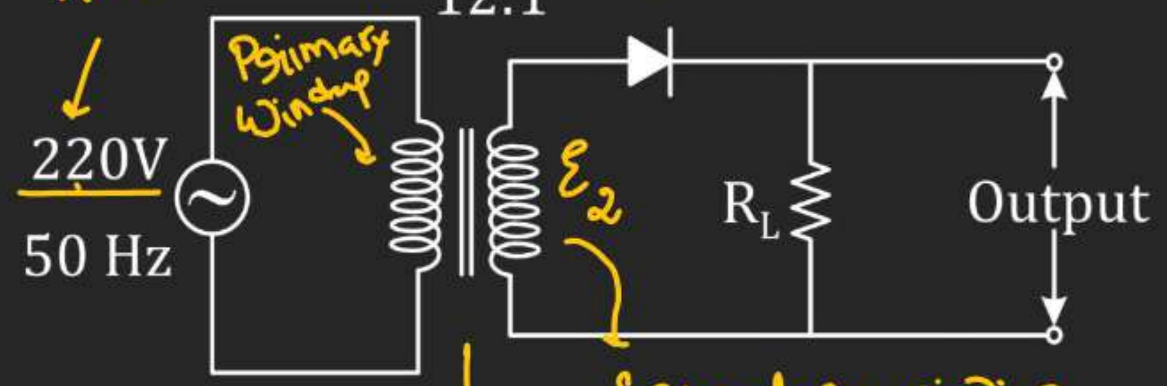
Q.6 Find the average value of dc voltage that can be obtained from the half-wave rectifier of Fig. Assume the diode to be ideal one.

$\frac{N_1}{N_2} = \frac{12}{1}$

R.M.S



secondary winding

Transformer.

For half Wave Rectifier.

$$\left[\begin{array}{l} V_{dc} = \frac{V_0}{\pi} \\ I_{dc} = \frac{I_0}{\pi} \end{array}\right]$$

$$\frac{\mathcal{E}_1}{\mathcal{E}_2} = \frac{N_1}{N_2} = \frac{I_2}{I_1}$$

2 → Secondary Winding

1 → Primary winding

$$\mathcal{E}_2 = \frac{N_2}{N_1} \times \mathcal{E}_1$$ ← peak value.

$$= \frac{1}{12} \times (220 \times \sqrt{2})$$

$$=$$

$$V_{os} = \mathcal{E}_2$$

$$(V_{os})_{dc} = \frac{V_{os}}{\pi} = \left(\frac{\mathcal{E}_2}{\pi}\right)$$

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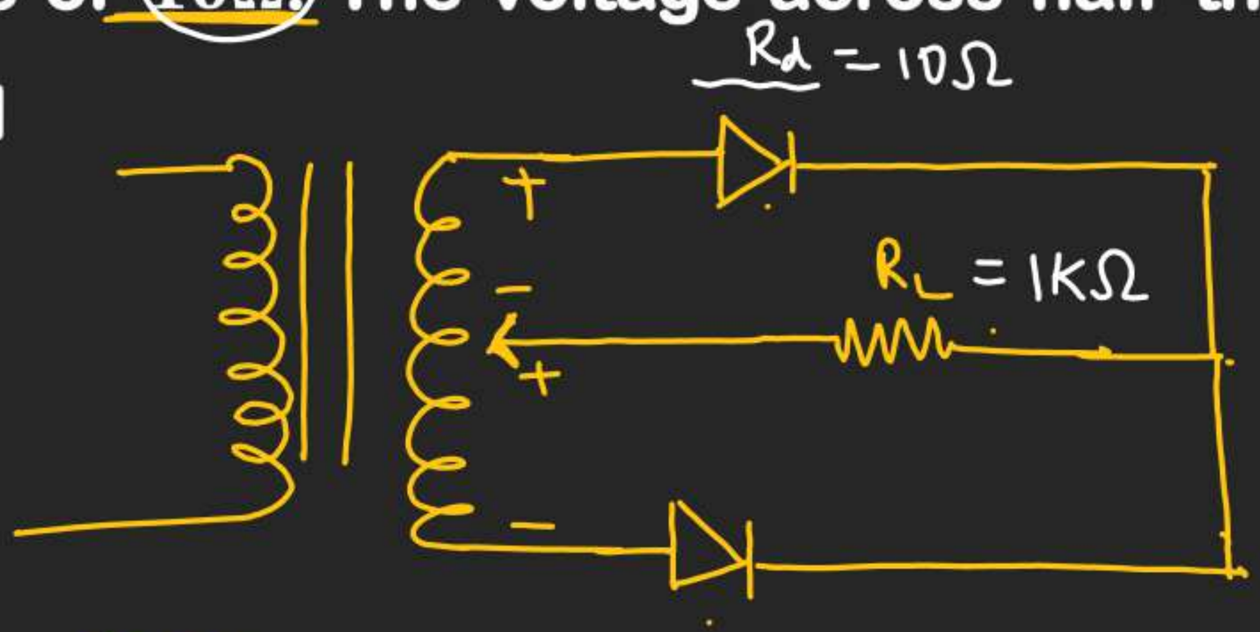
tape

Q.7 In a centre trap full wave rectifier, the load resistance $R_L = 1k\Omega$. Each diode has a forward bias dynamic resistance of 10Ω. The voltage across half the secondary winding is 220 sin 314t. Find

(i) the peak value of current

(ii) the dc value of current and

(iii) the rms value of current.



$$i_{peak} = \frac{220}{R_d + R_L} = \left(\frac{220}{10+1000}\right) = \_\_\_\_\_\_$$

$$I_{dc} = \left(\frac{2I_0}{\pi}\right)$$

$$I_{rms} = \frac{I_{peak}}{\sqrt{2}} = \_\_\_\_$$

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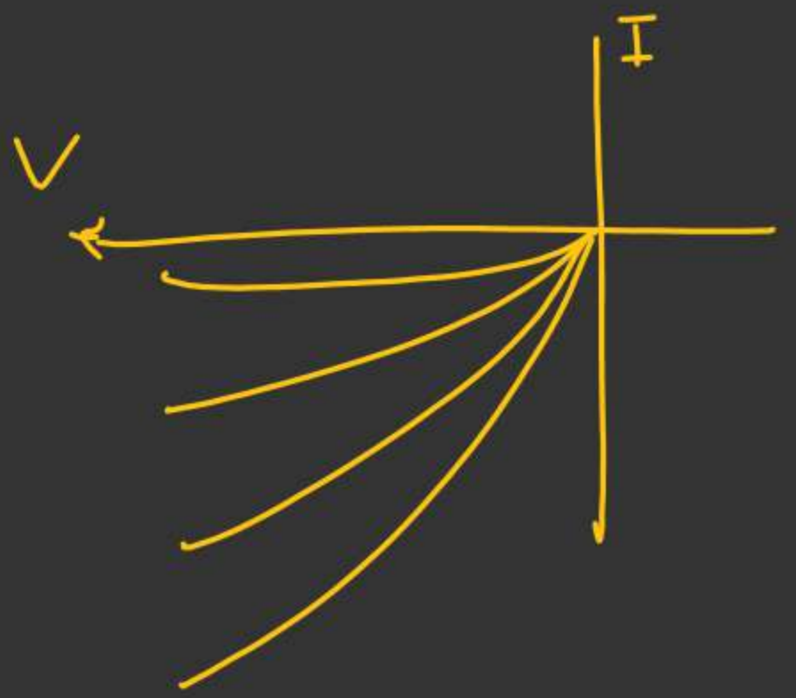
H.W:

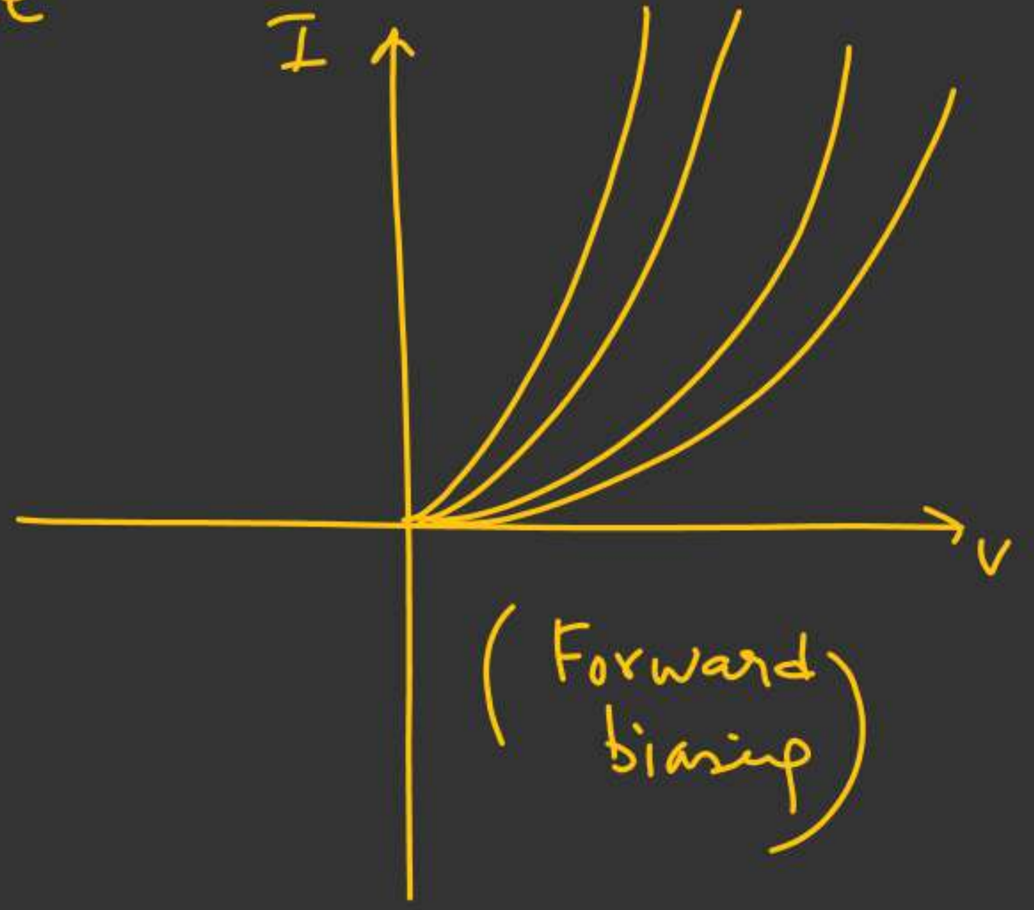
V-I Characteristics

① Photodiode

↳ (Work on Reverse biasing)



② L.E.D



③ Solar diode