

1. Logic Gates & Boolean Algebra.

Gates are two types. They are.

* Basic Gates

AND

OR

NOT

* Universal Gates.

NAND

NOR

~~Ex~~ Exclusive OR

~~Ex~~clusive NOR

Gate Means "Digital circuit"

AND gate :-

* The output of AND gate is '1' (or) True if two or more inputs where

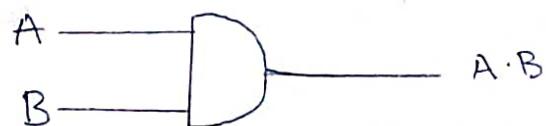
true.

* AND gate can be denoted as "Cor" dot.

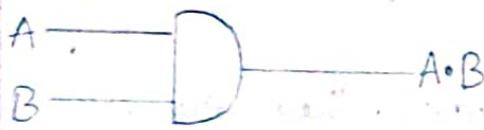
* "•" is used as multiplication of two

inputs.

* Symbol of AND gate



Truth Table :-



| Input | | output |
|-------|---|-------------|
| A | B | $A \cdot B$ |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

OR GATE :-

- * The output of the OR gate is true, if any one input is true.
- * Symbol of OR gate :-



Truth Table :-

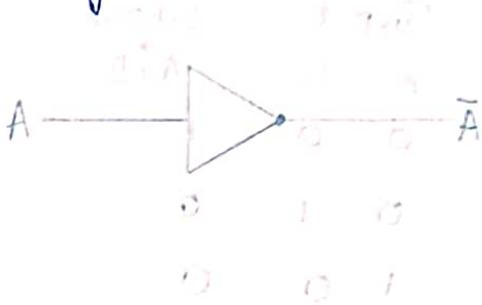
| Input | | output |
|-------|---|---------|
| A | B | $A + B$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

NOT GATE :-

In this gate, single input and single output

- * The output of NOT gate is complement (or) inverse of the input.

* Symbol of NOT Gate

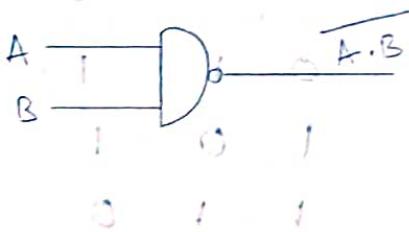


Truth Table :-

| Input | Output |
|-------|-----------|
| A | \bar{A} |
| 0 | 1 |
| 1 | 0 |

NAND Gate

- * Any two inputs is true, then the output is false.
- * If all the inputs of NAND gate are true. Then output is false, but in remaining cases it is false.
- * symbol of NAND gate is. Truth Table.

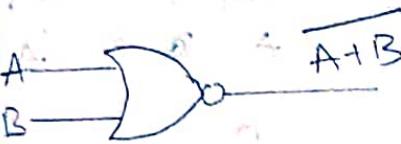


| Input | Output | |
|-------|--------|------------------------|
| A | B | $\overline{A \cdot B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

NOR Gate :-

If all the inputs are low then the output is high. The outputs all are quite opposite to OR gate.

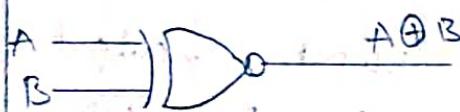
symbol of NOR gate is



| Input | | Output |
|-------|---|--------|
| A | B | $A+B$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

* Exclusive -OR gate :-

- * The outputs of the exclusive -OR gate is '1', where there are odd number of "ones" at the input.
- * The output of the exclusive OR gate is '1'.
- * Symbol of Ex-OR is



| Input | | Output |
|-------|---|--------------|
| A | B | $A \oplus B$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Exclusive NOR gate

- * The output of the Ex-NOR is when there are even number of '1' and all inputs are zero "0". The gate is quite opposite to Ex-OR gate.

* symbol of Ex-NOR gate :-

Truth Table

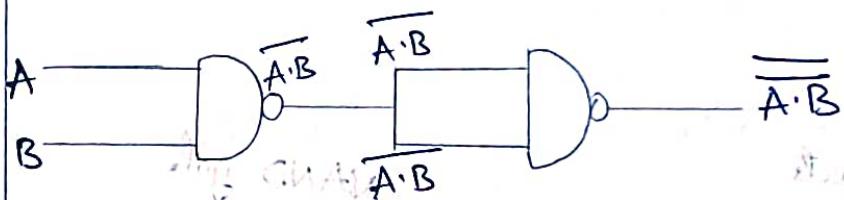
| Input | | Output |
|-------|---|--------------|
| A | B | $A \oplus B$ |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |



stop writing now

Basic gates using NAND gate:-

AND gate using NAND gate.



AND gate

| Input | | Output |
|-------|---|-------------|
| A | B | $A \cdot B$ |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

NAND gate

| Input | | Output |
|-------|---|------------------------|
| A | B | $\overline{A \cdot B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

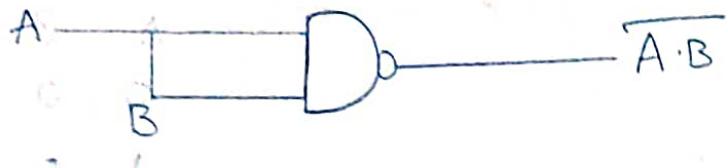
NOT gate using NAND gate.

NOT gate

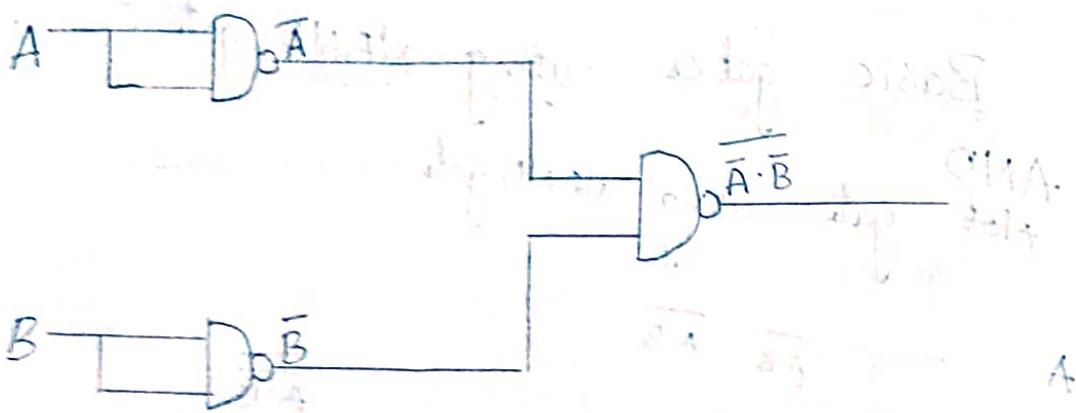
| Input | | Output |
|-------|----------------|--------|
| A | \overline{A} | |
| 0 | 1 | |
| 1 | 0 | |

NAND gate

| Input | | Output |
|-------|---|------------------------|
| A | B | $\overline{A \cdot B}$ |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |



OR gate using NAND gate:



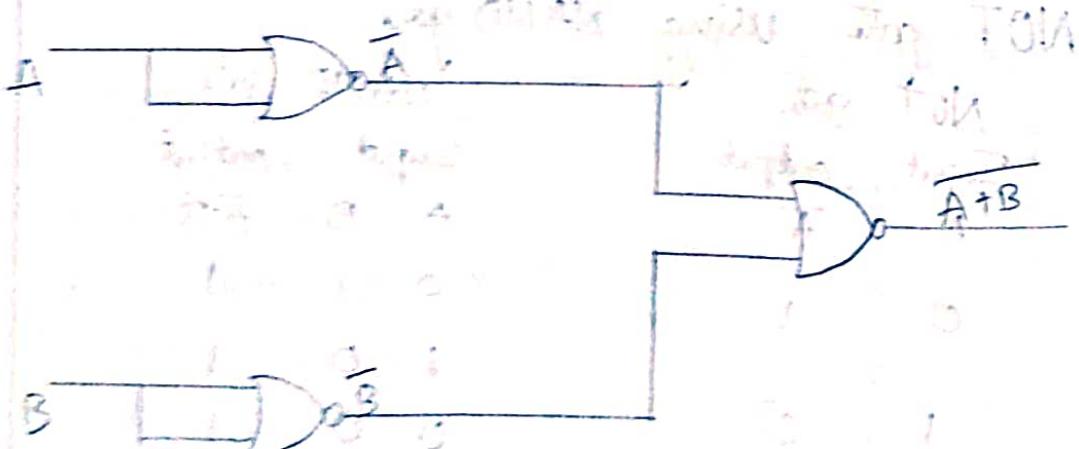
OR gate

NAND gate

| Input | | Output |
|-------|---|--------|
| A | B | $A+B$ |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

| Input | | Output |
|-------|---|-------------------------|
| A | B | $\bar{A} \cdot \bar{B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

AND gate using NOR gate:



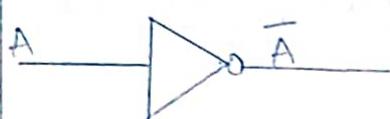
AND gate

| Input | Output | |
|-------|--------|-------------|
| A | B | $A \cdot B$ |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

NOR gate

| Input | Output | |
|-------|--------|------------------|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

NOT gate using NOR gate



NOT gate = $\overline{A+A}$

$$(\overline{A+A}) + (\overline{A+A}) = 0 + 1 = 1$$

NOT gate

| Input | Output |
|-------|----------------|
| A | \overline{A} |
| 1 | 0 |
| 0 | 1 |

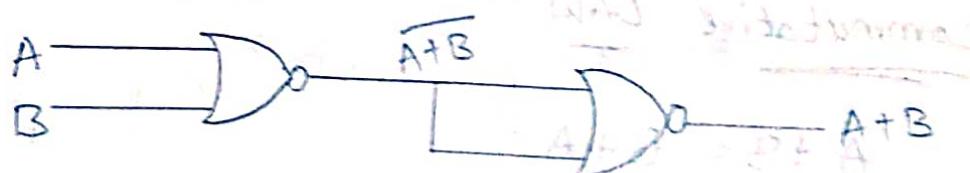
NOR gate

| Input | Output | |
|-------|--------|------------------|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

Law :- $A+A = A$

$$A \cdot A = A$$

OR gate using NOR gate



$$A + A = A$$

OR gate

| Input | Output | |
|-------|--------|-------|
| A | B | $A+B$ |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

NOR gate

| Input | Output | |
|-------|--------|------------------|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

$$= \overline{\overline{A+B} + \overline{A+B}}$$

$$\Rightarrow (\overline{A+B}) + (\overline{A+B})$$

$$\Rightarrow (A+B) + (A+B)$$

$$\Rightarrow A+B$$

BOOLEAN LAWS

AND LAW

$$A \cdot 0 = 0$$

$$A \cdot 1 = A$$

$$A \cdot A = A$$

$$A \cdot \overline{A} = 0$$

OR LAW

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + A = A$$

$$A + \overline{A} = 1$$

NOT LAW:

$$A + A \cdot A$$

$$\overline{\overline{A}} = A$$

Commutative LAW:

$$A + B = B + A \rightarrow$$

$$A \cdot B = B \cdot A$$

Associative LAW

$$A + (B + C) = (A + B) + C = A + B + C$$

$$A(B \cdot C) = (A+B) \cdot (A+C)$$

Distributive LAW

$$A(B+C) = AB + AC$$

$$A + (BC) = (A+B)(A+C)$$

Auxiliary Laws

$$A + A \cdot B = A \rightarrow (A+A \cdot B) = A \quad A(1+B) = A$$

$$A + \bar{A} \cdot B = A + B$$

$$(A+B)(A+C) = AB + BC$$

$$AB + BC + \bar{B}C = AB + C$$

$$1. (A+B)(A+\bar{B})$$

$$A \cdot A + A \cdot \bar{B} + B \cdot A + B \cdot \bar{B}$$

$$\Rightarrow A + A\bar{B} + BA + 0$$

$$\Rightarrow A + A(B + \bar{B})$$

$$\Rightarrow A + A(1)$$

$$\Rightarrow A + A$$

$$\Rightarrow A.$$

$$(2) ABC + A\bar{B}C + A\bar{B}\bar{C}$$

$$\Rightarrow AC(B + \bar{B}) + A\bar{B}\bar{C}$$

$$\Rightarrow AC + A\bar{B}\bar{C}$$

$$\Rightarrow A(C + \bar{B}\bar{C})$$

$$\Rightarrow A(C + B) + A(\bar{C} + \bar{B})$$

$$\Rightarrow AB + A\bar{C} + A\bar{B}$$

$$\Rightarrow A(B + \bar{C} + \bar{B})$$

$$\Rightarrow A(B + \bar{C})$$

$$3. (A+B)(A+\bar{B})(\bar{A}+C)$$

$$(A \cdot A + A\bar{B} + BA + B\bar{B})(\bar{A}+C) \quad \text{using } A+A = A$$

$$\Rightarrow (A + A\bar{B} + BA + 0)(\bar{A}+C) \quad \text{using } 0 \cdot A = 0$$

$$\Rightarrow A + A(B+\bar{B})(\bar{A}+C) \quad \text{using } B+\bar{B} = 1$$

$$\Rightarrow (A+A)(\bar{A}+C)$$

$$\Rightarrow A(\bar{A}+C)$$

$$\Rightarrow A\bar{A} + AC \Rightarrow AC$$

$$4. AB + A(B+C) + B(B+C)$$

$$AB + AB + AC + BB + BC$$

$$\Rightarrow AB + AC + B + BC$$

$$\Rightarrow AB + AC + B(1+C) \quad \text{using } 1+C = 1$$

$$\Rightarrow AB + AC + B$$

$$\Rightarrow B(A+1) + AC$$

$$= B(1+1) + AC \quad \text{using } 1+1 = 2$$

$$\Rightarrow B + AC$$

$$5. (A+B)(A+C)$$

$$AA + AC + BA + BC$$

$$A + AC + BA + BC$$

$$A(1+C) + BA + BC$$

$$\Rightarrow A + BA + BC$$

$$\Rightarrow A(1+B)BC$$

$$\Rightarrow A + BC$$

$$6. 0 + A = A$$

$$0 \cdot A = 0$$

$$7. 1 + A = 1$$

$$A = A$$

$$8.(a) \bar{A} + A = 1$$

$$(b) \bar{A} \cdot A = 0$$

$$9. (a) A + \bar{A}B = A + B$$

$$(b) A(\bar{A} + B) = A \cdot B$$

$$10. \bar{\bar{A}} = A$$

$$A + B = A + B(1)$$

$$= A + B(\bar{A} + A)$$

$$= A + B\bar{A} + BA \\ AB = BA$$

$$S: A(\bar{A} + B) = \bar{A}B$$

$$= A(1) + \bar{A}B$$

$$S: 1 + \bar{A}B$$

$$\Rightarrow A + \bar{A}B$$

DE-MORGAN'S THEOREM :-

The sum of two or more variables with complement is equal to the product of individual complements.

$$\underline{I \text{ law:}} \quad \overline{A+B} = \bar{A} \cdot \bar{B}$$

$$\overline{A+B+C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$

The complement of sum is equal to the product of individual complements.

II law :-

The whole complement two or more variables with complement.

* The complement of the product is equal to the sum of the complements. $A = \bar{A}$

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

$$\overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$

1. ~~$\overline{\overline{AB} + A \cdot \bar{B}}$~~

$$D = A \cdot \bar{B}$$

$$P + A = \bar{A} + A \quad (\text{P})$$

$$\bar{A} \cdot A = (\bar{A} + \bar{A})A \quad (\text{d})$$

A.

$$\overline{\overline{A+B} + A \cdot \bar{B}}$$

$$A = \bar{A}^2 \text{ of}$$

$$\overline{\overline{A+B}} + \overline{A \cdot \bar{B}}$$

$$A+B \cdot \bar{A} \cdot B$$

$$B(A+\bar{A})$$

$$\Rightarrow \bar{A}B$$

$$\text{So, } \bar{A}B \text{ is the simplified form}$$

$$\text{Also, } \bar{B} \cdot \bar{A} + \bar{A} \cdot B$$

$$\text{Also, } \bar{B} \cdot \bar{A} + \bar{B} \cdot A$$

$$\text{So, } \bar{B} \cdot \bar{A} \text{ and } \bar{B} \cdot A$$

$$\text{So, } \bar{B} \cdot \bar{A} \text{ and } \bar{B} \cdot A$$

$$\overline{\overline{A+B}} + \overline{\overline{A}\overline{B}}$$

$$\cancel{\overline{A+B}} \cdot \cancel{\overline{A}\overline{B}}$$

$$\Rightarrow (A+B) \cdot (\overline{A}\overline{B})$$

$$\Rightarrow A\overline{A}\overline{B} + B\overline{A}\overline{B}$$

$$\Rightarrow \overline{A}\overline{B}$$

$$\overline{\overline{A+BC}} + \overline{\overline{A}\overline{B}}$$

$$\overline{\overline{A+BC}} + \overline{\overline{A}\overline{B}}$$

$$\overline{\overline{A+BC}} + \overline{A}\overline{B}$$

$$\overline{\overline{A+\overline{B}+\overline{C}}} + A\cdot\overline{B}$$

$$A \cdot B \cdot C + A \cdot \overline{B}$$

$$A (BC + \overline{B})$$

$$A (B+C)$$

$$\overline{\overline{AB+BC(B+C)}} + \overline{AB}$$

$$\overline{\overline{AB}} + \overline{\overline{BC} \cdot (B+C)} + \overline{\overline{AB}}$$

$$\overline{\overline{AB}} + \overline{\overline{BC} + \overline{C}(B+C)} + \overline{\overline{AB}}$$

$$\overline{\overline{AB}} + \overline{\overline{BC}} + \overline{\overline{B}} + \overline{\overline{C}} + \overline{\overline{AB}}$$

$$\overline{\overline{A+\overline{B}}} + \overline{\overline{B+\overline{C}}} + \overline{\overline{B}} + \overline{\overline{C}} + A + B$$

$$B(A+C) \quad B(A+C)$$

$$(B+B)(A+C)$$

$$B(A+C)$$

Canonical forms

Two types of expressions are directly obtainable from a truth table.

- * Sum - of - products (minterms)

- * products - of - sums (Maxterm)

These are two to represent an equation

by using truth table

| A | B | $f(A, B)$ | Minterms (sum of products) | Maxterms (products of sums) |
|---|---|-----------|-------------------------------|---------------------------------|
| 0 | 0 | 0 | | |
| 1 | 0 | 0 | | |
| 0 | 1 | 1 | $(\bar{A}B) + (AB)$ | $(A\bar{B}) + (\bar{A}\bar{B})$ |
| 1 | 1 | 1 | $\Sigma m(2, 4)$ | $\Sigma M(1, 3)$ |

Minterms

$$A = 1$$

$$\bar{A} + A \quad \left\{ \begin{array}{l} \text{This is} \\ \text{Minterm form} \end{array} \right.$$

$$A' = 0 \quad \Rightarrow B(\bar{A} + A) \quad \left\{ \begin{array}{l} \text{in notation} \\ \text{form} \end{array} \right.$$

$$B = 1$$

$$\Rightarrow B(1)$$

$$B' = 0$$

$$\Rightarrow B$$

Maxterms

$$A = 0$$

| A | B | $F(A, B)$ |
|---|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

$$(A+B) \cdot (\bar{A}+B)$$

$$A\bar{A} + B\bar{A} + AB + B\cdot B$$

$$\Rightarrow 0 + AB + \bar{A}B + B$$

$$\Rightarrow B(A + \bar{A}) \Rightarrow B(1) = B.$$

| A | B | C | $F(A, B, C)$ | Minterms (SOP) |
|---|---|---|--------------|---|
| 0 | 0 | 0 | 0 | $\bar{A} + \bar{B} + \bar{C}$ |
| 0 | 0 | 1 | 1 | $\bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$ |
| 0 | 1 | 0 | 0 | $(A + \bar{B} + \bar{C})$ |
| 0 | 1 | 1 | 1 | $\bar{A}BC$ |
| 1 | 0 | 0 | 0 | $(\bar{A} + \bar{B} + C)$ |
| 1 | 0 | 1 | 0 | $(\bar{A} + B + \bar{C})$ |
| 1 | 1 | 0 | 1 | $A\bar{B}C$ |
| 1 | 1 | 1 | 1 | ABC |

min terms

$$(\bar{A}\bar{B}C) + \bar{A}BC + A\bar{B}\bar{C} + ABC$$

$$\Rightarrow \bar{A}\bar{B}C + BC(\bar{A}+A) + A\bar{B}\bar{C}.$$

$$\Rightarrow \bar{A}\bar{B}C + BC(1) + ABC$$

$$\Rightarrow BC + \bar{A}\bar{B}C + A\bar{B}\bar{C}$$

Max terms :-

$$(A+B+C)(A+\bar{B}+C)(\bar{A}+B+C)(\bar{A}+\bar{B}+\bar{C})$$

二

$$1. \quad xyz + xy'z + xyz' + x'y'z.$$

| x | y | z |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 1 |

$$2. \quad y'z' + y'z + yz' + xyz.$$

| x | y | z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$$3. \quad y'z' + yz' + y'z + yz + xyz.$$

| x | y | z |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$$4. \quad y'z' + yz' + xyz.$$

| x | y | z |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

DE & CA

1. Write the truth tables for the following expressions.

$$1. \quad xyz + x'y'z + xyz' + x'y'z'$$

| x | y | z | $x'y'z'$ | xyz | $x'yz$ | xyz' | $x'y'z$ | $xyz + x'y'z + xyz' + x'y'z'$ |
|-----|-----|-----|----------|-------|--------|--------|---------|-------------------------------|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1. |

$$2. \quad x'y'z' + x'yz + x'y'z + xyz$$

| x | y | z | $x'y'z'$ | $x'yz$ | $x'y'z$ | xyz | $x'y'z' + x'yz + x'y'z + xyz$ |
|-----|-----|-----|----------|--------|---------|-------|-------------------------------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

$$3 \quad x^1 y^1 z^1 + x^1 y^1 z^1 + x^1 y^1 z + x^1 y^1 z + x y z.$$

$$4. \quad \cancel{x^2} \cdot x^1 y^1 z^1 + x^1 y^1 z^1 + x y^1 z^1$$

Karnaugh Map [k-MAP]

2 Variables.

| | | | |
|-----------|------------------|------------|------------|
| A | B | \bar{B} | B |
| \bar{A} | $\bar{A}\bar{B}$ | $\bar{A}B$ | $A\bar{B}$ |
| A | $A\bar{B}$ | AB | AB |

$2^2 = 4$ cells

2, 1 code

| 2 | 1 | |
|-----------|------------------|-----|
| 0 | 0 | = 0 |
| \bar{A} | $\bar{A}\bar{B}$ | = 1 |
| 0 | 1 | = 2 |
| 1 | 0 | = 3 |
| 1 | 1 | = 4 |

4 Variables . , 8, 4, 2, 1 code

| | | | | |
|------------------|--------------------------------|--------------------------|--------------------|--------------------------|
| AB | $\bar{C}\bar{D}$ | $\bar{C}D$ | CD | $C\bar{D}$ |
| $\bar{A}\bar{B}$ | $\bar{A}\bar{B}\bar{C}\bar{D}$ | $\bar{A}\bar{B}\bar{C}D$ | $\bar{A}\bar{B}CD$ | $\bar{A}\bar{B}C\bar{D}$ |
| $\bar{A}B$ | $\bar{A}B\bar{C}\bar{D}$ | $\bar{A}B\bar{C}D$ | $\bar{A}BCD$ | $\bar{A}B\bar{C}\bar{D}$ |
| AB | $A\bar{B}\bar{C}\bar{D}$ | $A\bar{B}\bar{C}D$ | $ABC\bar{D}$ | $ABC\bar{D}$ |
| $A\bar{B}$ | $A\bar{B}\bar{C}\bar{D}$ | $A\bar{B}\bar{C}D$ | $A\bar{B}CD$ | $A\bar{B}C\bar{D}$ |

| 8 | 4 | 2 | 1 |
|------------|-------------------|--------------------|--------------------------|
| 0 | 0 | 0 | 0 |
| \bar{A} | $\bar{A}\bar{B}$ | $\bar{A}C$ | $\bar{A}D$ |
| 1 | 0 | 0 | 1 |
| $\bar{A}B$ | $\bar{A}B\bar{C}$ | $\bar{A}B\bar{C}D$ | $\bar{A}B\bar{C}\bar{D}$ |
| 2 | 0 | 0 | 0 |
| \bar{A} | \bar{B} | C | D |
| 3 | 0 | 0 | 0 |
| \bar{A} | \bar{B} | \bar{C} | D |
| 4 | 0 | 1 | 0 |
| \bar{A} | B | \bar{C} | D |
| 5 | 0 | 1 | 1 |
| \bar{A} | B | C | 0 |
| 6 | 0 | 1 | 1 |
| \bar{A} | B | C | 1 |
| 7 | 1 | 0 | 0 |
| A | B | C | 0 |
| 8 | 1 | 0 | 0 |
| A | B | C | 0 |
| 9 | 1 | 0 | 1 |
| A | B | C | 0 |
| 10 | 1 | 0 | 1 |
| A | B | C | 1 |
| 11 | 1 | 1 | 0 |
| A | B | C | 0 |
| 12 | 1 | 1 | 0 |
| A | B | C | 0 |
| 13 | 1 | 1 | 1 |
| A | B | C | 1 |
| 14 | 1 | 1 | 1 |
| A | B | C | 1 |

2⁴ = 16 cells.

| | | | | |
|-----------|-------------------------|-------------------|-------------|-------------------|
| BC | $\bar{B}\bar{C}$ | $\bar{B}C$ | BC | $B\bar{C}$ |
| \bar{A} | $\bar{A}\bar{B}\bar{C}$ | $\bar{A}\bar{B}C$ | $\bar{A}BC$ | $\bar{A}B\bar{C}$ |
| AB | $A\bar{B}\bar{C}$ | $A\bar{B}C$ | ABC | $A\bar{B}C$ |

3 variables.

4, 2, 1, code

| | | | | |
|---|---|---|---|-------------------------------------|
| 0 | 0 | 0 | 0 | $\rightarrow \bar{A}\bar{B}\bar{C}$ |
| 1 | 0 | 0 | 1 | $\rightarrow \bar{A}\bar{B}C$ |
| 2 | 0 | 1 | 0 | $\rightarrow \bar{A}B\bar{C}$ |
| 3 | 0 | 1 | 1 | $\rightarrow \bar{A}B\bar{C}$ |
| 4 | 1 | 0 | 0 | $\rightarrow A\bar{B}\bar{C}$ |
| 5 | 1 | 0 | 1 | $\rightarrow A\bar{B}C$ |
| 6 | 1 | 1 | 0 | $\rightarrow AB\bar{C}$ |
| 7 | 1 | 1 | 1 | $\rightarrow ABC$ |

| | | | | |
|---|---|---|---|-------------------------------------|
| A | 0 | 0 | 0 | $\rightarrow \bar{A}\bar{B}\bar{C}$ |
| A | 1 | 0 | 1 | $\rightarrow \bar{A}\bar{B}C$ |
| B | 1 | 0 | 0 | $\rightarrow \bar{A}B\bar{C}$ |
| B | 1 | 1 | 0 | $\rightarrow \bar{A}B\bar{C}$ |
| C | 1 | 1 | 0 | $\rightarrow \bar{A}B\bar{C}$ |
| C | 1 | 1 | 1 | $\rightarrow \bar{A}B\bar{C}$ |
| D | 1 | 1 | 0 | $\rightarrow A\bar{B}\bar{C}$ |
| D | 1 | 1 | 1 | $\rightarrow A\bar{B}C$ |
| E | 1 | 1 | 1 | $\rightarrow AB\bar{C}$ |
| E | 1 | 1 | 1 | $\rightarrow ABC$ |
| F | 1 | 1 | 1 | $\rightarrow ABC$ |
| F | 1 | 1 | 1 | $\rightarrow ABC$ |
| G | 1 | 1 | 1 | $\rightarrow ABC$ |
| G | 1 | 1 | 1 | $\rightarrow ABC$ |
| H | 1 | 1 | 1 | $\rightarrow ABC$ |
| H | 1 | 1 | 1 | $\rightarrow ABC$ |
| I | 1 | 1 | 1 | $\rightarrow ABC$ |
| I | 1 | 1 | 1 | $\rightarrow ABC$ |
| J | 1 | 1 | 1 | $\rightarrow ABC$ |
| J | 1 | 1 | 1 | $\rightarrow ABC$ |

DE & CA

1. Solve the following Expressions?

1. Map for $f(x, y, z) = \sum m(0, 1, 5, 7)$

| | $\bar{y}\bar{z}$ | $\bar{y}z$ | $y\bar{z}$ | yz |
|-----------|------------------|------------|------------|------|
| x | 1 | 1 | | |
| \bar{x} | | | 1 | 1 |
| x | | 1 | 1 | 1 |

$$\bar{x}\bar{y} + \bar{y}z + xz.$$

2. $f(w, x, y, z) = \sum m(1, 2, 3, 5, 6, 7, 8, 13)$

| | $\bar{y}\bar{z}$ | $\bar{y}z$ | $y\bar{z}$ | yz |
|------------|------------------|------------|------------|------|
| wx | 1 | 1 | | |
| $\bar{w}x$ | | | 1 | 1 |
| $\bar{w}x$ | | 1 | 1 | 1 |
| wx | 1 | 1 | 1 | 1 |
| $w\bar{x}$ | 1 | | | |

$$\Rightarrow \bar{w}\bar{x}\bar{z} + \bar{w}\bar{x}y + \bar{w}\bar{x}y + \bar{w}\bar{x}y + \bar{w}yz + \bar{w}y\bar{z} + \bar{w}xz + x\bar{y}z + w\bar{x}y\bar{z}$$

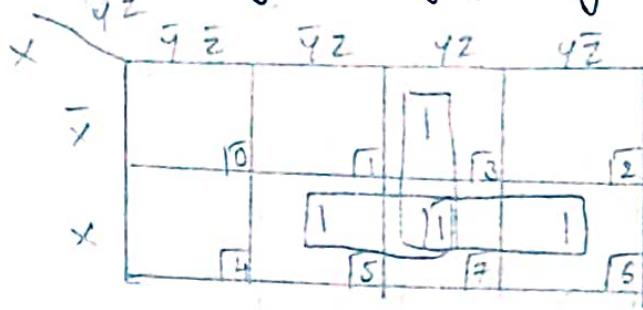
$$\Rightarrow \bar{w}z(\bar{y} + y) + \bar{w}z(x + \bar{x}) + \bar{w}y(\bar{x} + x) + \bar{w}y\bar{z} + x\bar{y}z + w\bar{x}\bar{y}\bar{z}$$

$$\Rightarrow \bar{w}x + \bar{w}y + \bar{w}zy\bar{z} + x\bar{y}z + w\bar{x}\bar{y}z.$$

$$\Rightarrow \bar{w}(x + y + y\bar{z}) + x\bar{y}z + w\bar{x}\bar{y}\bar{z}$$

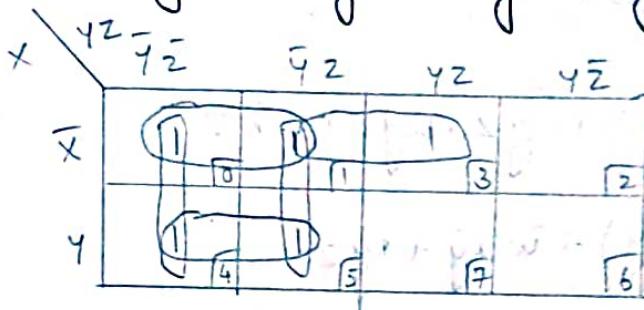
$$\Rightarrow w(y + x + y + z) + x\bar{y}\bar{z} + w\bar{x}\bar{y}z.$$

$$3. F = xy\bar{z} + \bar{x}\bar{y}z + \bar{x}yz' + x'y\bar{z}'$$



$$xz + xy + yz$$

$$4. F = x'y'z' + xy'z' + x'y'z + xy'z + xyz$$

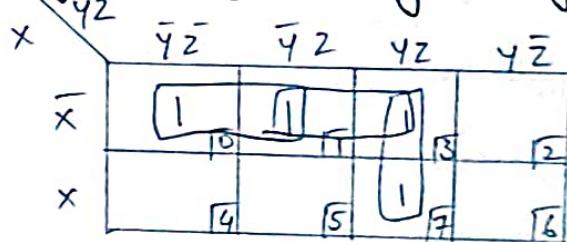


$$\bar{y}\bar{z} + \bar{y}z + \bar{x}\bar{y} + xy + \bar{x}z$$

$$\bar{y}(\bar{z} + z + \bar{x} + x) + \bar{x}z$$

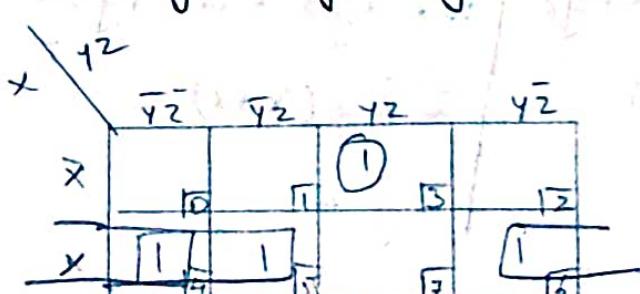
$$\bar{y} + \bar{x}z.$$

$$6. xyz + x'y'z + x'y'z + x'y'z'$$



$$\Rightarrow \bar{x}\bar{y} + \bar{x}z + yz$$

$$7. x'y'z' + xy'z + x'y'z + xyz'$$



$$\Rightarrow \bar{x}\bar{y} + x\bar{z} + xyz$$

$$8. wxyz + w'xy'z + wx'y'z + wx'y'z + wxyz$$

$$+ w'xy'z$$

| $\bar{w}\bar{x}$ | $\bar{y}\bar{z}$ | $\bar{y}z$ | $y\bar{z}$ | yz |
|------------------|------------------|------------|------------|------|
| $\bar{w}x$ | 10 | 11 | 13 | 12 |
| $w\bar{x}$ | 1 | 4 | 5 | 6 |
| wx | 12 | 14 | 15 | 16 |
| $w\bar{x}$ | 18 | 19 | 11 | 10 |

$$\bar{w}x\bar{y} + x\bar{y}z + w\bar{x}z + w\bar{y}z + w\bar{y}z + w\bar{x}z$$

$$wz(x + \bar{x} + \bar{y} + y) + \bar{w}x\bar{y} + x\bar{y}z$$

$$wz + \bar{w}x\bar{y} + x\bar{y}z$$

$$wz + x\bar{y}(\bar{w} + x)$$

$$9. w'xy'z + w'xyz' + w'x'y'z + w'x'y'z + wxyz + wxy'z + wxyz$$

| $\bar{w}\bar{x}$ | $\bar{y}\bar{z}$ | $\bar{y}z$ | $y\bar{z}$ | yz |
|------------------|------------------|------------|------------|------|
| $\bar{w}x$ | 10 | 11 | 13 | 12 |
| $w\bar{x}$ | 15 | 1 | 17 | 16 |
| wx | 1 | 15 | 13 | 14 |
| $w\bar{x}$ | 1 | 1 | 11 | 10 |

$$\bar{w}\bar{x} + \bar{y}z + \bar{w}\bar{x} + yz$$

$$\Rightarrow \bar{w}\bar{x}z(\bar{y} + y)$$

$$\Rightarrow \bar{w}\bar{x}z$$

$$\bar{w}\bar{x} + \bar{y}z + \bar{w}x + \bar{y}z$$

$$\bar{w}\bar{y}z(\bar{x} + x)$$

$$\bar{w}\bar{y}z$$

$$\Rightarrow \bar{w}\bar{x}z + \bar{w}\bar{y}z + wxy\bar{z} + \bar{w}xy\bar{z} + w\bar{x}y\bar{z}$$

$$10. \quad x'y'z + x'y'z + x'y'z + x'y'z.$$

~~x~~ $\bar{y}z$ $y\bar{z}$ $y\bar{z}$ $y\bar{z}$

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |

$$\Rightarrow \bar{x}\bar{y} + \bar{x}z + \bar{y}z.$$

$$11. \quad \bar{x}\bar{y}'z' + x\bar{y}'z + x'y'z + xy'z.$$

~~x~~ $\bar{y}z'$ $\bar{y}z$ $y\bar{z}$ $y\bar{z}$

| | | | | |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |

$$x\bar{y} + \bar{y}z + xy\bar{z}$$

$$\Rightarrow \bar{y}(x+z) + xy\bar{z}$$

$$12. \quad w'xy'z + w'xy'z + w'x'y'z + w'x'y'z + wxy'z + wxy'z.$$

~~wx~~ $\bar{y}z$ $\bar{y}z$ $y\bar{z}$ $y\bar{z}$

| | | | | |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |

$$\bar{w}x\bar{y} + \bar{w}\bar{y}z + x\bar{y}z + w\bar{x}yz$$

$$\bar{w}\bar{y}(x+z) + z(x\bar{y} + w\bar{x}y).$$

$$13. w'x'y'z + w'x'y'z' + w'x'y'z + w'xy'z + w'xy'z + w'xy'z \\ + w'x'y'z + w'xy'z.$$

| $w'x'y'z$ | $\bar{y}z$ | $\bar{y}z$ | $y\bar{z}$ | $y\bar{z}$ |
|------------------|------------|------------|------------|------------|
| $\bar{w}\bar{x}$ | ① | II | I | III |
| $\bar{w}x$ | IV | ① | V | VI |
| wx | ① | VI | VII | VIII |
| $w\bar{x}$ | VIII | IX | X | XI |

$$\Rightarrow \bar{x}yz + w\bar{x}\bar{y}\bar{z} + \bar{w}x\bar{y}z + w\bar{x}\bar{y}\bar{z}.$$

$$5. f = xy' + wxz + w'x'yz.$$

$$\Rightarrow w'x'y'z + w'xy'z' + wxy'z + wxyz + w'xyz$$

| $w'x'y'z$ | $\bar{y}z$ | $\bar{y}z$ | $y\bar{z}$ | $y\bar{z}$ |
|------------------|------------|------------|------------|------------|
| $\bar{w}\bar{x}$ | II | III | IV | V |
| $\bar{w}x$ | VI | ① | V | VI |
| wx | ① | VI | VII | VIII |
| $w\bar{x}$ | VIII | IX | X | XI |

$$\Rightarrow w\bar{x}\bar{y} + wxz + xy'z + wxyz.$$

9/20 Arithmetic Circuits

The logical circuits which is designed for calculations of arithmetic operations like addition, subtraction, multiplication and division

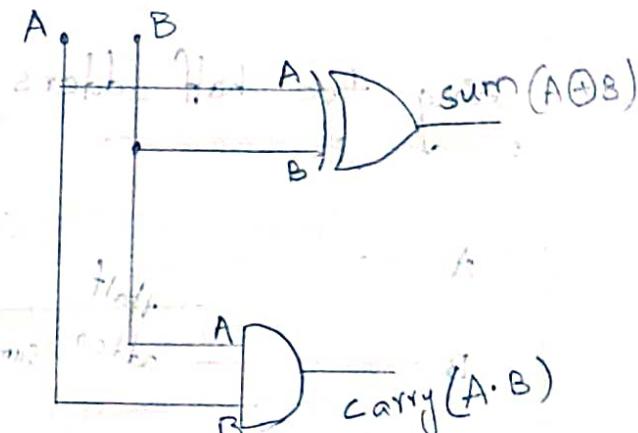
- * It has been used for Arithmetic logic unit.

Half adder

| sum carry. | | | |
|------------|---|---|---|
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

$$\text{Sum} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry} = AB.$$



Full adder

| Input | | | output | |
|-------|---|---|--------|--------|
| A | B | C | sum | carry. |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Sum :-

$$\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$\Rightarrow \bar{A}\bar{B}C + ABC + \bar{C}(\bar{A}B + AB)$$

$$\Rightarrow \bar{A}\bar{B}C + ABC + \bar{C}(A \oplus B)$$

$$\Rightarrow C(\bar{A}\bar{B} + AB) + \bar{C}(A \oplus B)$$

$$\Rightarrow C(\overline{A \oplus B}) + \bar{C}(A \oplus B)$$

$$\Rightarrow C \oplus B \oplus A$$

$$\Rightarrow A \oplus B \oplus C.$$

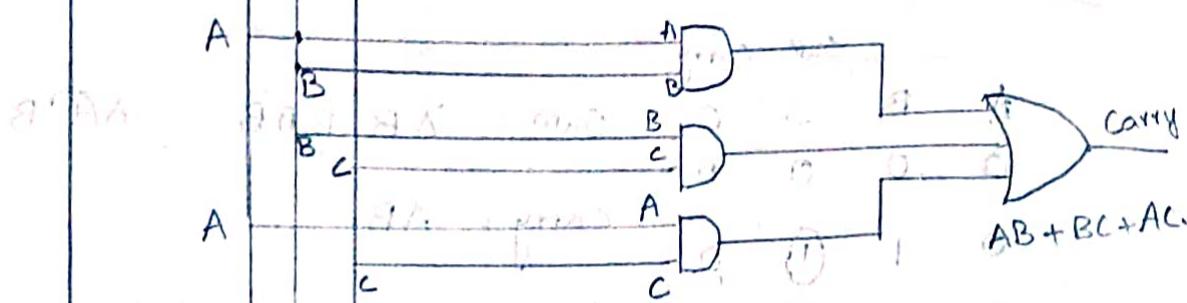
$$\text{Carry} := \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC + ABC + ABC$$

$$\Rightarrow BC(\bar{A}+A) + AC(\bar{B}+B) + ABC(\bar{C}+C)$$

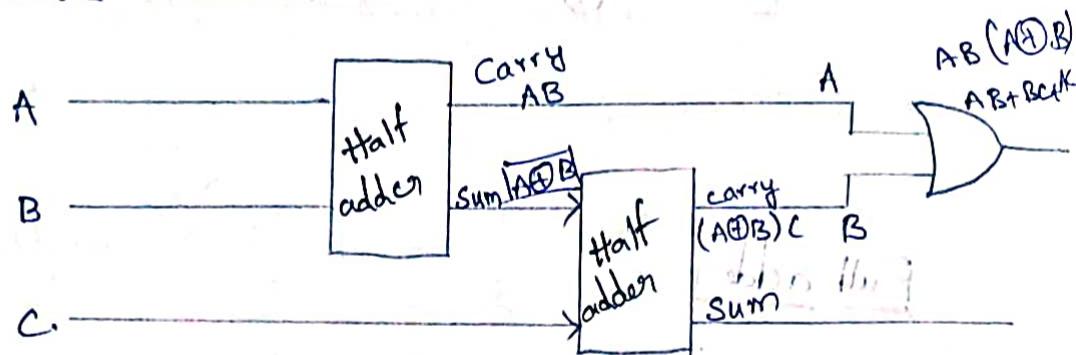
$$\Rightarrow BC + AC + AB.$$



Robert's Method



Using two half adders and OR gate.



$$(A \oplus B) \oplus C = A \oplus B \oplus C$$

Half adder

$$\text{sum} = A \oplus B, \quad AB + C(\bar{A}B) + (\bar{B}A)$$

$$\text{carry} = AB, \quad AB + \bar{A}BC + A\bar{B}C$$

$$(A \oplus B) \oplus C = (A \oplus B)C + \bar{C}(A \oplus B) + \bar{A}BC + A\bar{B}C$$

$$(A \oplus B) \oplus C = (\bar{A}B + A\bar{B})C + \bar{C}(A + \bar{B}) + \bar{A}BC + A\bar{B}C$$

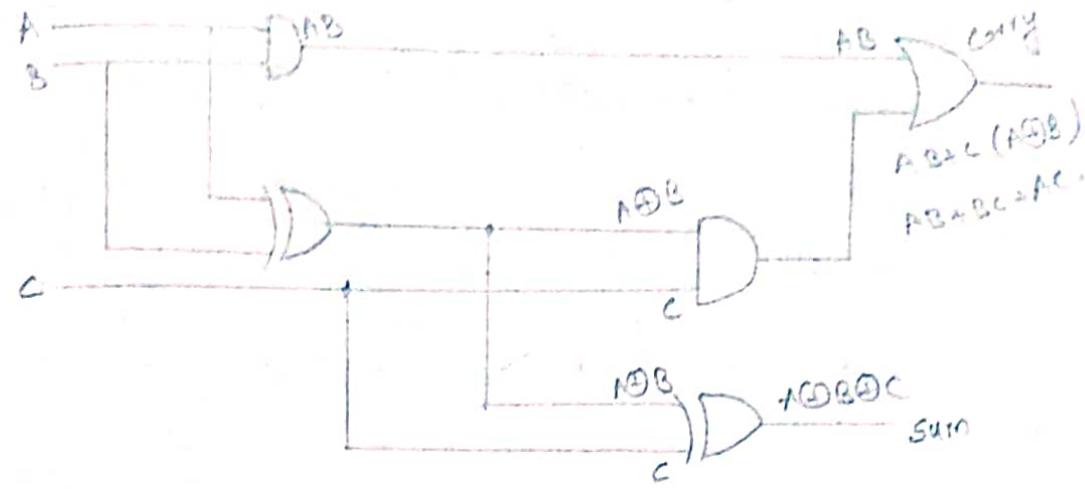
$$ABC + ABC + ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$$

$$ABC + ABC + ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$$

$$AB + AC + BC$$

$$\Rightarrow AB + BC + AC$$

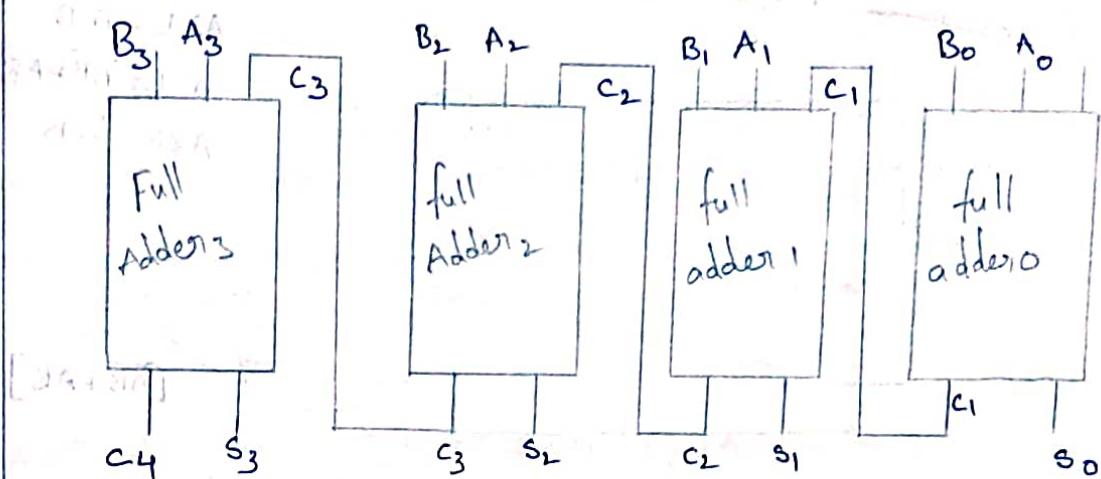
| | | | | |
|-----|---|---|---|---|
| A | 0 | 1 | 1 | 0 |
| B | 0 | 0 | 1 | 1 |
| C | 0 | 1 | 0 | 0 |
| Sum | 0 | 1 | 1 | 0 |



Parallel adder
(Combinational)

$$A = 11 \rightarrow \begin{matrix} A_3 & A_2 & A_1 & A_0 \\ 1 & 0 & 1 & 1 \end{matrix}$$

$$B = 13 \rightarrow \begin{matrix} B_3 & B_2 & B_1 & B_0 \\ 1 & 1 & 0 & 1 \end{matrix}$$



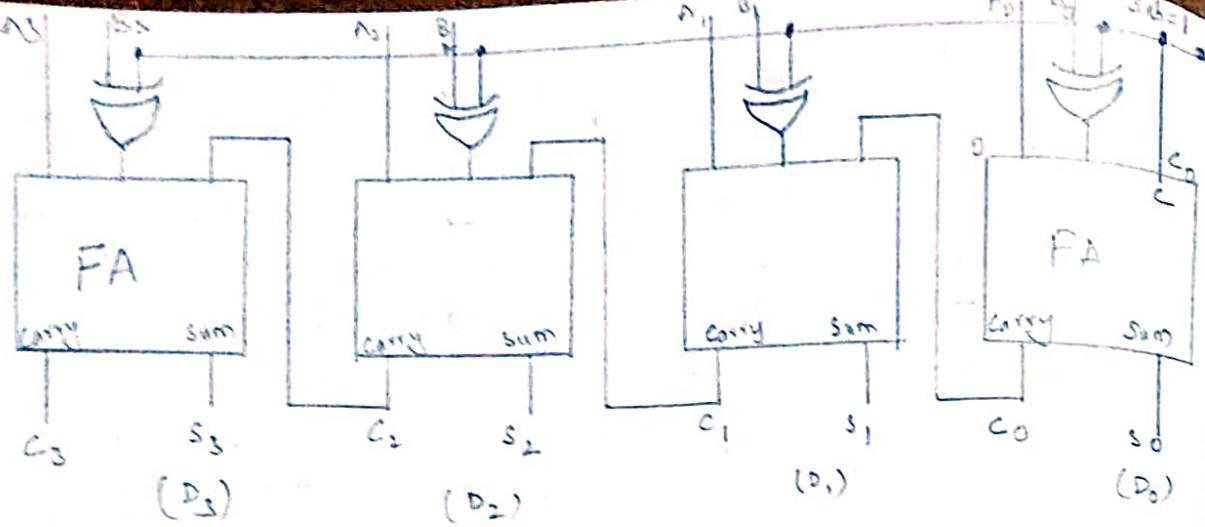
Result :- $C_4 \ S_3 \ S_2 \ S_1 \ S_0 \rightarrow \text{Add}$

$S_3, S_2, S_1, S_0 \rightarrow \text{sub}$

2's Complement Adder Subtractor :-

1bit comparator

| Input | | Output | | |
|-------|---|---------|---------|---------|
| A | B | $A > B$ | $A = B$ | $A < B$ |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |



Addition sub=0

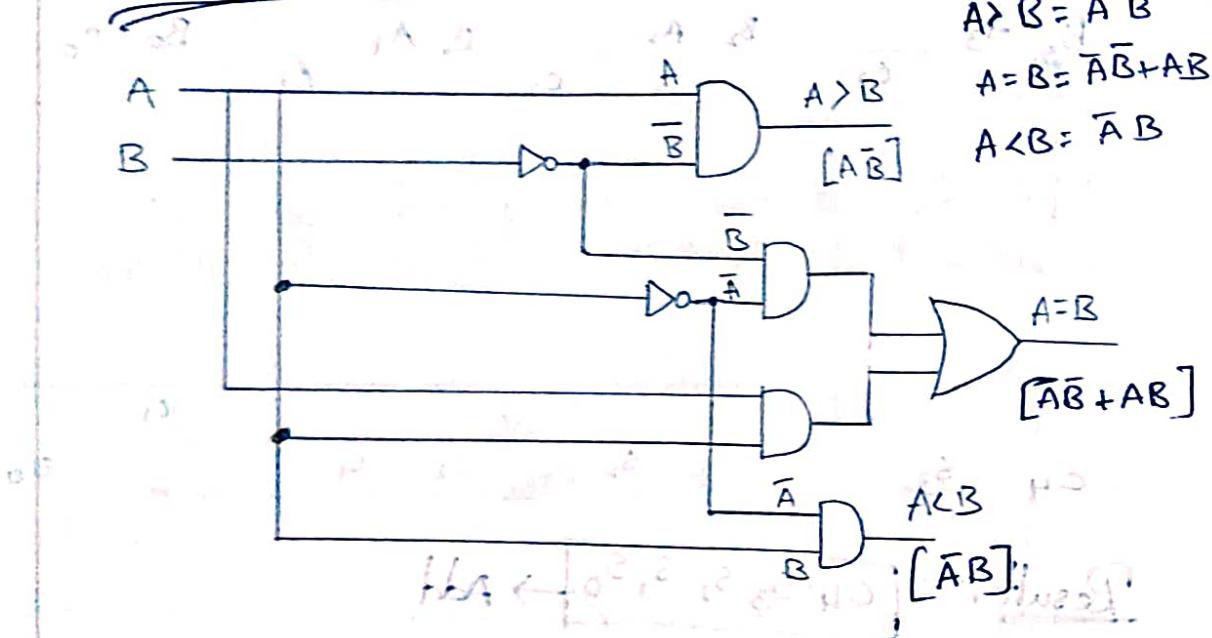
Subtraction sub=1

Result :-

Addition: C₃S₃S₂S₁0

Subtraction: D₃D₂D₁D₀

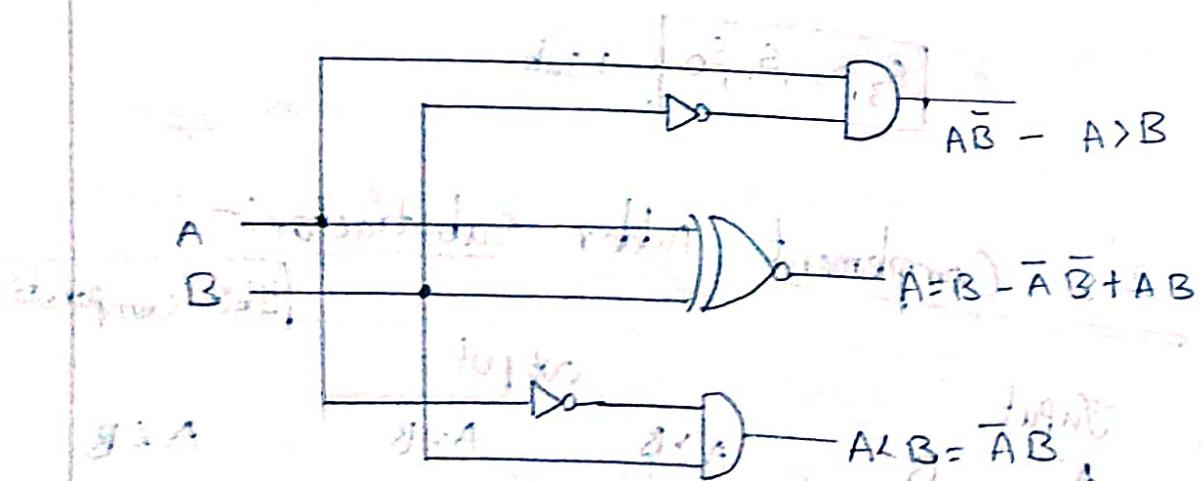
2's complement ADDer Substractor (Diagrams)



$$A > B = A \bar{B}$$

$$A = B = \bar{A} \bar{B} + A B$$

$$A < B = \bar{A} B$$



1 BIT COMPARATOR IC.

4 BIT COMPARATOR (IC 7485)

| Comparing Input | | cascading Input | | output | |
|-----------------|-------------|-----------------------|---------|---------|---------|
| $A_3 B_3$ | $A_2 B_2$ | $A_1 B_1 A_0 B_0$ | $A > B$ | $A = B$ | $A < B$ |
| $A_3 > B_3$ | X | X X X X X | 1 | 0 | 0 |
| $A_3 < B_3$ | X | X X X X X | 0 | 0 | 1 |
| $A_3 = B_3$ | $A_2 > B_2$ | X X X X X | 1 | 0 | 0 |
| $A_3 = B_3$ | $A_2 < B_2$ | X X X X X | 0 | 0 | 1 |
| $A_3 = B_3$ | $A_2 < B_2$ | $A_1 > B_1$ | X X X X | 1 | 0 0 |
| $A_3 = B_3$ | $A_2 < B_2$ | $A_1 > B_1$ | X X X X | 0 | 0 1 |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1 A_0 > B_0$ | X X X | 1 | 0 0 |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1 A_0 < B_0$ | X X X | 0 | 0 1 |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1 A_0 = B_0$ | 1 0 0 | 1 0 | 0 |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1 A_0 = B_0$ | 0 0 1 | 0 0 | 1 |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1 A_0 = B_0$ | 0 1 0 | 0 | 1 0 |

$$A > B \Rightarrow A_3 \bar{B}_3 + (A_3 \oplus B_3) A_2 \bar{B}_2 + (A_3 \oplus B_3) (A_2 \oplus B_2) A_1 \bar{B}_1 +$$

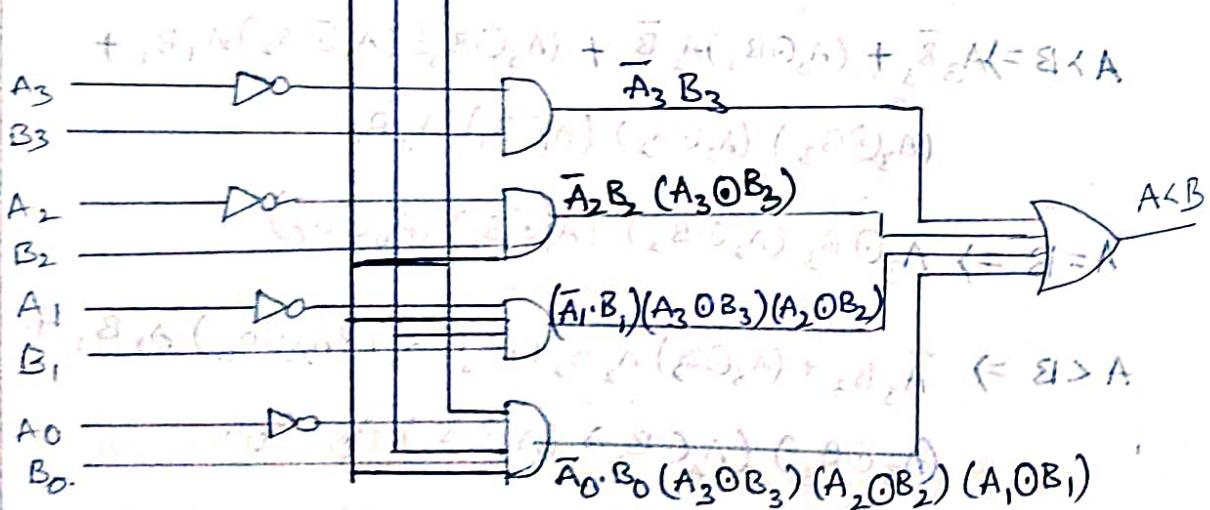
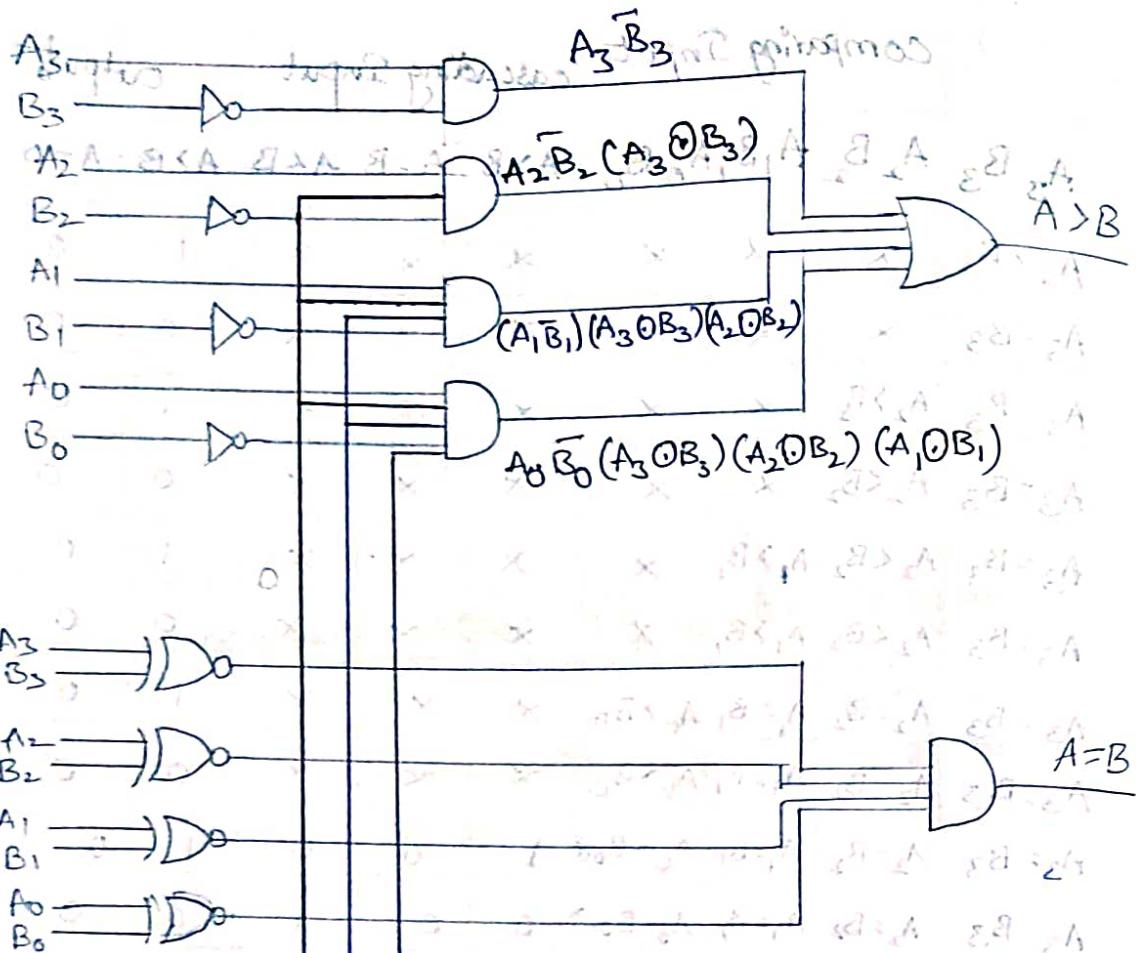
$$(A_3 \oplus B_3) (A_2 \oplus B_2) (A_1 \oplus B_1) A_0 \bar{B}_0$$

$$A = B \Rightarrow A_3 \oplus B_3 (A_2 \oplus B_2) (A_1 \oplus B_1) (A_0 \oplus B_0)$$

$$A < B \Rightarrow \bar{A}_3 B_3 + (A_3 \oplus B_3) \bar{A}_2 B_2 + (A_3 \oplus B_3) (A_2 \oplus B_2) \bar{A}_1 B_1 +$$

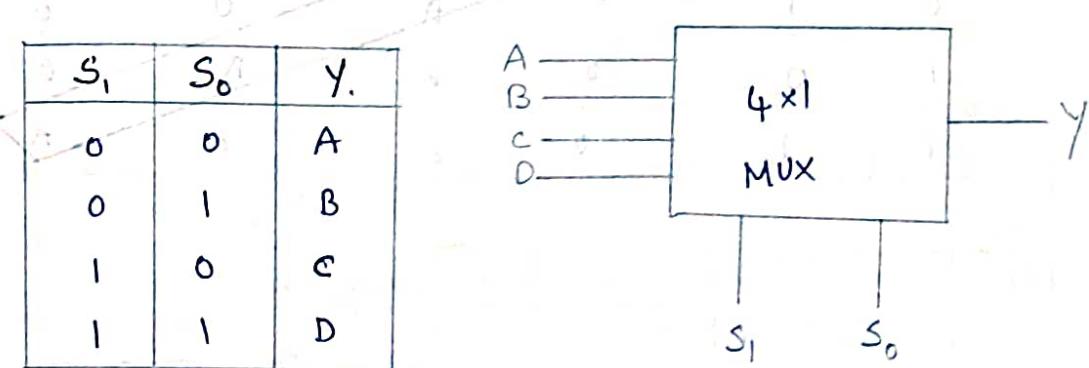
$$(A_3 \oplus B_3) (A_2 \oplus B_2) (A_1 \oplus B_1) \bar{A}_0 \cdot B_0.$$

(COMPARATOR) BIT +

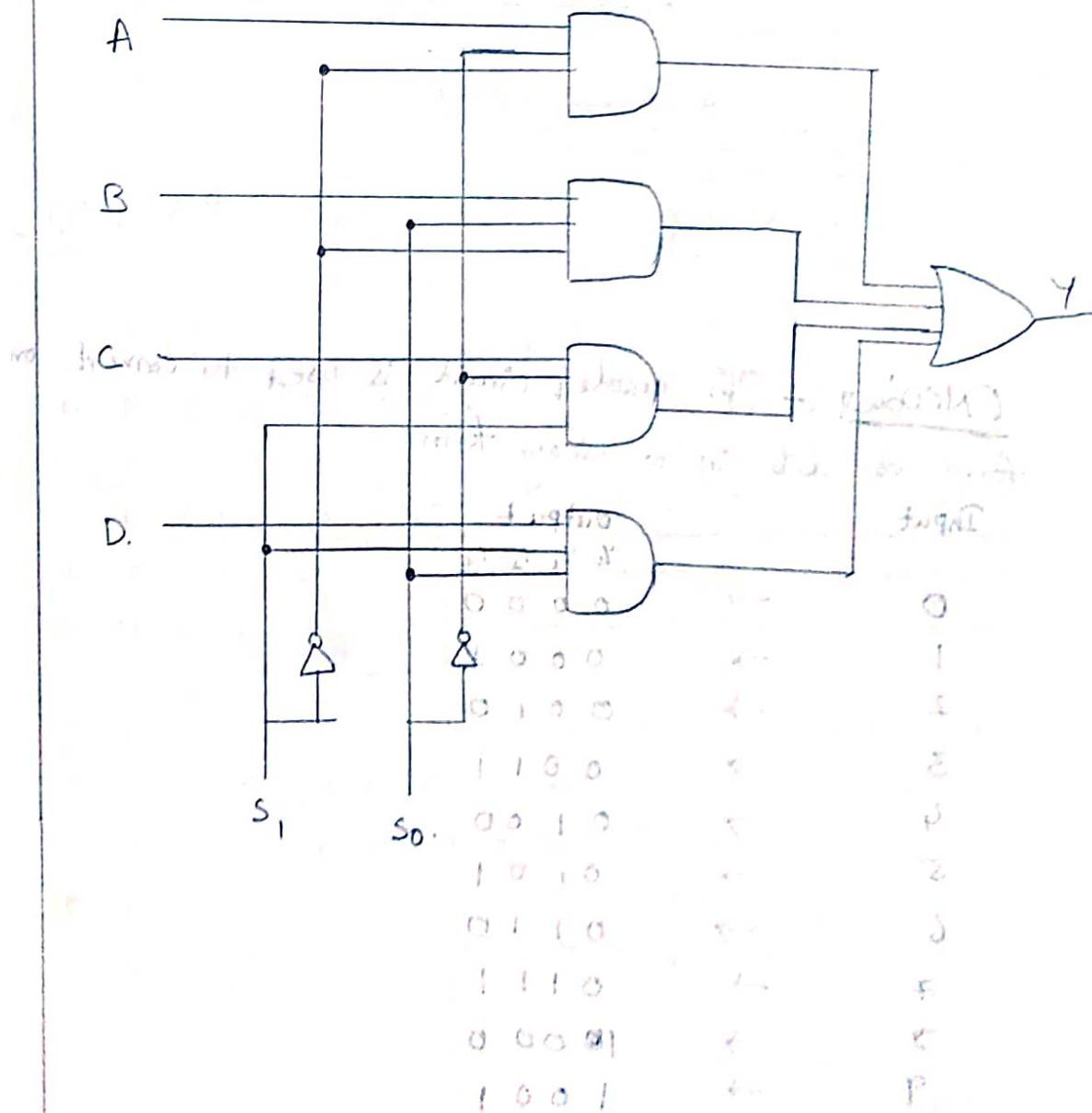


4. COMBINATIONAL CIRCUITS

* Multiplexer [MUX] :- A digital circuit that sends data from anyone of many lines into a single line.

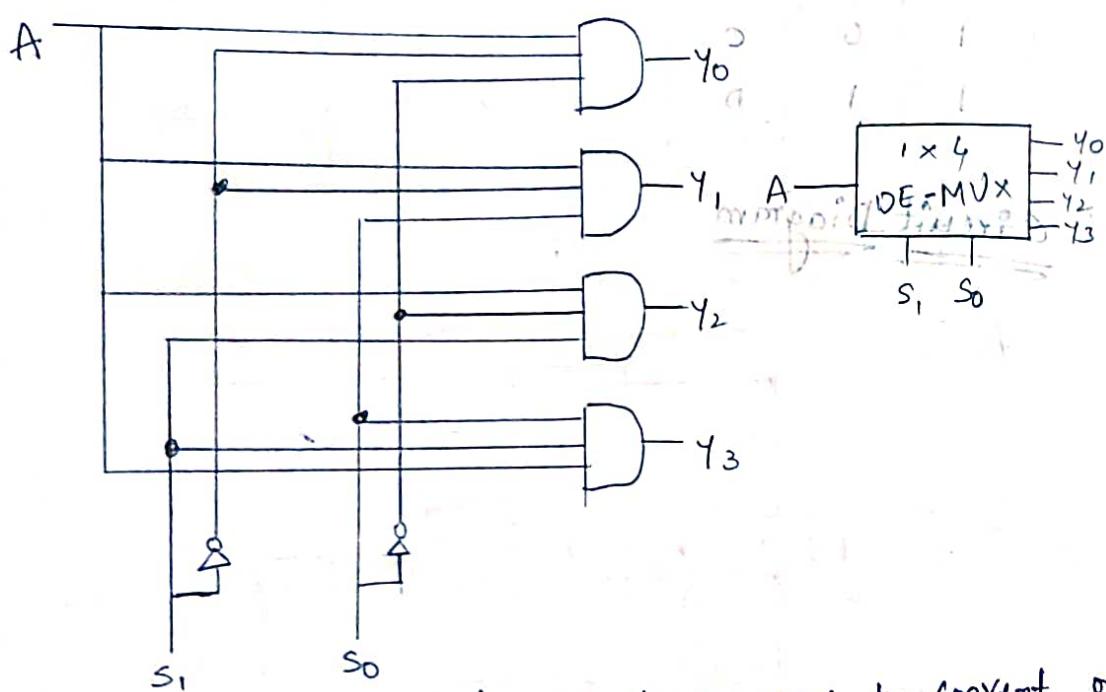


Circuit Diagram



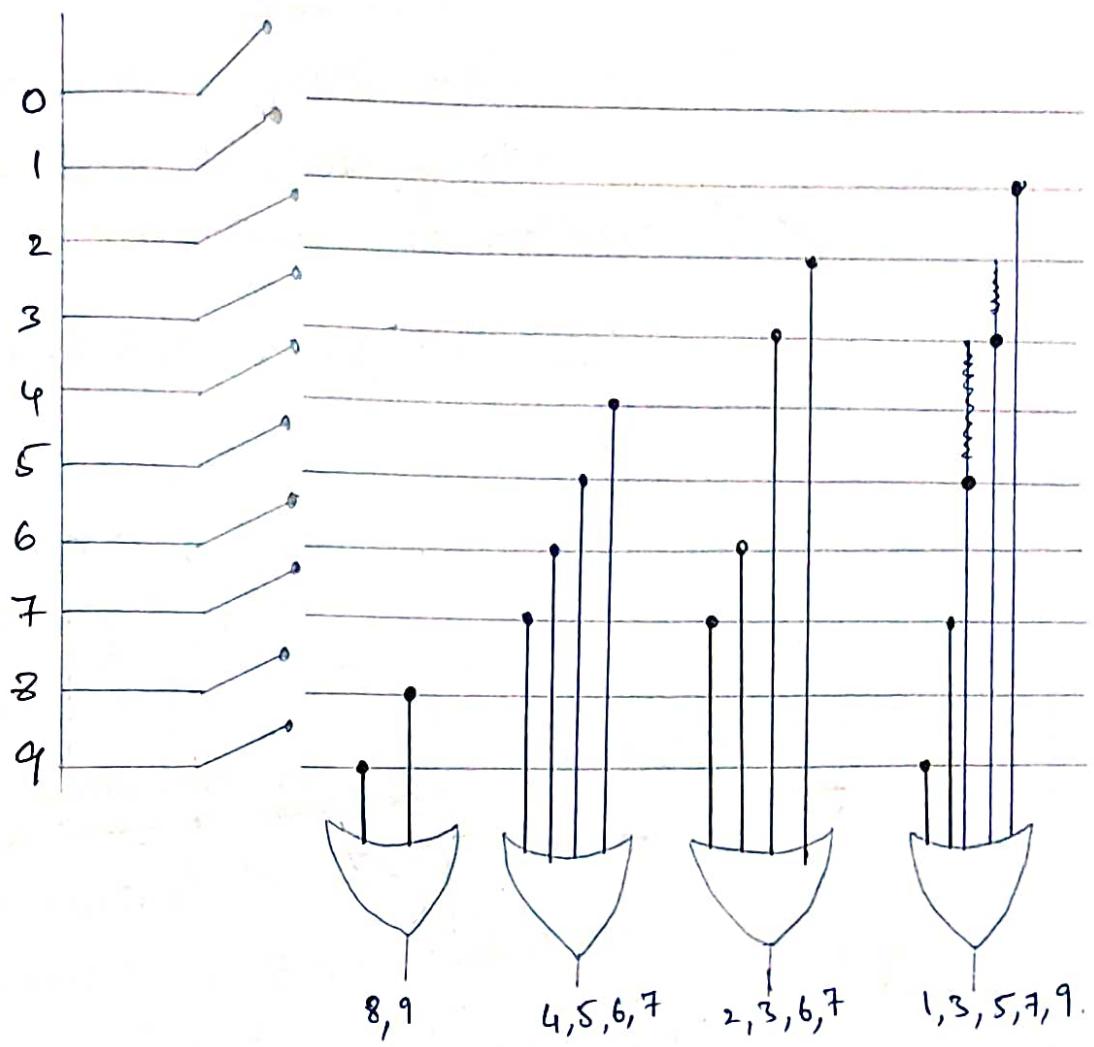
DEMULTIPLEXER :- [DE-MUX] = go this data from one line can be sent on to any one of many lines.

| Input | | Output | | | |
|-------|-------|--------|-------|-------|-------|
| s_1 | s_0 | y_0 | y_1 | y_2 | y_3 |
| 0 | 0 | A | 0 | 0 | 0 |
| 0 | 1 | 0 | A | 0 | 0 |
| 1 | 0 | 0 | 0 | A | 0 |
| 1 | 1 | 0 | 0 | 0 | A |

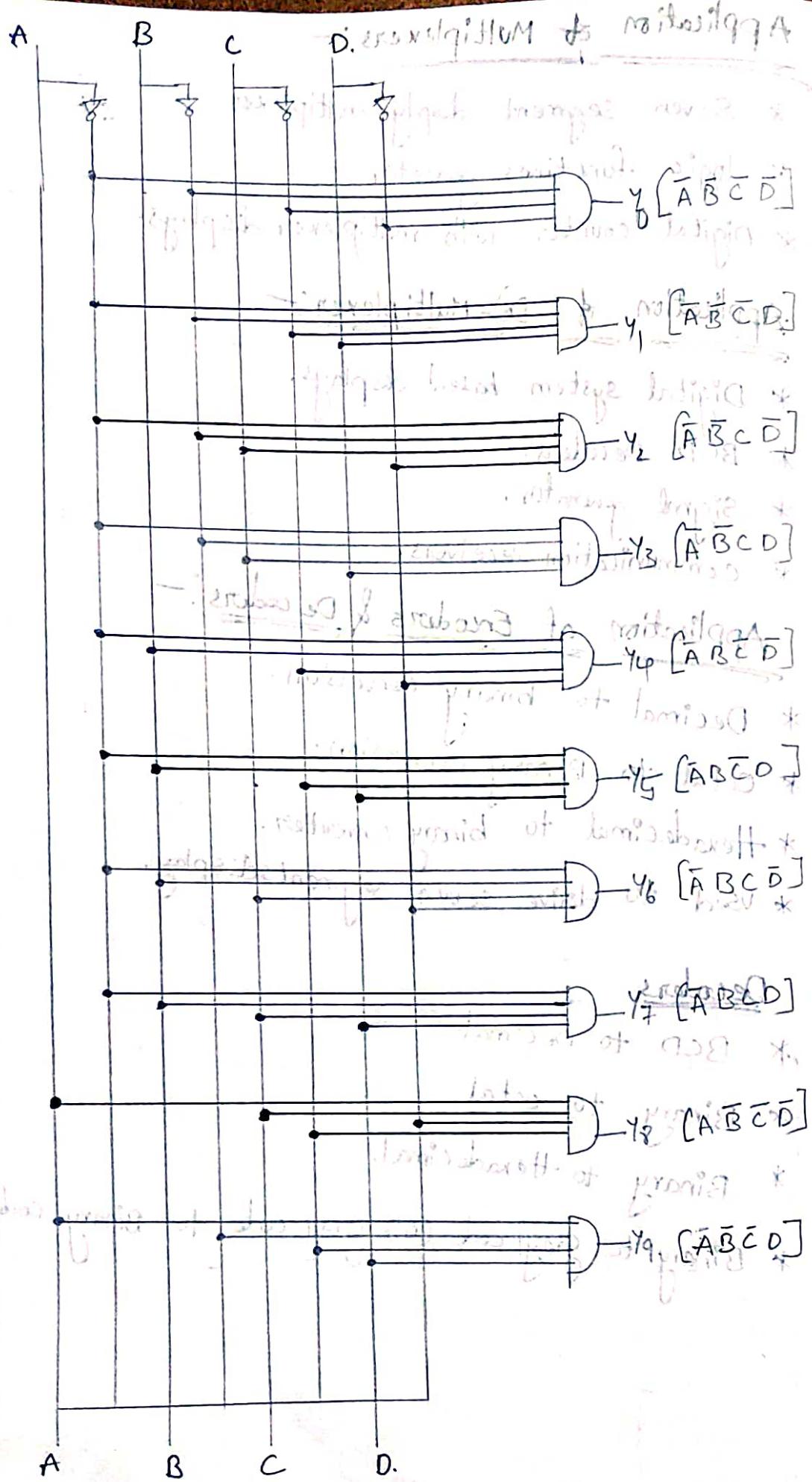


Encoder :- The encoder circuit is used to convert one form of data in to binary form.

| Input | Output |
|-------|-------------------------|
| | $y_0 \ y_1 \ y_2 \ y_3$ |
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 0 1 1 |
| 4 | 0 1 0 0 |
| 5 | 0 1 0 1 |
| 6 | 0 1 1 0 |
| 7 | 0 1 1 1 |
| 8 | 1 0 0 0 |
| 9 | 1 0 0 1 |



DECODER:- This circuit converts binary data to other form of data.



Application of Multiplexers:-

- * Seven segment display multiplexer
- * logic functions generator.
- * Digital counter with multiplexer displays.

Application of De-Multiplexer:-

- * Digital system based displays.
- * BCD Decoders.
- * Signal generator.
- * communication receivers.

Application of Encoders & Decoders:-

- * Decimal to binary conversion.
- * Octal to Binary conversion.
- * Hexadecimal to binary converter.
- * Used to drive seven segments display.

Decoders

- * BCD to Decimal.
- * Binary to octal
- * Binary to Hexadecimal.
- * Binary to gray code (or) gray code to Binary code

2. LOGIC FAMILIES & FLIP-FLOPS

R_S LATCH USING NAND GATE:-

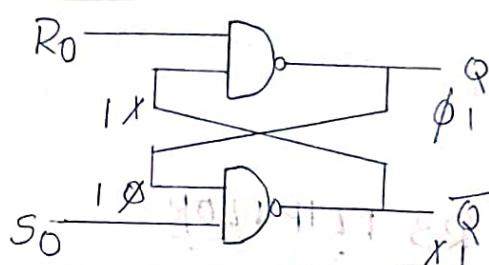
$$Q = 0, \bar{Q} = 1$$

| R | S | Q | \bar{Q} | comment |
|---|---|---|-----------|-------------|
| 0 | 0 | * | * | Forbidden |
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | 0 | 1 | No changes. |

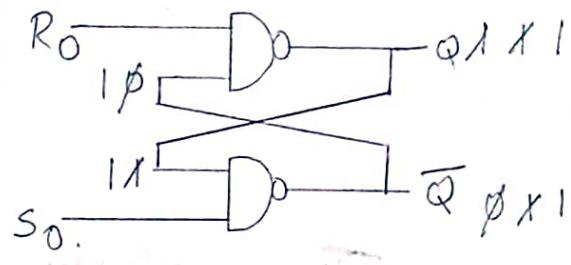
$$Q = 1, \bar{Q} = 0$$

| R | S | Q | \bar{Q} | comment |
|---|---|---|-----------|-----------|
| 0 | 0 | * | * | Forbidden |
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | 1 | 0 | No change |

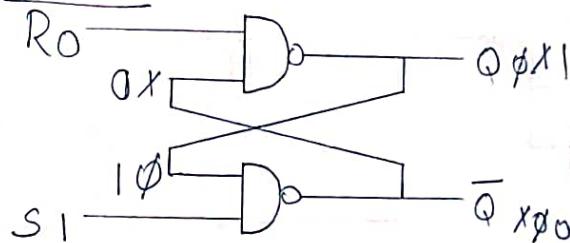
Case - 1 → Forbidden



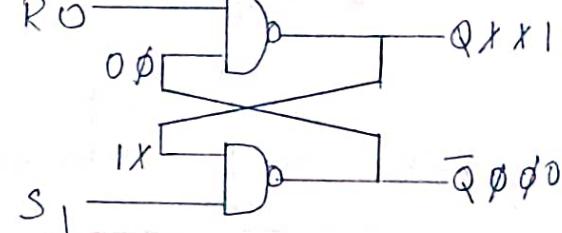
Case - 1 → Forbidden.



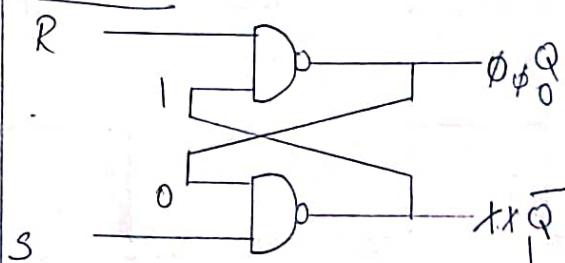
Case - 2 → SET



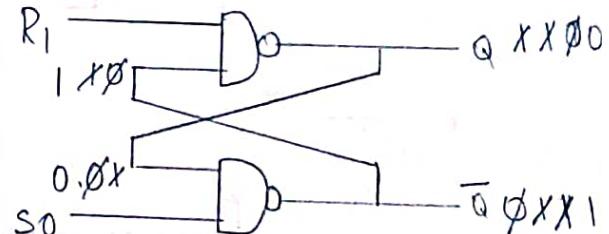
Case - 2 → SET



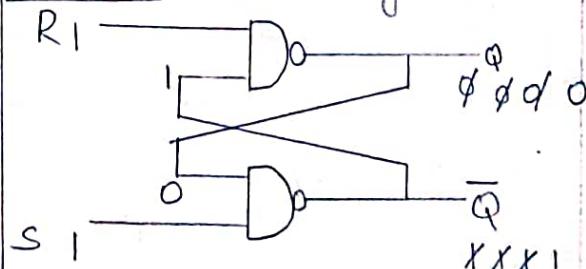
Case - 3 → RESET



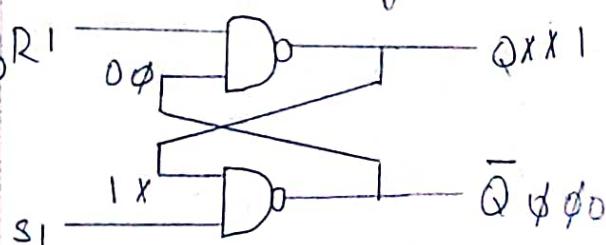
Case - 3 → RESET



Case - 4 - No change

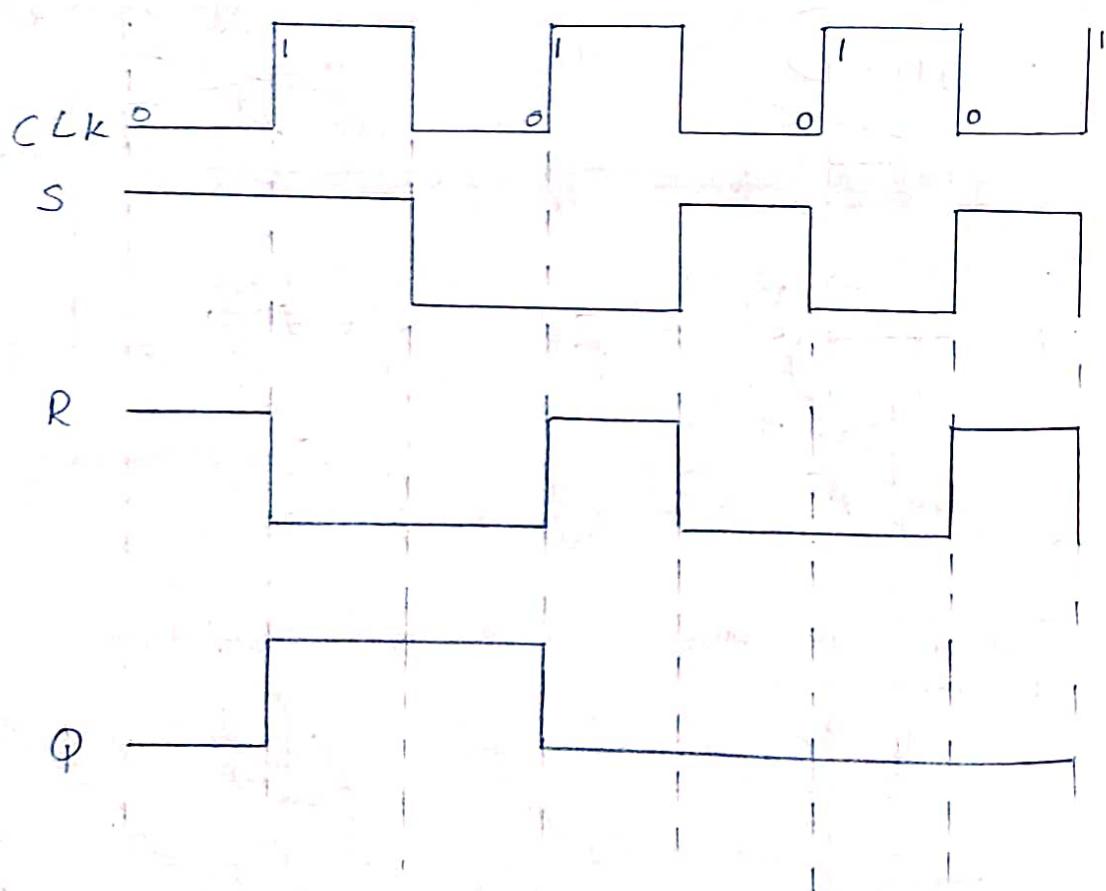


Case - 4 - No change



2907-517 8 231316 FAMILE 8 10410 8

Timing Diagram of RS FLIP FLOP



R-S LATCH USING NOR GATE:-

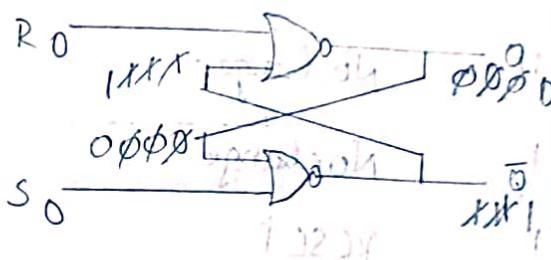
$$Q = 0, \bar{Q} = 1$$

| R | S | Q | \bar{Q} | Comment |
|---|---|---|-----------|-----------|
| 0 | 0 | 1 | 0 | Nochange |
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | * | * | Forbidden |

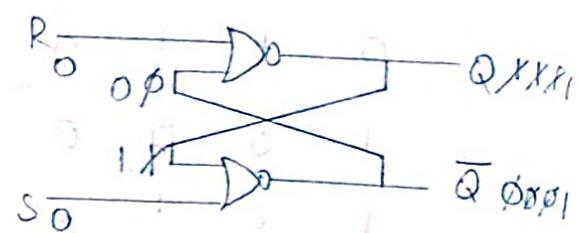
$$\bar{Q} = 0, Q = 1$$

| R | S | Q | \bar{Q} | comment |
|---|---|---|-----------|-----------|
| 0 | 0 | 1 | 0 | Nochange |
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | * | * | Forbidden |

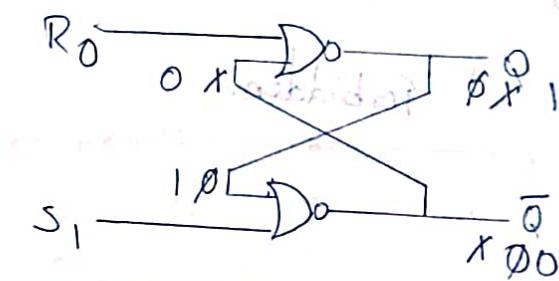
Case - 1 Nochange



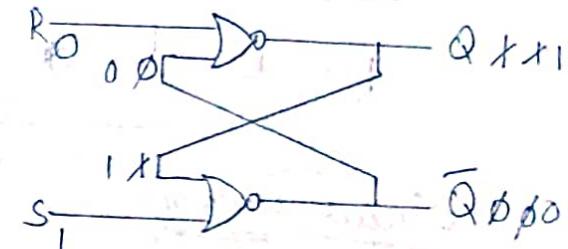
case-1 Nochange



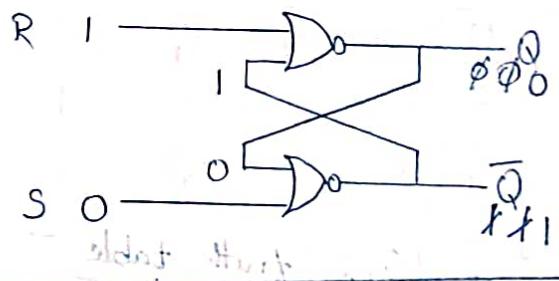
case - 2 SET



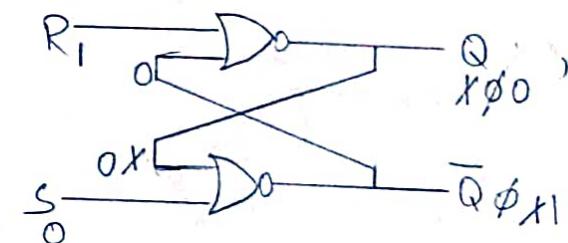
case - 2 SET



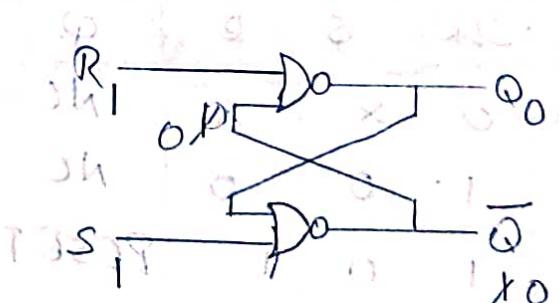
case - 3 RESET



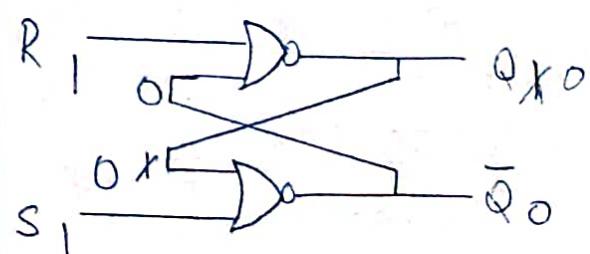
case - 3 RESET



case - 4 Forbidden



case - 4 Forbidden

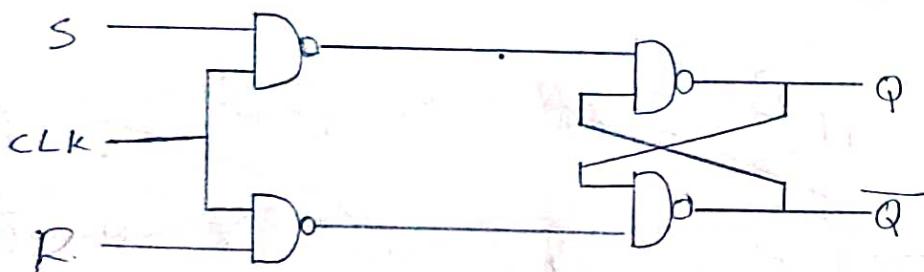


CLOCKED RS FLIP FLOP :-

$$1 = \bar{Q}, 0 = Q$$

| CLK | S | R | Q | \bar{Q} | Comment |
|-----|---|---|---|-----------|------------|
| 0 | 0 | 0 | 0 | 1 | No change |
| 0 | 0 | 1 | 0 | 1 | No change |
| 0 | 1 | 0 | 0 | 1 | No change |
| 0 | 1 | 1 | 0 | 1 | No change |
| 1 | 0 | 0 | 0 | 1 | No change |
| 1 | 0 | 1 | 0 | 1 | RESET |
| 1 | 1 | 0 | 1 | 0 | SET |
| 1 | 1 | 1 | * | * | Forbidden. |

Circuit Diagram



Logical Diagram

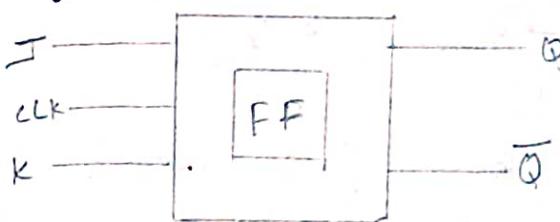


Simplified truth table :-

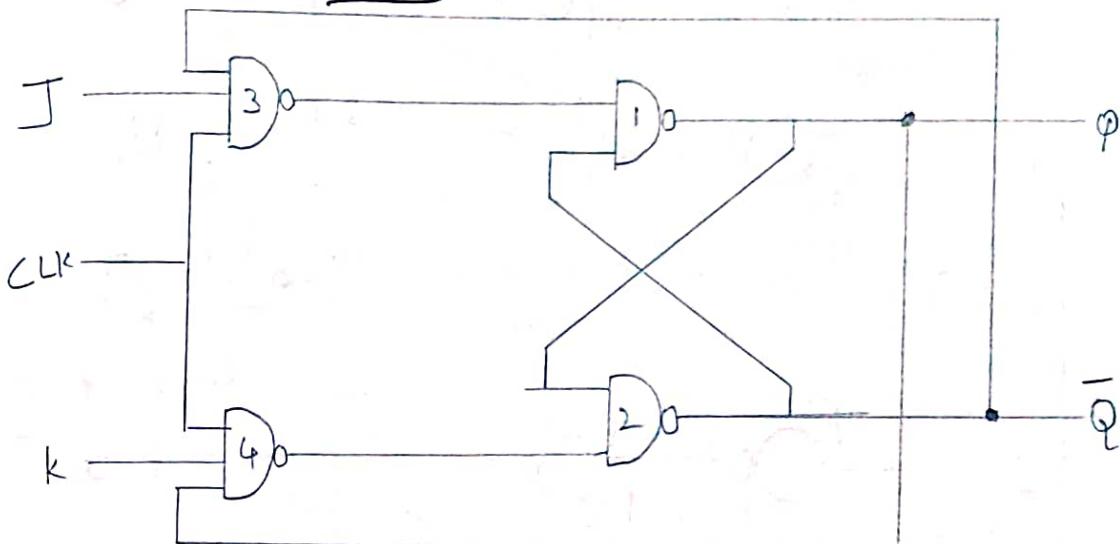
| CLK | S | R | Q |
|-----|---|---|-------|
| 0 | x | x | NC |
| 1 | 0 | 0 | NC |
| 1 | 0 | 1 | RESET |
| 1 | 1 | 0 | SET. |
| 1 | 1 | 1 | * |

J K FLIP FLOP

Logic symbol



Circuit Diagram

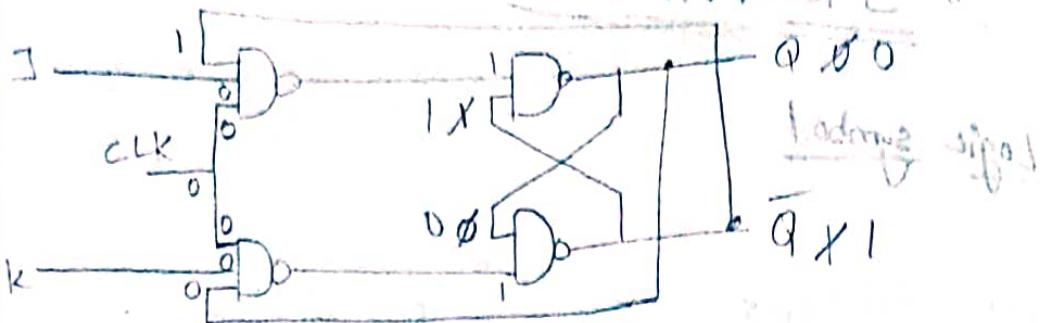


| CLK | J | K | Q | \bar{Q} | COMMENT |
|-----|---|---|-----------|-----------------|-----------|
| 0 | 0 | 0 | 0 | 1 | No change |
| 0 | 0 | 1 | 0 | 1 | No change |
| 0 | 1 | 0 | 0 | 1 | No change |
| 0 | 1 | 1 | 0 | 1 | No change |
| 1 | 0 | 0 | 0 | 1 | No change |
| 1 | 0 | 1 | 0 | 1 | RESET |
| 1 | 1 | 0 | 1 | 0 | SET |
| 1 | 1 | 1 | Q_{n+1} | \bar{Q}_{n+1} | Toggling. |

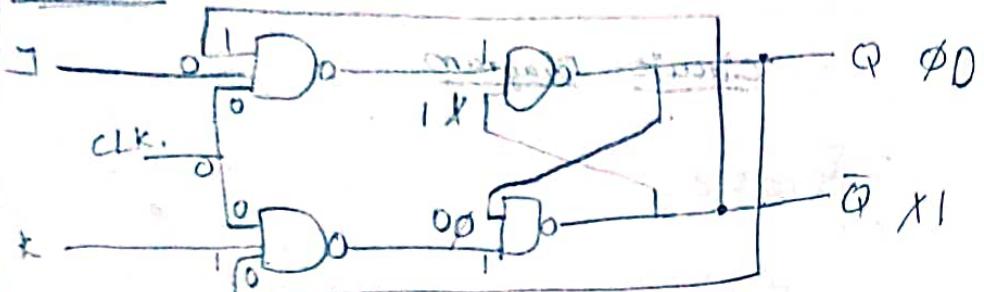
Simplified Truth Table:-

| CLK | J | K | Q |
|-----|---|---|-----------|
| 0 | x | x | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | RESET |
| 1 | 1 | 0 | SET |
| 1 | 1 | 1 | Q_{n+1} |

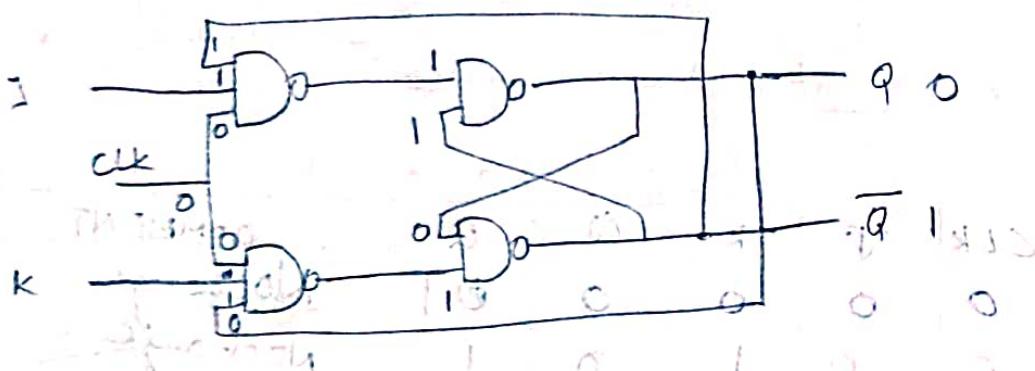
Case 1 $CLK=0, J=0, K=0$ [No-change]



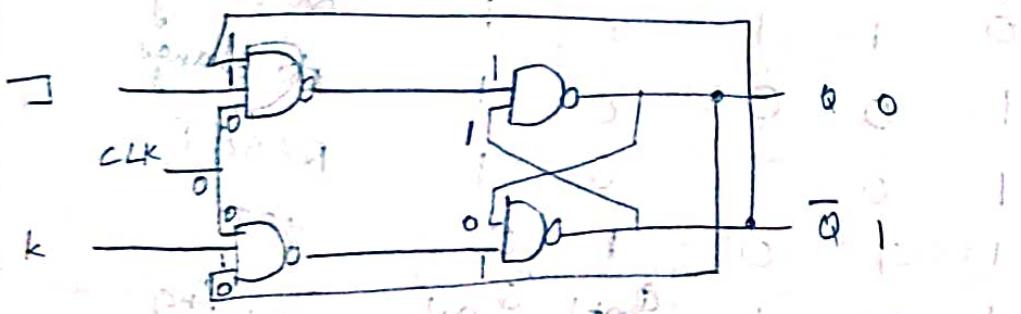
case 2 $CLK=0, J=0, K=1$ [No-change]



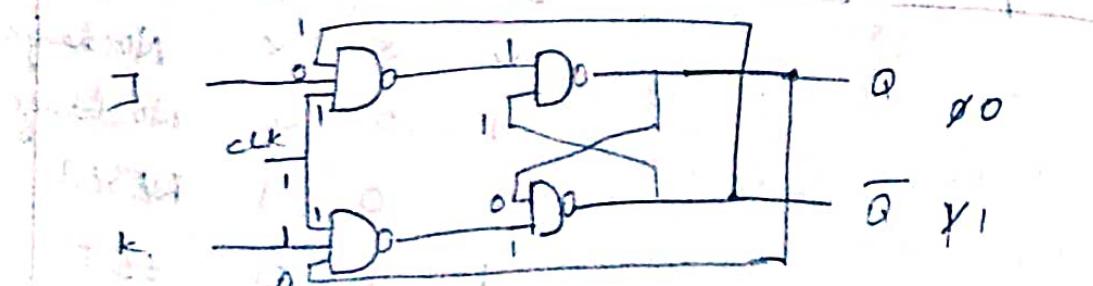
case 3 $CLK=0, J=1, K=0$ [No-change]



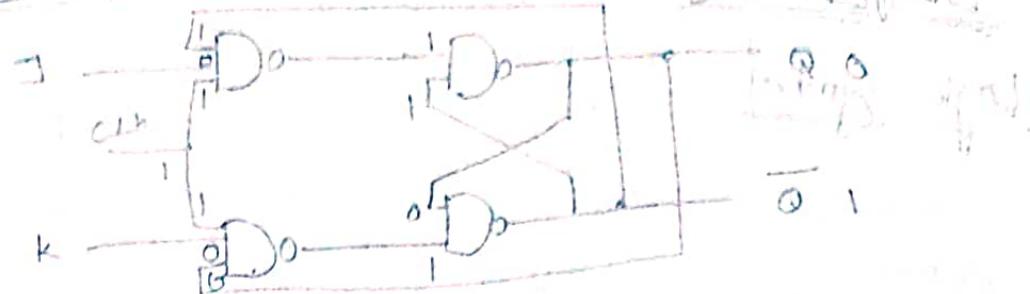
case 4 $CLK=0, J=1, K=1$ [No-change]



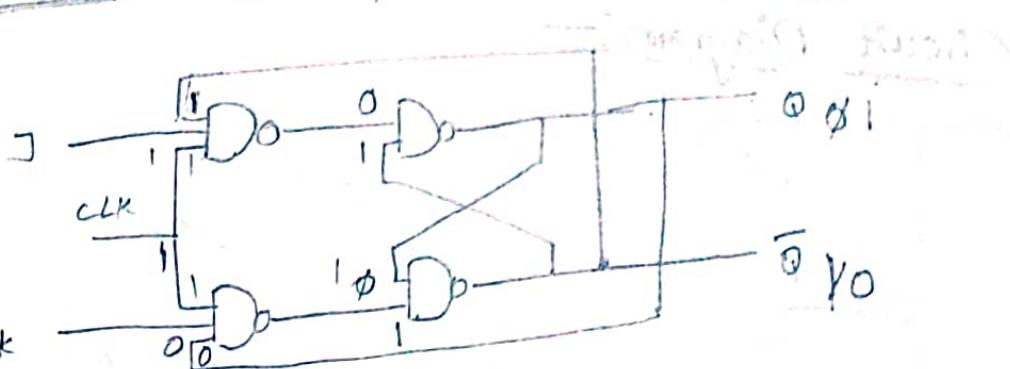
case 5 $CLK=1, J=0, K=1$ [RESET]



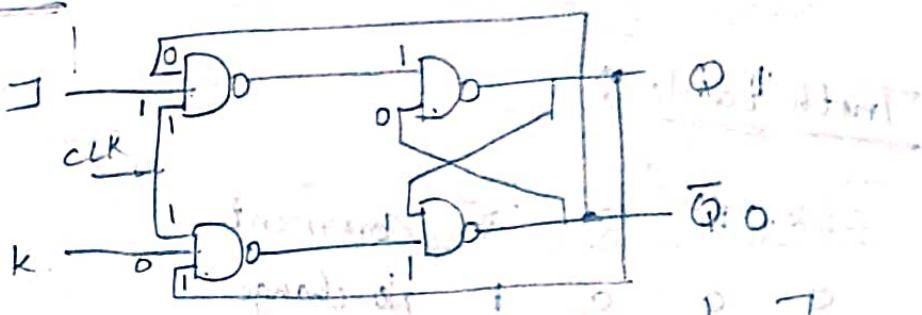
case 6: $clk=1, J=0, k=0$ [D flip-flop]



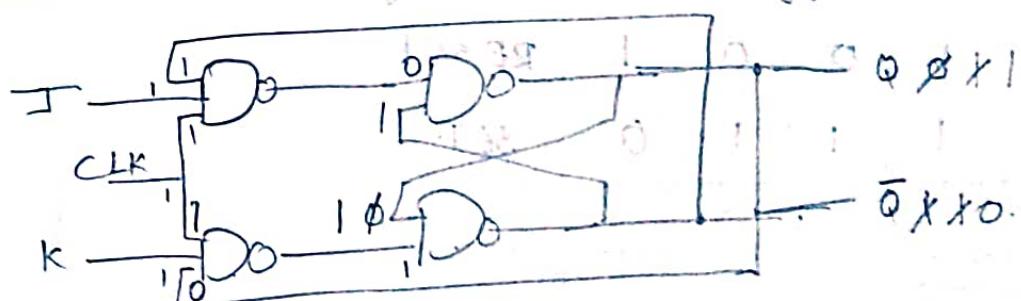
case 7: $clk=1, J=1, k=0$ [SET]



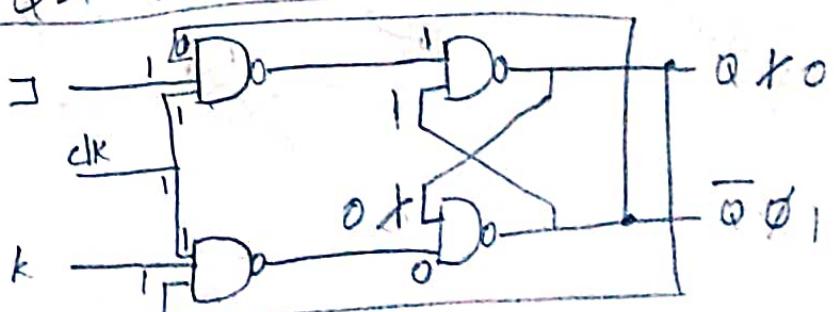
$$Q=1 \quad \bar{Q}=0$$



case 8: $clk=1, J=1, k=1$ [Toggle]

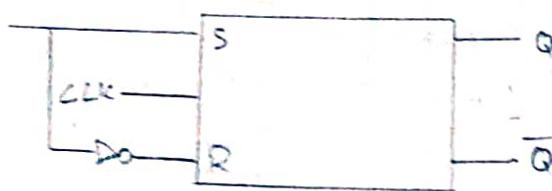


$$Q=1 \quad \bar{Q}=0$$

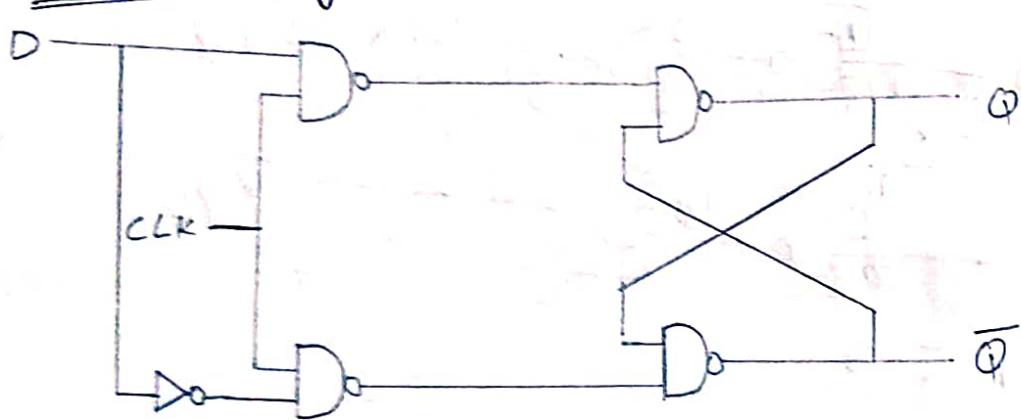


D-FLIP FLOP

Logic symbol



Circuit Diagram:-

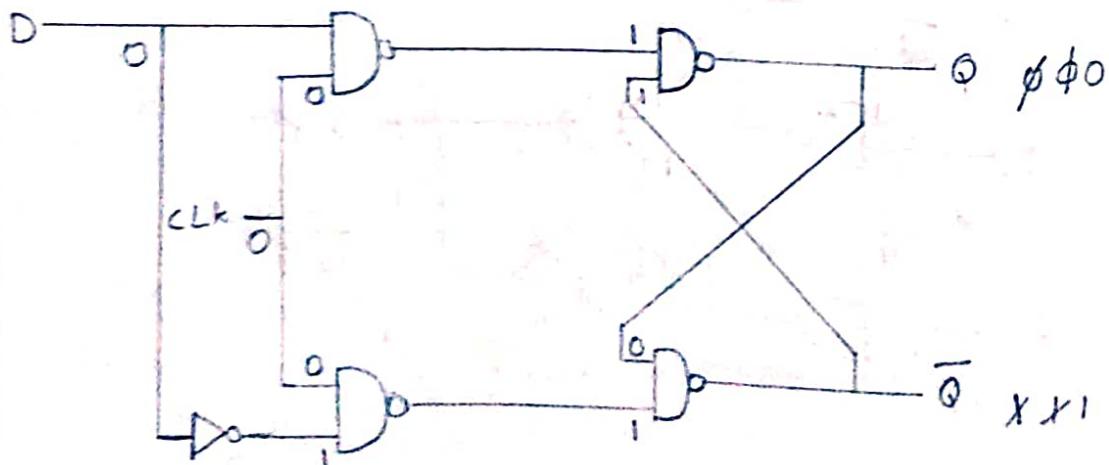


Truth table:-

| CLK | D | Q | \bar{Q} | Comment |
|-----|---|---|-----------|-----------|
| 0 | 0 | 0 | 1 | No-change |
| 0 | 1 | 0 | 1 | No-change |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | 1 | 0 | SET. |

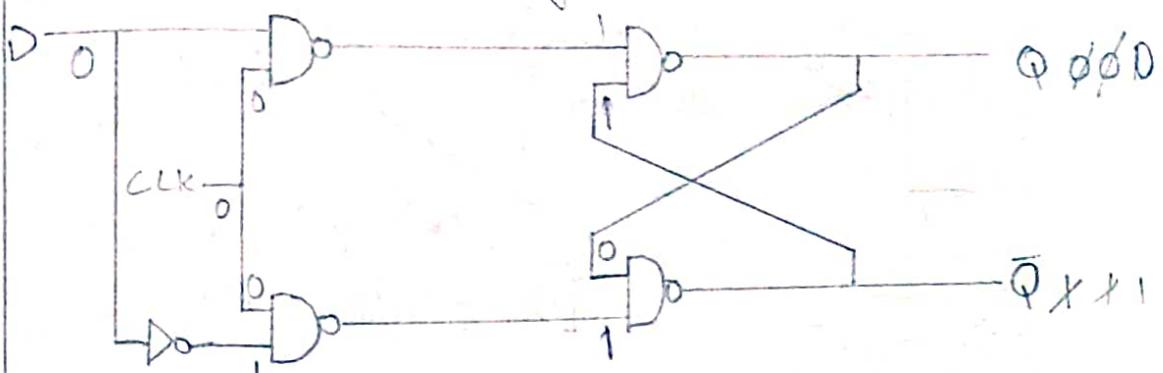
Case - 1

No-change



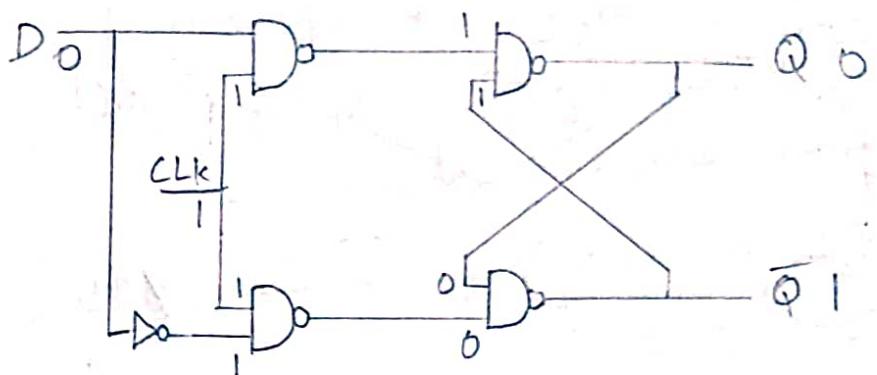
Case - 2 :-

No-change



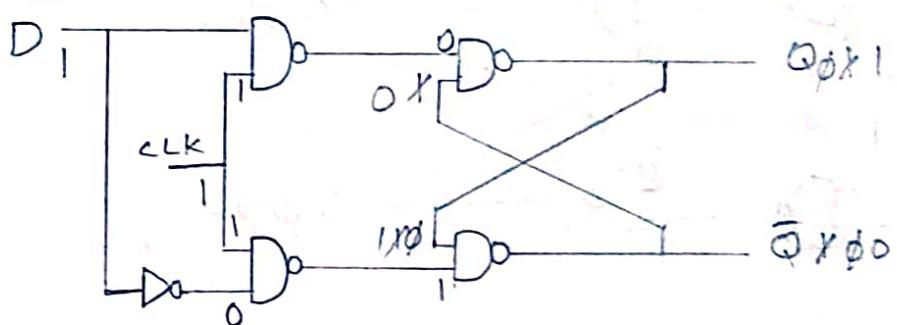
Case - 3 :-

RESET

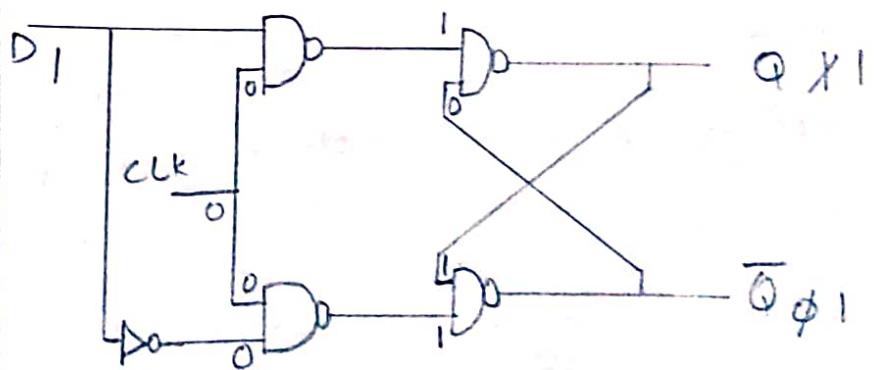


Case - 4 :-

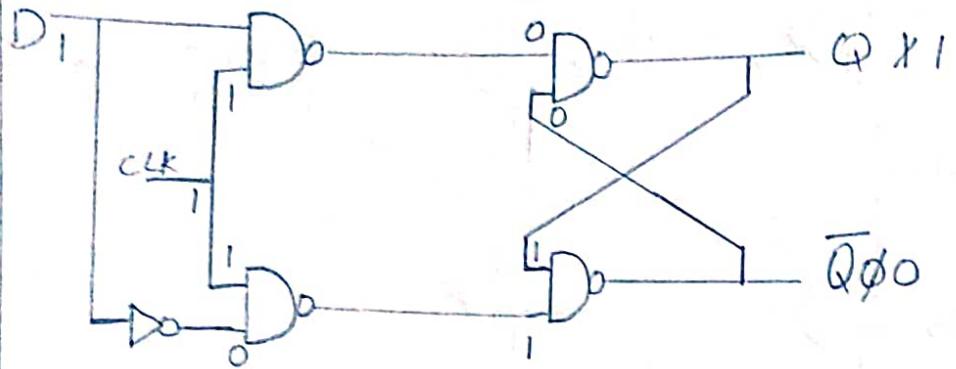
SET



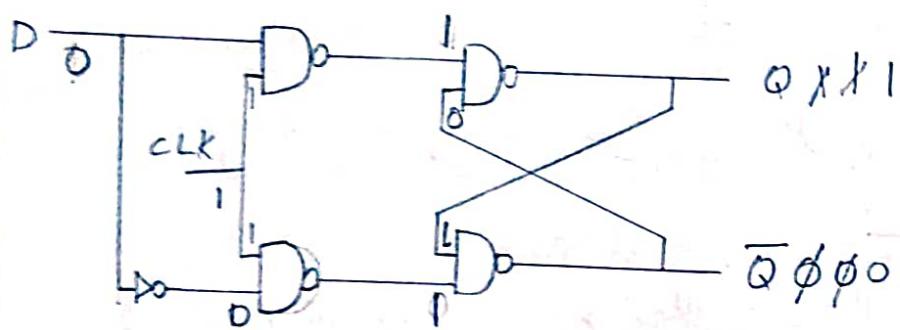
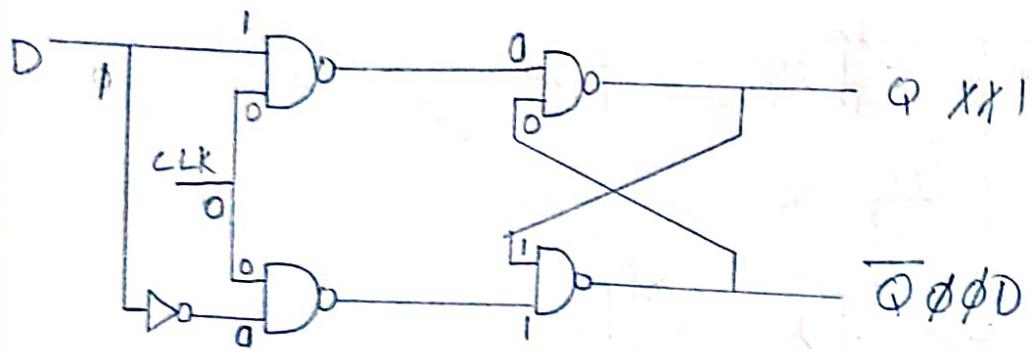
No change



No change

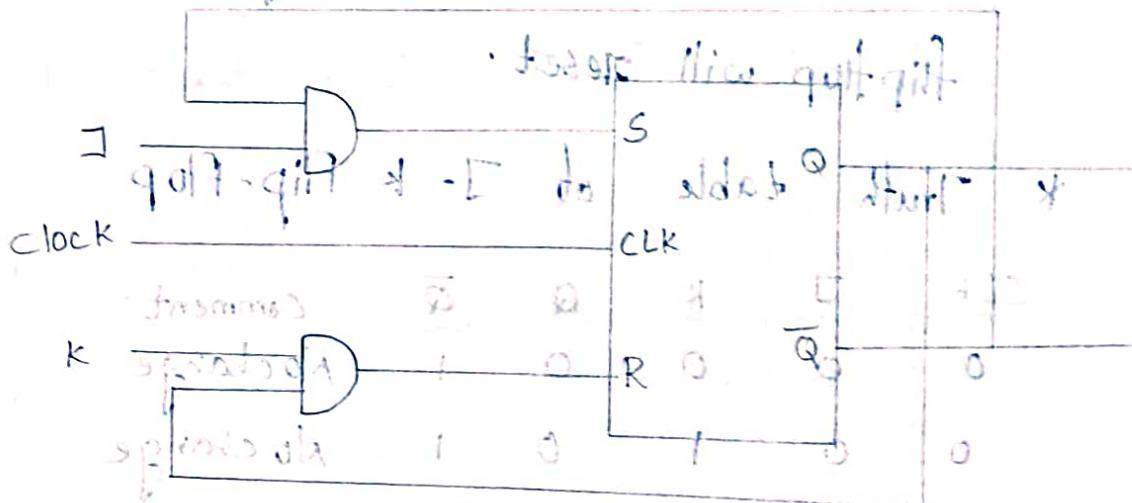


-SET

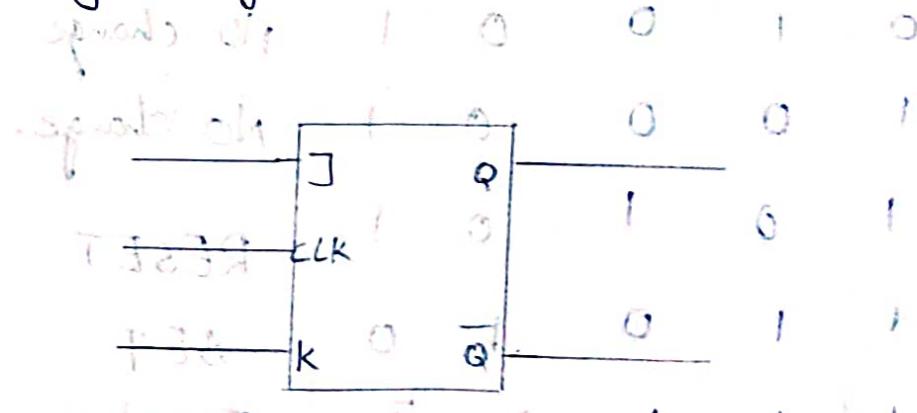


J-K FLIP FLOP

- * The J-K flip flop is the most widely used flip flop.
- * J-K flip flop is also known as universal flip flop because J-K flip flop can give the functionality of SR and T flip flop.
- * J-K flip flop is used in construction of ripple counter, decade synchronous counter.
- * The below diagram shows a J-K flip flop. J and K are the data inputs and CLK is the clock input and Q and \bar{Q} are the outputs.



* Logic diagram of J-K Flip Flop.



* Working of J-K Flip Flop.

\Rightarrow When both the inputs J and K are '0' the flip flop is in hold state. So it has no effect on output.

\Rightarrow In the hold state the inputs have no effect on output.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

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\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

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\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

\Rightarrow When both J and K are at logic '1', repeated clock pulses cause the outputs to turn off, on, off, and so on.

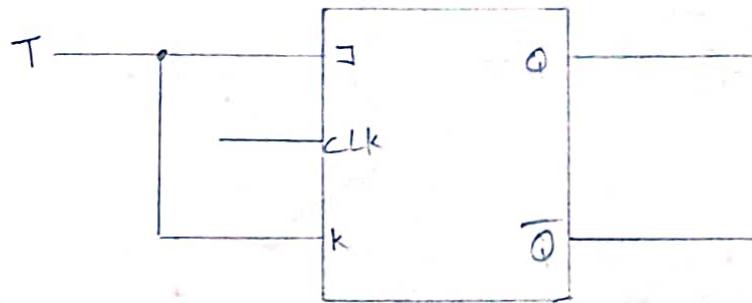
* Truth table of J-K Flip-Flop.

| CLK | J | K | Q | \bar{Q} | Comment |
|-----|---|---|------------|------------------|-----------|
| 0 | 0 | 0 | 0 | 1 | No change |
| 0 | 0 | 1 | 0 | 1 | No change |
| 0 | 1 | 0 | 0 | 1 | No change |
| 1 | 0 | 0 | 0 | 1 | No change |
| 1 | 0 | 1 | 0 | 1 | RESET |
| 1 | 1 | 0 | 1 | 0 | SET |
| 1 | 1 | 1 | Q_{nt+1} | \bar{Q}_{nt+1} | Toggle |

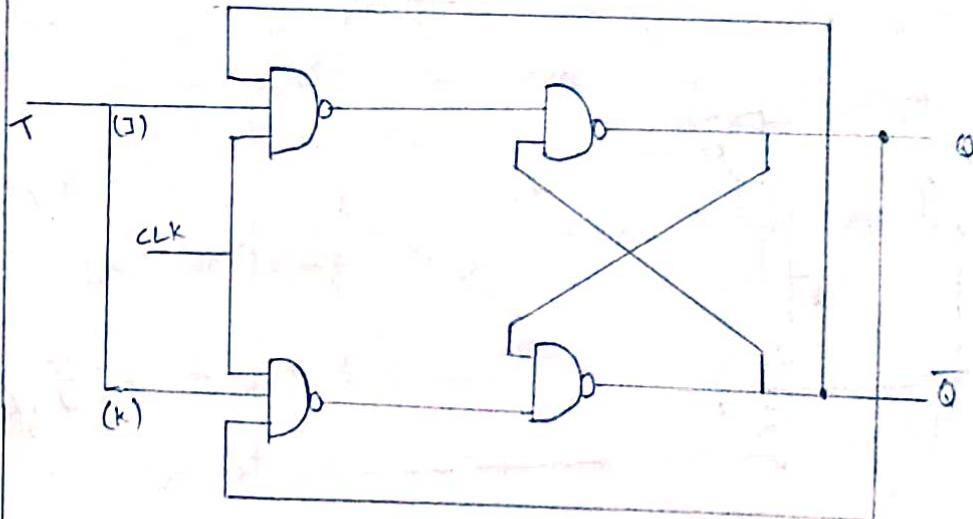
T- Flip Flop

T- flip flop is an edge triggered device. The low to high or high to low transitions on a clock signal of narrow trigger's that is provided as input will cause the change in output state of flip flop.

* Logic symbol of T- Flip Flop.



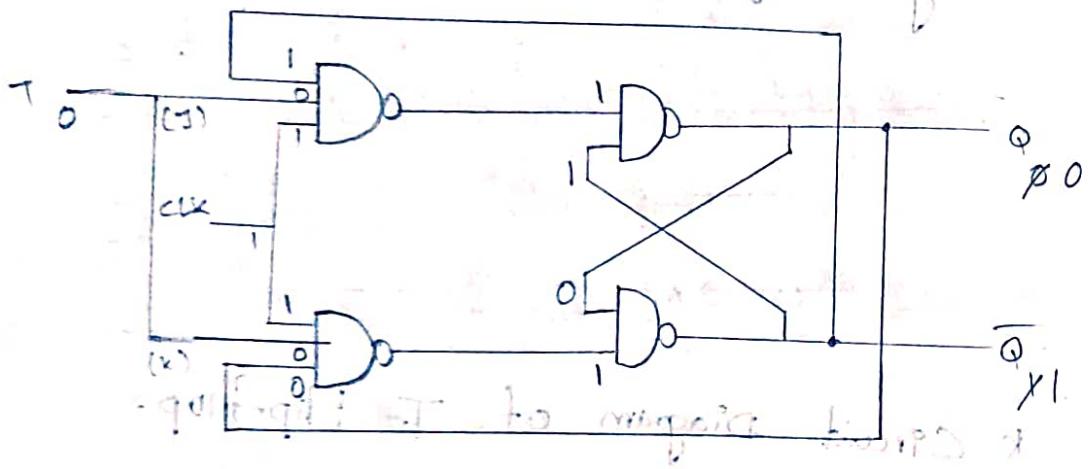
* Circuit Diagram of T-Flip-flop.



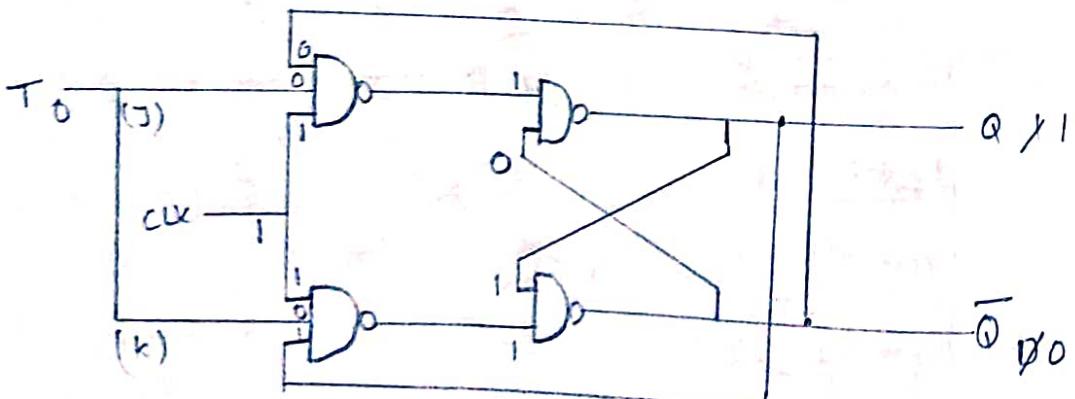
* Truth table of T- flip flop :-

| Case No. | CLK | T | Q | \bar{Q} | Comment |
|----------|-----|---|---|-----------|---------|
| 1 | 0 | 0 | 0 | 1 | Hold |
| 2 | 1 | 0 | 1 | 0 | Hold |
| 3 | 0 | 1 | 0 | 1 | Toggle |
| 4 | 1 | 1 | 1 | 0 | Toggle |

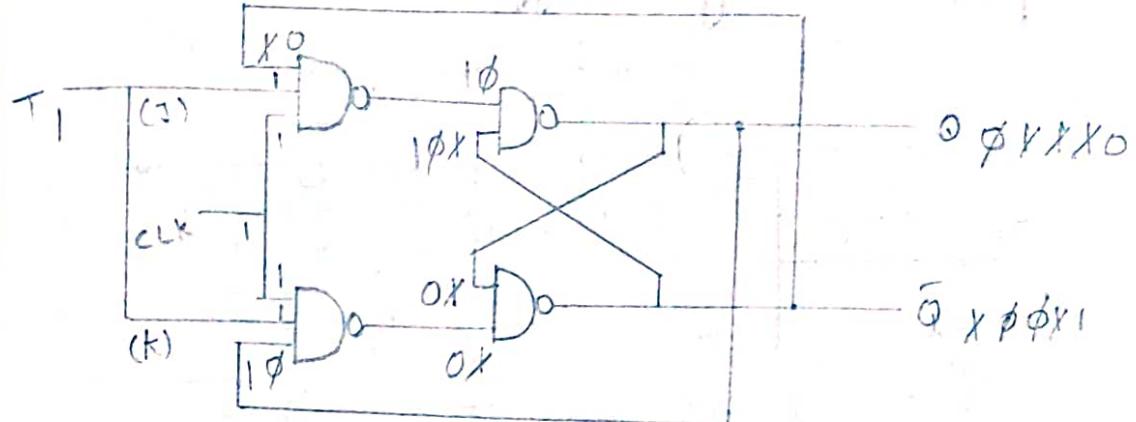
Case 1 :- $CLK = 1, T = 0$ [Hold]



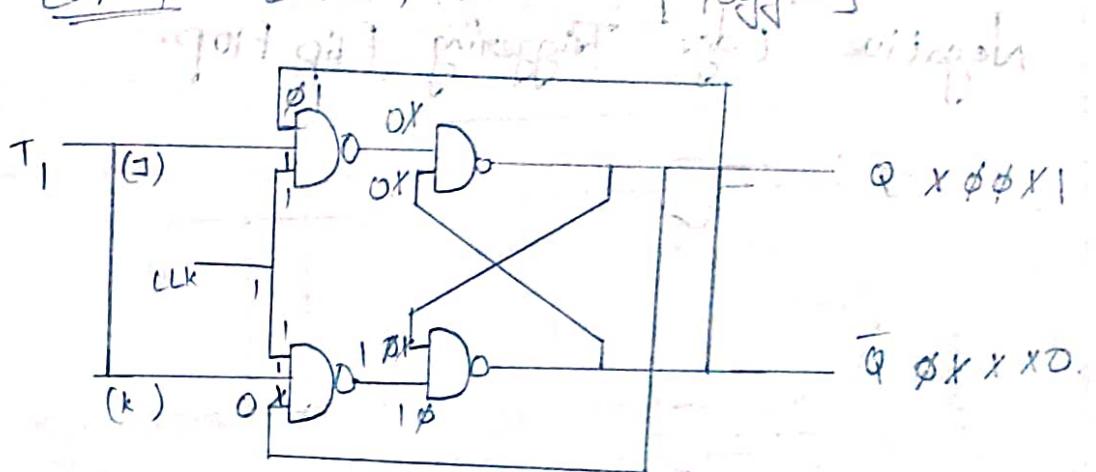
Case 2 :- $CLK = 1, T = 0$ [Hold]



Case 3 $CLK = 1, T = 1$ [Toggle] ~~Q = Q + 1~~



Case 4 $CLK = 1, T = 1$ [Toggle]



Edge & Level Triggering

* Edge Triggering: This means that the flip flop is changing the state either at the positive edge or negative edge of the clock pulse. ~~it goes all the time~~ No preditions.

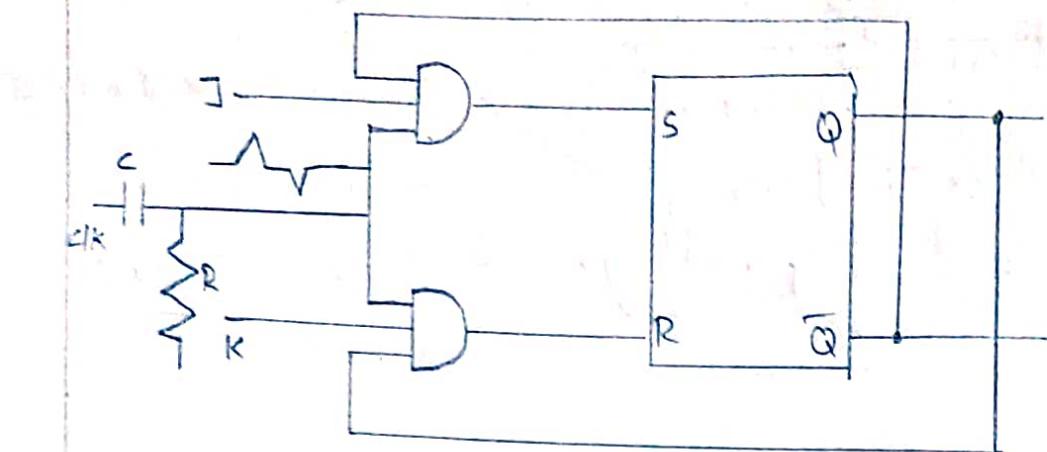
* Output is insensitive to other inputs, & only at the transition of the clock.

* +ve edge is also known as leading edge.

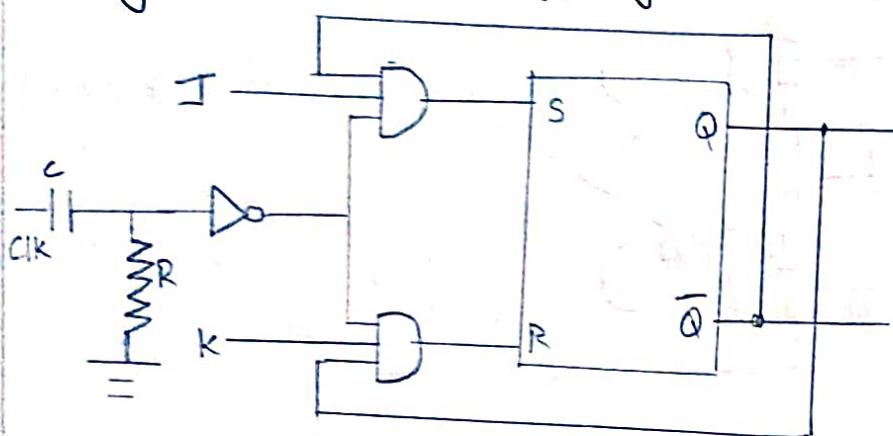
* -ve edge is also known as trailing edge.

• ~~means~~

Positive Edge triggered flip flop.



Negative Edge Triggering Flip Flop.



* Level Triggering:- The flip flop responds to the low and high level of the clock signal.

* The clock is thus a basic circuit controlling all the operations.

* These clock pulses initiate actions in flip-flops and logic gates.

* A simple square wave is called a clock, which is shown in the below diagram.

positive going (01) rising Edge.



So we find a falling edge & finding a rising edge triggers Negative going (i) Falling Edge.

```

graph LR
    A[Identify Risks] --> B[Assess Risks]
    B --> C[Prioritize Risks]
    C --> D[Develop Risk Response Plan]
  
```

Level triggered Flip FLOP.

~~Synchronous~~ ~~first~~ Synchronous sequential circuit

Shift Register is a sequential circuit in which the stages digital output of one stage is fed back to the input of the next stage.

governed by clock signals.

Asynchronous — On other hand Asynchronous

(9.1) Sequential Circuits are digital sequential circuits which involves memory cells.

3. video interface which provides feedback to the input for next
soft & platinium output set of constraints. so that
spbs output generation is not governed by
clock signals. set do

2020-01-20 10:00:00 - 2020-01-20 10:00:00

Wortbedeutung mit den Zusätzen - Lernvokabular mit

古文真賞

D/W edge triggering & Level triggering.

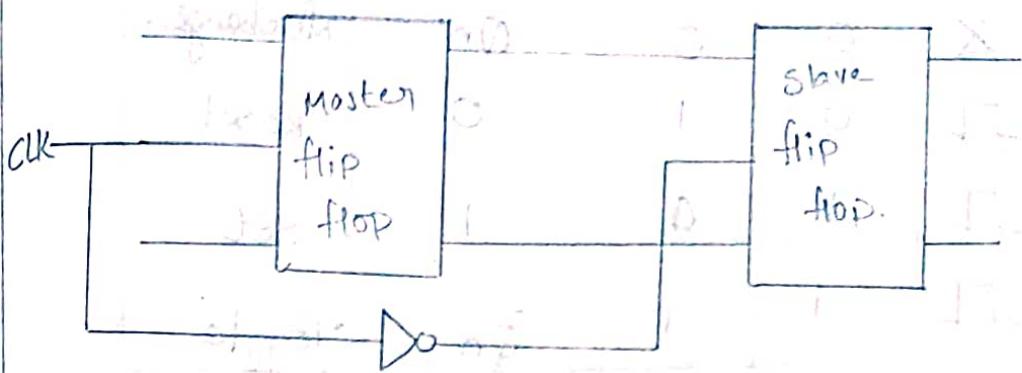
| Edge triggering. | Level clocking |
|--|---|
| When a circuit is edge-triggered, the output can change only on the rising or falling edge of the clock. | When a circuit level clocked the output can change while clock is high or low. |
| With edge triggering the output can change only at one instant during the clock cycle. | With level clocking, the output can change during an entire half cycle of the clock. |
| An edge triggering clock is obtained using a constant RC circuit fed to the clock input of a flip-flop. | It's level clocked the square wave clock is directly fed to clock input of a flip-flop. |

D/W SYNCHRONOUS & ASYNCHRONOUS Inputs

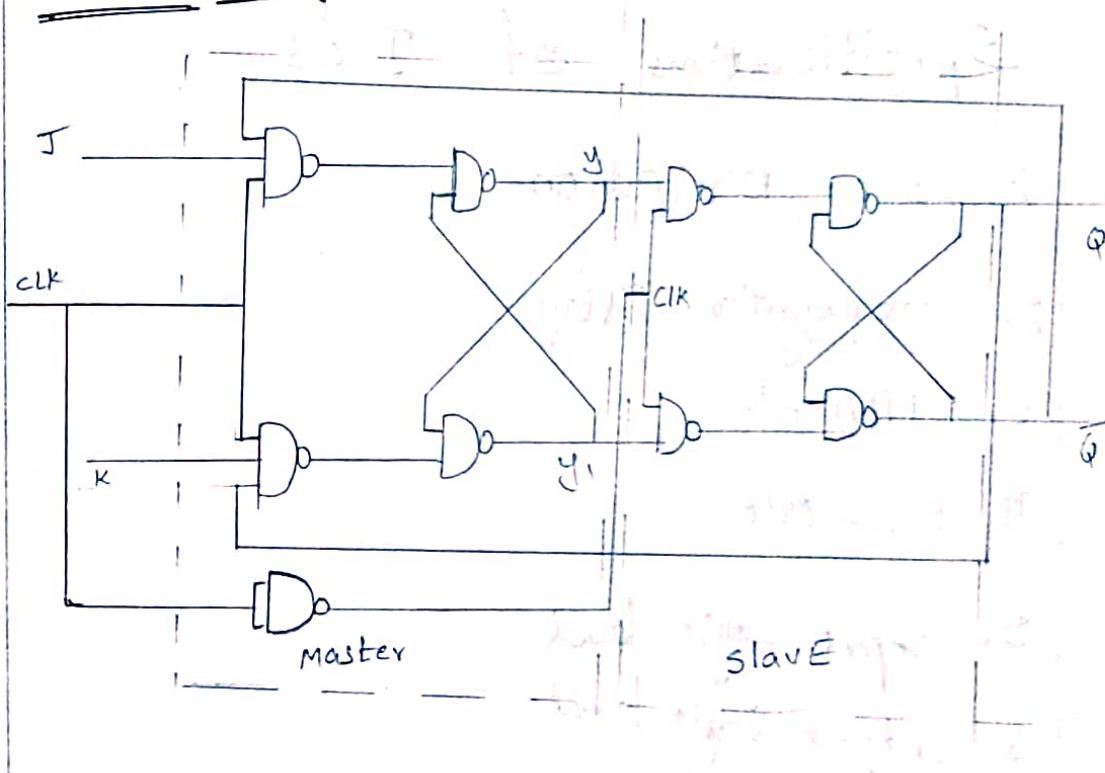
| Synchronous Inputs | Asynchronous Inputs |
|---|--|
| The S-R, D & J-K are called synchronous inputs. | The asynchronous inputs are PRESET (PR) and CLEAR (CLR). |
| The data on the synchronous inputs are transferred to the output of a flip-flop only. | The asynchronous inputs active on the triggered edge of the clock pulse. |
| These inputs will not affect the synchronous. | These inputs override the effect of the synchronous inputs. |

MASTER SLAVE FLIP-FLOP

Logic Diagram:-



Circuit Diagram:-



When clock is high(1) master flip flop is on (active)

When clock is low(0) slave flip flop is off (inactive).

When clock is low(0) master flip flop is off (inactive)

When clock is high(1) slave flip flop is on (active)

Master slave flip flop TRUTH TABLE

| Inputs | | | outputs | |
|--------|----|----|------------------|------------|
| CLK | In | kn | Q _{n+1} | Comment |
| X | 0 | 0 | Q _n | No change. |
| [L] | 0 | 1 | 0 | Reset |
| [L] | 1 | 0 | 1 | Set |
| [L] | 1 | 1 | \bar{Q}_n | Toggle. |

Specifications of IC's

1. Power Dissipation

2. Propagation Delay

3. FID - In

4. Fan - Out

5. Input Logic level

6. Output Logic level

7. compatibility

8. Noise Margin

9. Speed power product.

CHAPTER - 3

9/0

1 mark for diagram

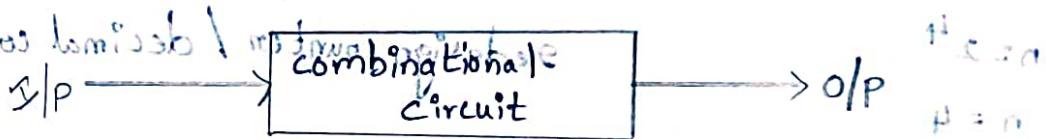
COUNTERS AND REGISTERS

from
forms

COUNTER:- Counter is a device which stores the number of times a particular event or process has occurred , often in relationship to a clock. The most common type is a sequential circuit.

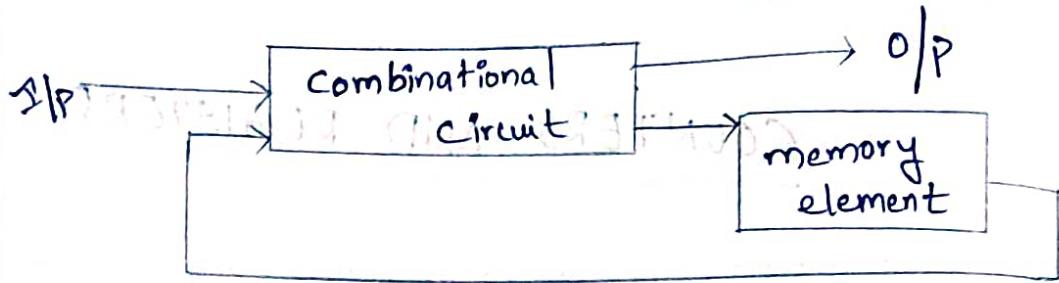
Combinational logic circuit:-

Combinational logic circuits are memoryless digital logic circuits whose outputs at any instant in time depends on the combination of its inputs.



Sequential logic circuit:-

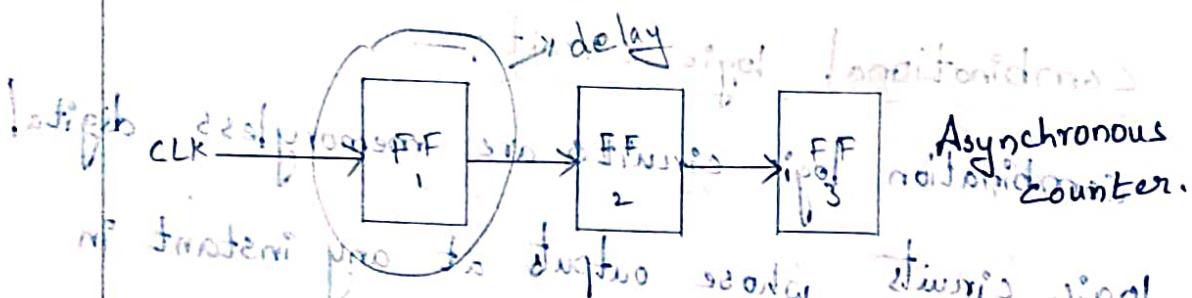
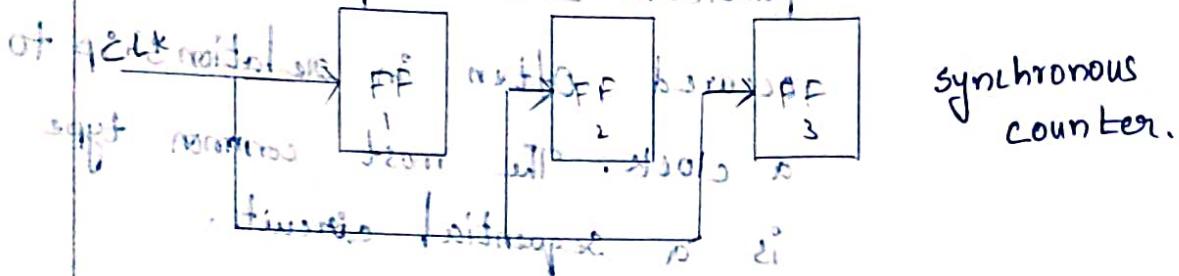
Sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the sequence of past inputs, the input history as well. This is in contrast to combinational logic, whose output is a function of only the present input.



design gives us an advantage - COUNTER

3-bit counter down with 2 inputs

last 4 words is basic working



• Invert di to no inversion set 1111

16 states \rightarrow mod 10 counter (0-9) / ripple counter.

$$n = 2^4$$

→ redesign counter / decimal counter

$$n = 4$$

\Rightarrow 4 bit binary counter.

$8 = 2^3$ signal to invert or not invert

$3 + 8 = 2^3$ bits no plus for oblique digits

$3 + 8 = 2^3$ bit binary counter.

2 bits. If we invert digit then feed to

oblique digits without loss of information n 2

digit freezing with plus do no invert n 2

Mod-8 Counter.

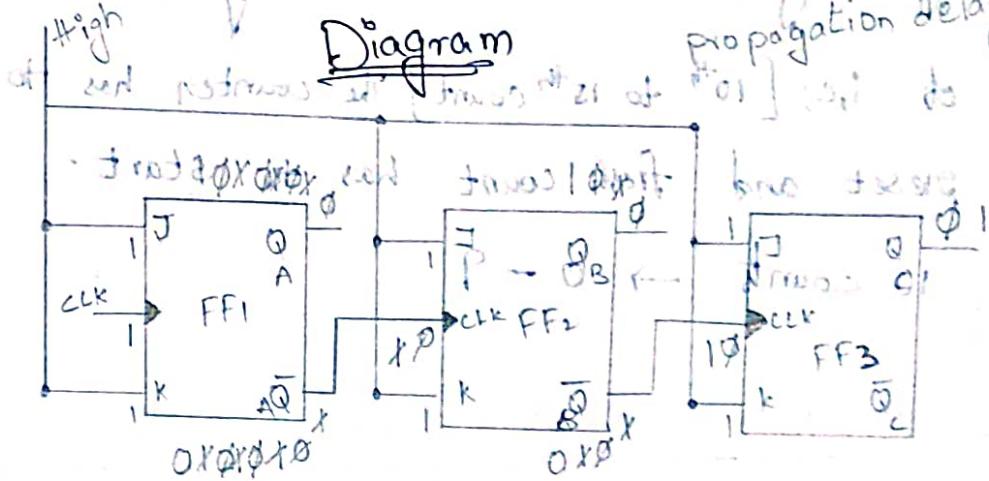
Asynchronous mode :- [Ripple counter]

$$8 \rightarrow 2^3$$

$$8 \rightarrow 2^3$$

$$n = 3$$

so, we want 3 FFs
of each postures at time of t_0 [as it has propagation delay.]



Outputs :- $Q_C Q_B Q_A$.

| CLK | Q_C | Q_B | Q_A |
|-----|-------|-------|-------|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 |
| 8 | 0 | 0 | 0 |
| 9 | 0 | 0 | 0 |
| 10 | 0 | 0 | 1 |
| 11 | 0 | 1 | 0 |
| 12 | 0 | 1 | 1 |
| 13 | 1 | 0 | 0 |
| 14 | 1 | 0 | 1 |
| 15 | 1 | 1 | 0 |
| 16 | 0 | 1 | 1 |
| 17 | 0 | 0 | 0 |
| 18 | 0 | 0 | 0 |
| 19 | 0 | 0 | 1 |
| 20 | 0 | 1 | 0 |
| 21 | 0 | 1 | 1 |
| 22 | 1 | 0 | 0 |
| 23 | 1 | 0 | 1 |
| 24 | 1 | 1 | 0 |
| 25 | 0 | 1 | 1 |
| 26 | 0 | 0 | 0 |
| 27 | 0 | 0 | 0 |
| 28 | 0 | 0 | 1 |
| 29 | 0 | 1 | 0 |
| 30 | 0 | 1 | 1 |
| 31 | 1 | 0 | 0 |

Mod- 10-Counter

Asynchronous mode : decade counter

$$16 \rightarrow 2^n$$

$$16 \rightarrow 2^4$$

$$n = 4$$

$$C_c \leftarrow 8$$

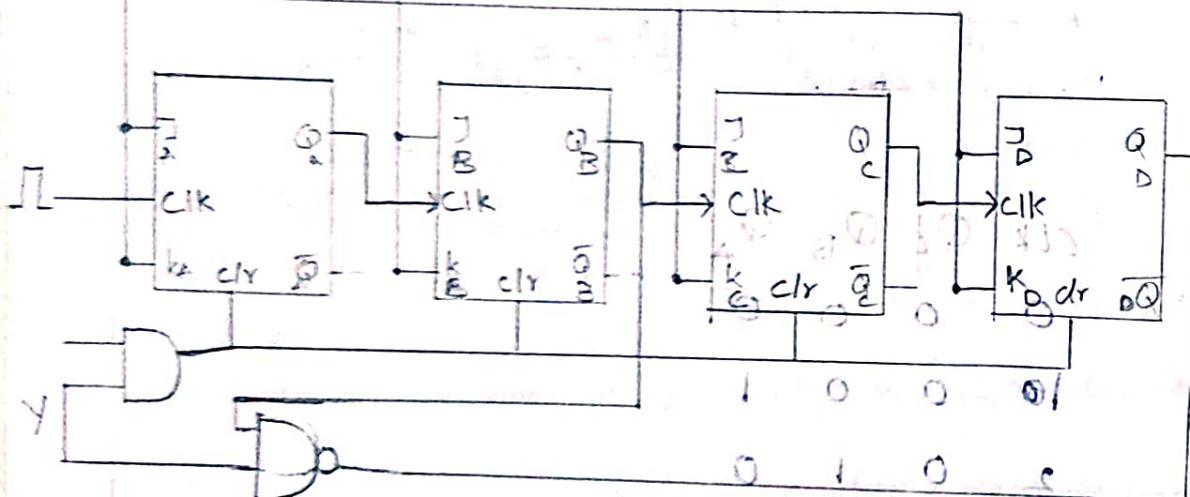
$$E_c \leftarrow 8$$

$$(C) \leftarrow n$$

by using this we can reducing 6 states

of i.e; [10th to 15th count] The counter has to
reset and fresh count has to start.

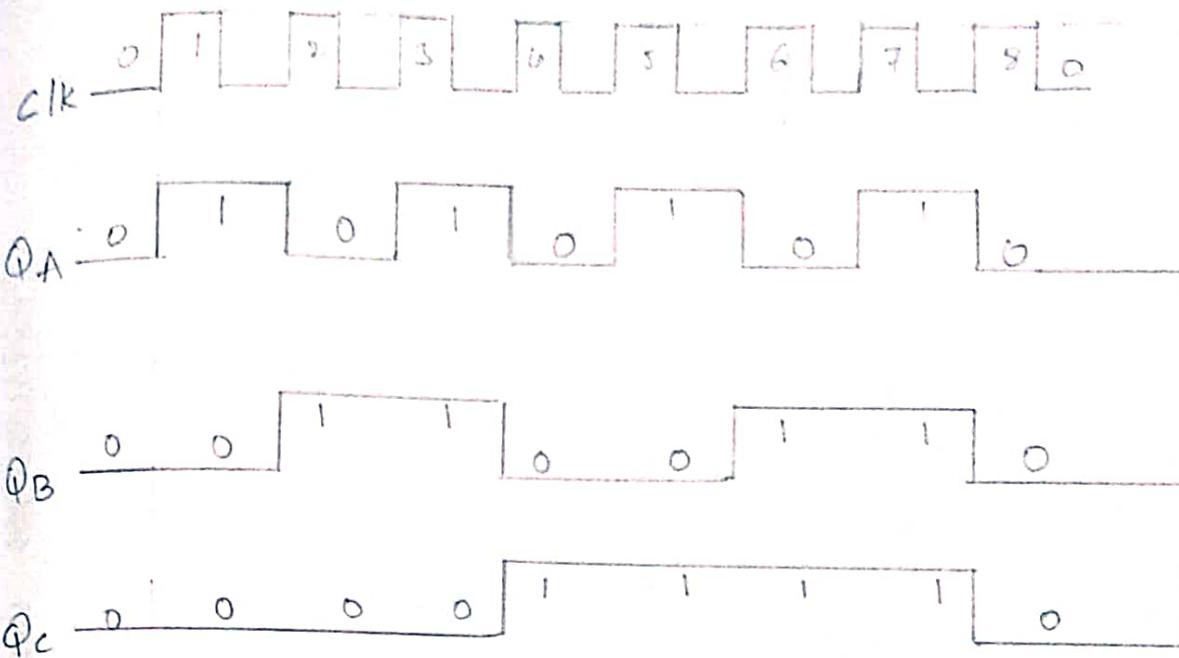
^{High} 10 counts $\rightarrow 0 - 9$



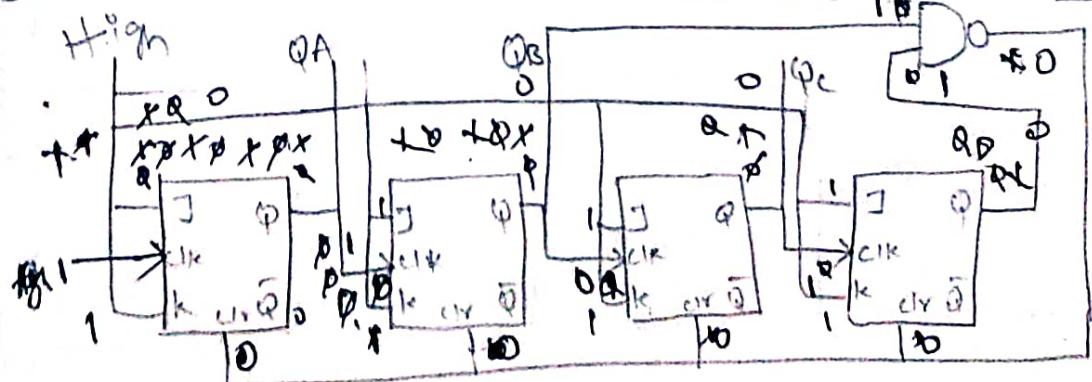
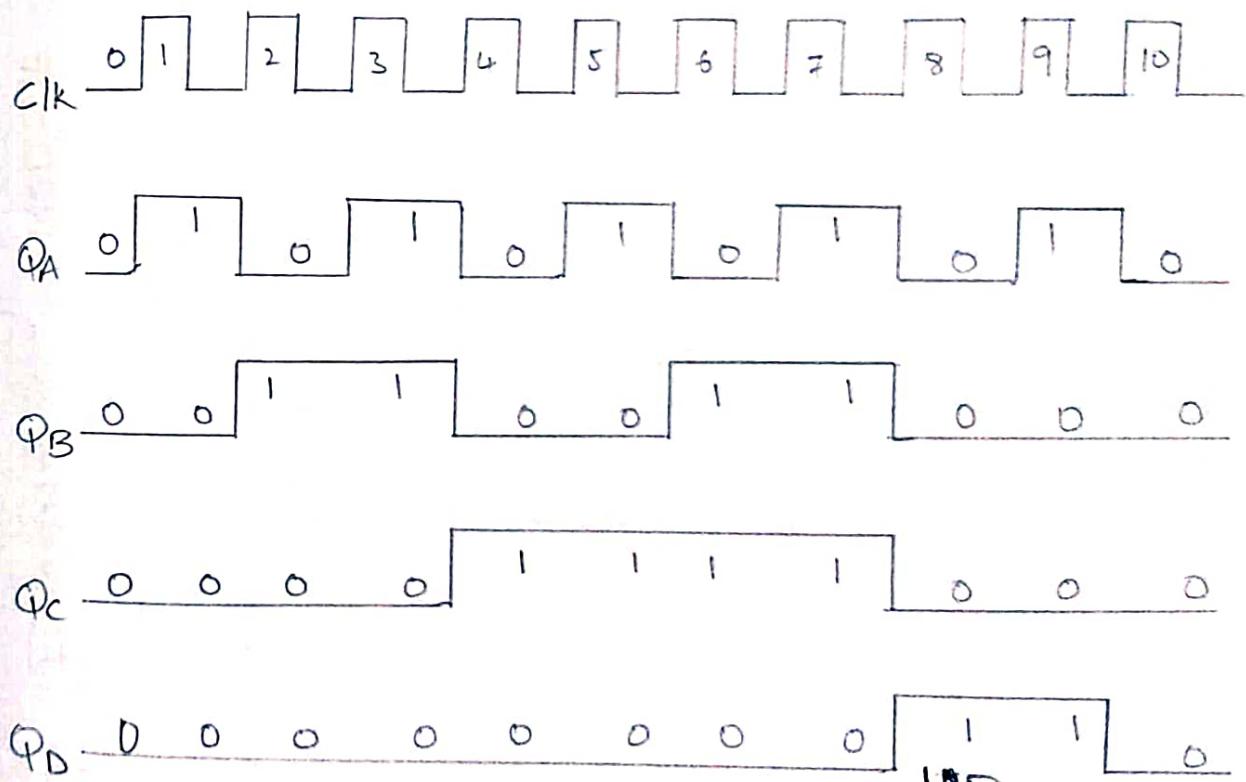
| Clr | Q _D | Q _C | Q _B | Q _A |
|-----|----------------|----------------|----------------|----------------|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |

| Clr | Q _D | Q _C | Q _B | Q _A |
|-----|----------------|----------------|----------------|----------------|
| 16 | 0 | 0 | 1 | 1 |
| 07 | 1 | 0 | 1 | 1 |
| 18 | 1 | 1 | 0 | 0 |
| 09 | 0 | 1 | 0 | 0 |
| 10 | 0 | 0 | 0 | 0 |

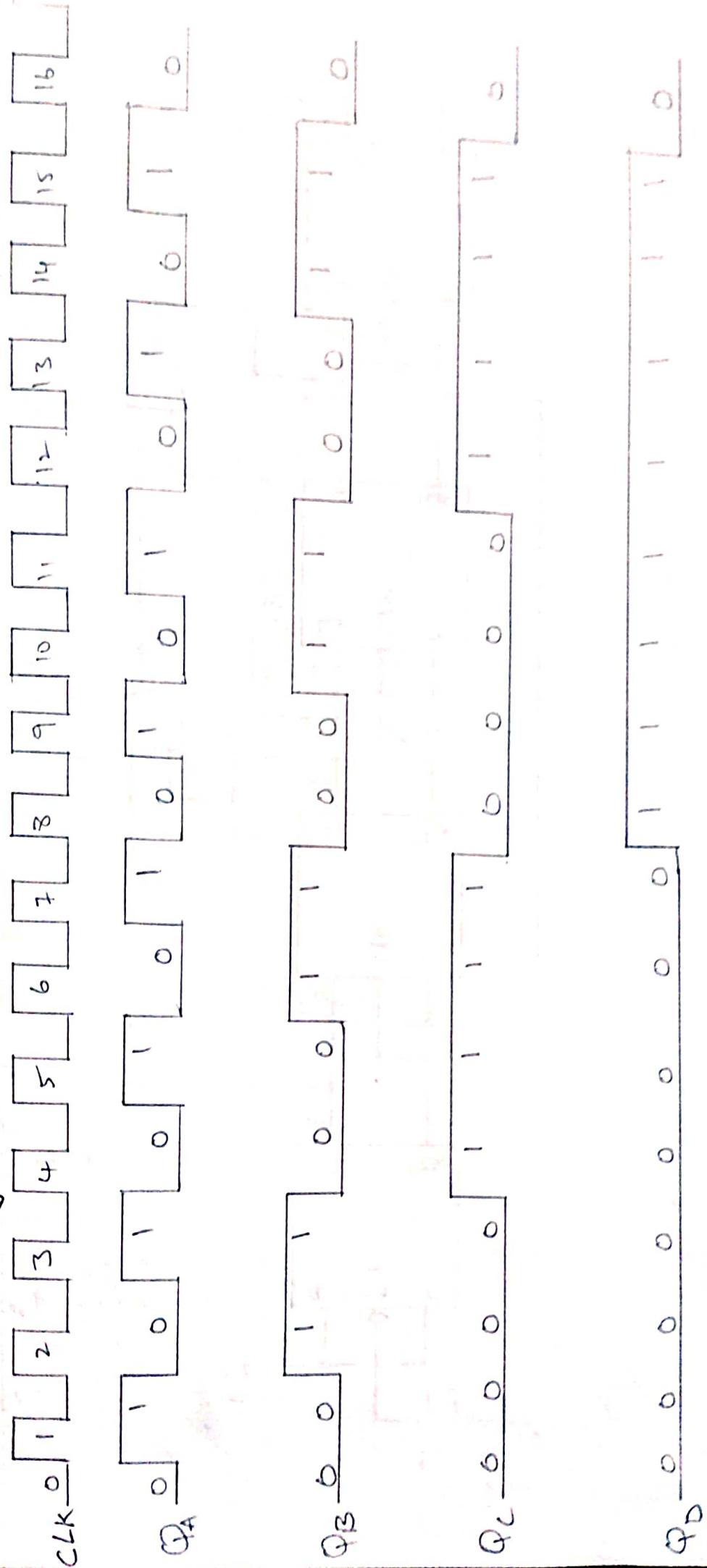
Timing Diagram [MOD-8 Asynchronous Counter]



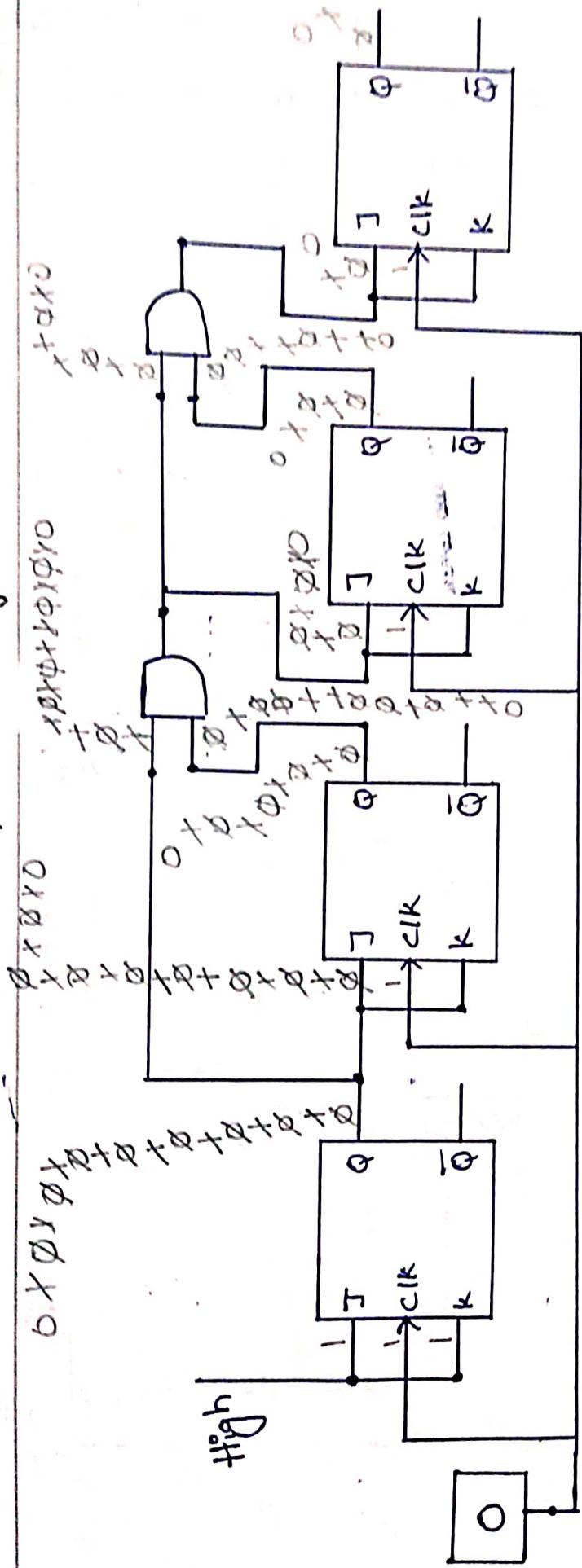
Timing Diagram [MOD-10 Asynchronous Counter].



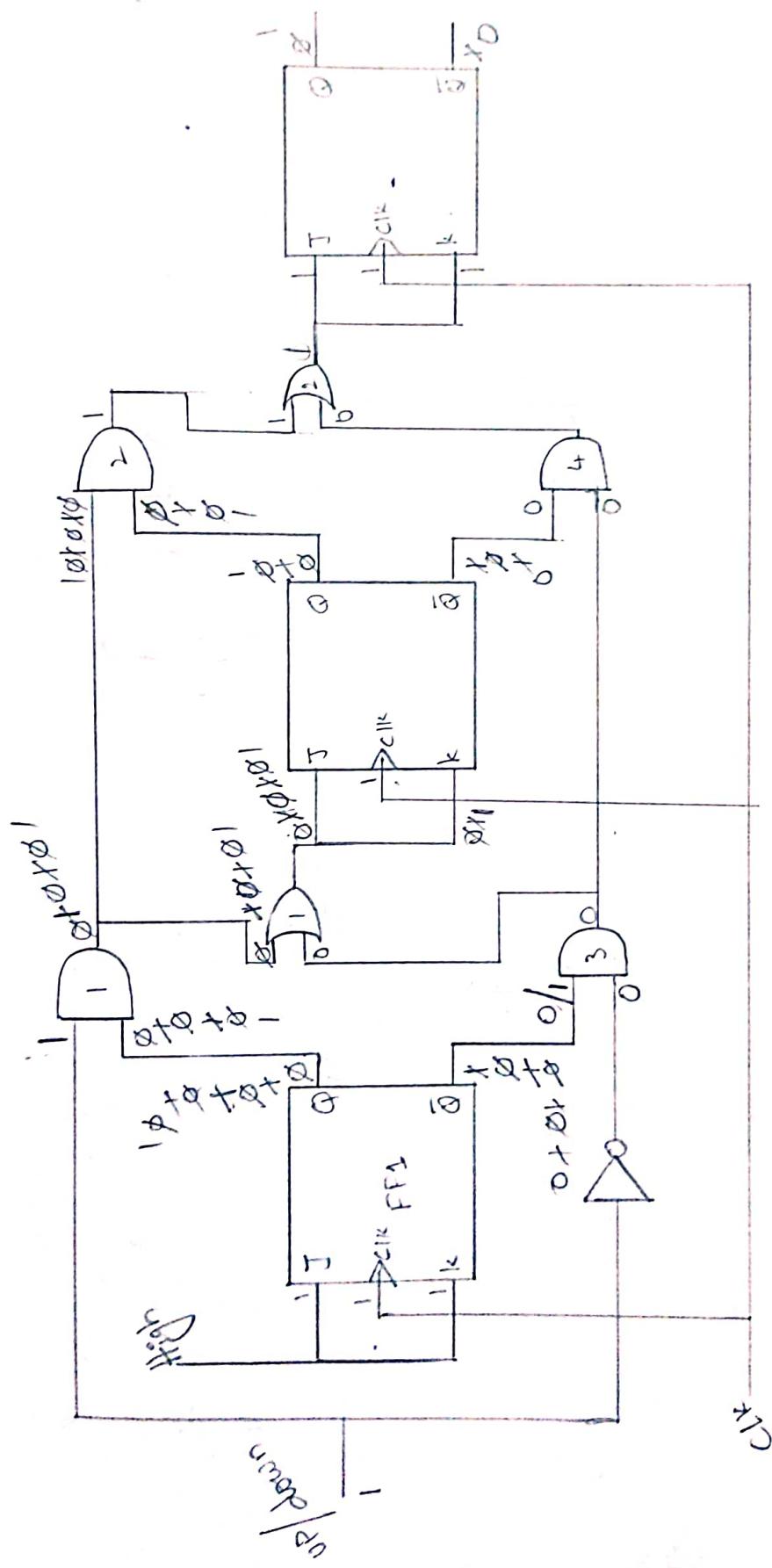
Timing Diagram :— MOD-16 Asynchronous counter.



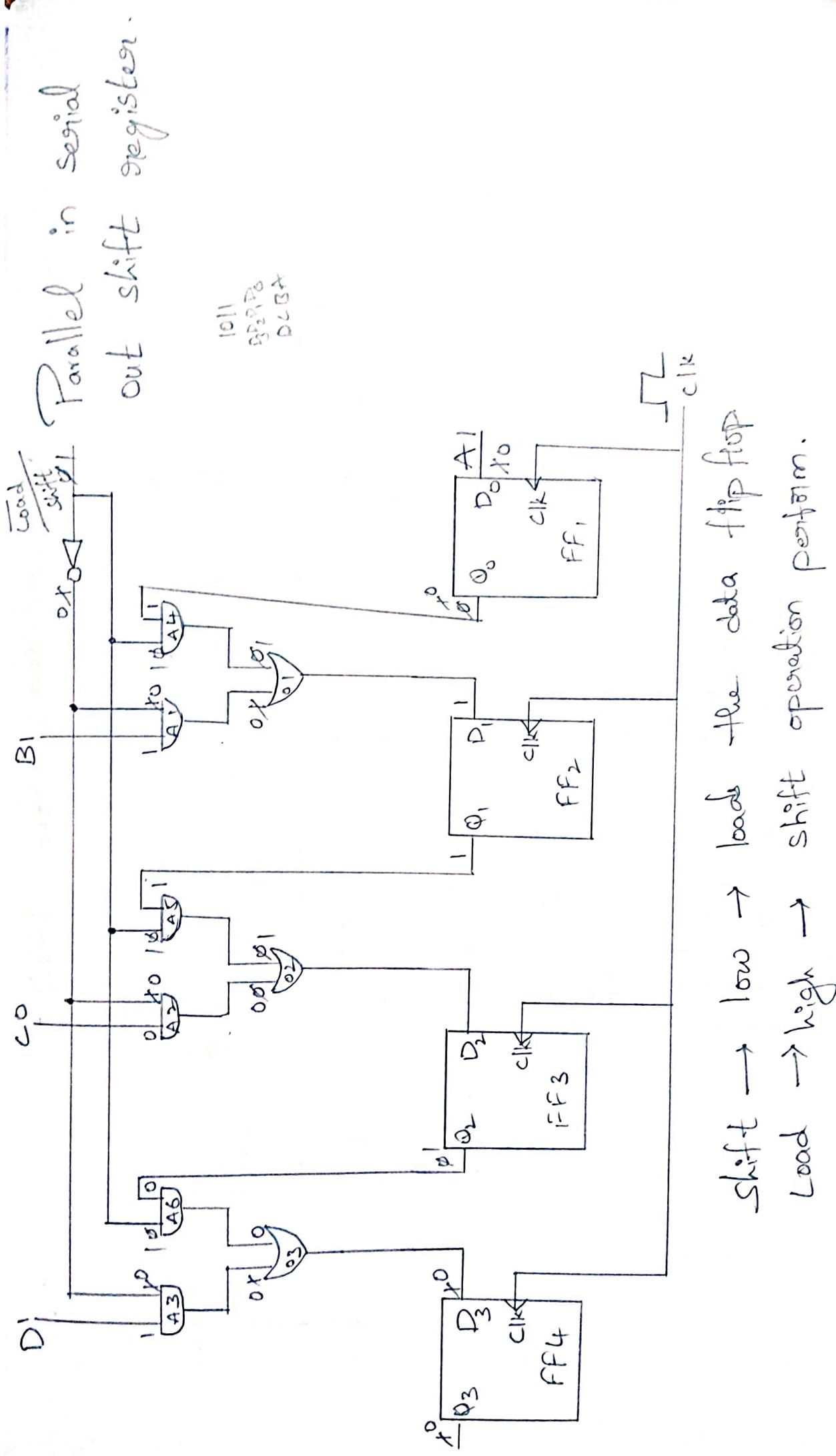
4-bit Synchronous Counter.



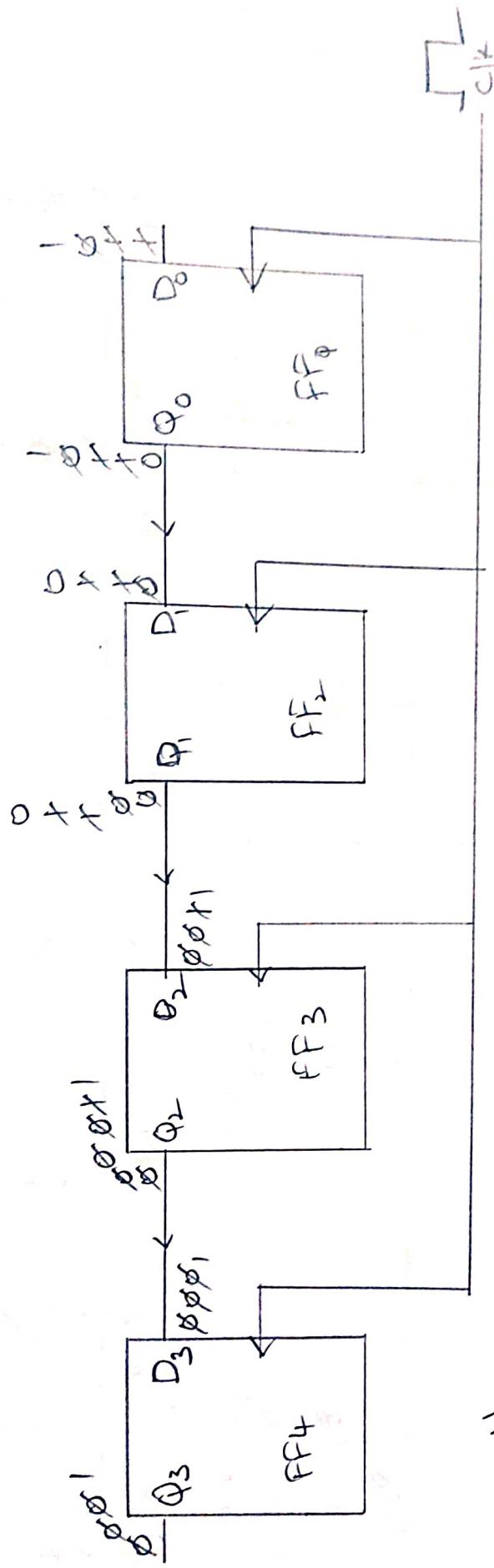
| | | | | | | | | | | | | | | | |
|--|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Q _A | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| | Q _B | 0 | 0 | - | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| | Q _C | 0 | 0 | 0 | 0 | - | - | - | - | - | - | - | - | - | - |
| | | 0 | - | 2 | 3 | 4 | 5 | 6 | 1 | 7 | - | - | - | - | - |



Upwards Counter.



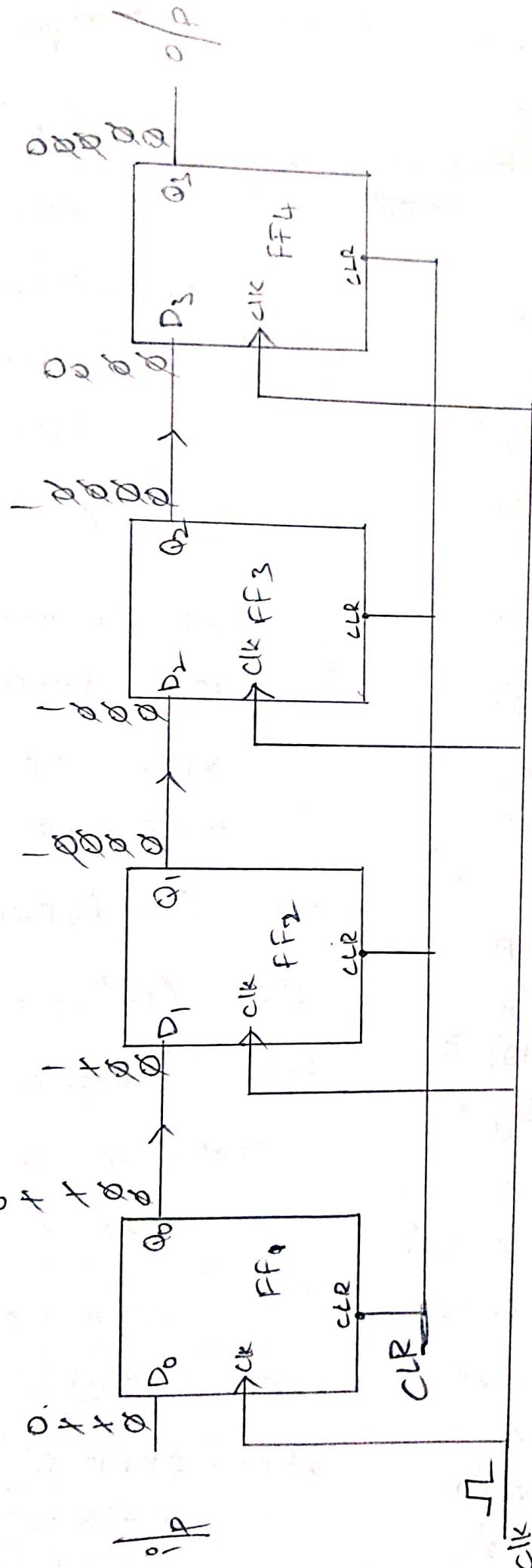
Shift Left Register.



$$D = 1011$$

| Clk | D | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
|-----|---|----------------|----------------|----------------|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | - | 0 | 0 | 0 | 0 |
| 2 | - | 0 | 0 | - | 1 |
| 3 | 1 | 0 | - | - | 0 |
| 4 | 1 | 1 | - | - | 0 |

Shift Right Register :-



| | Q3 | Q2 | Q1 | Q0 | CLK |
|-----|----|----|----|----|-----|
| Q3 | 0 | 0 | 0 | 0 | - |
| Q2 | 0 | 0 | 0 | 0 | - |
| Q1 | 0 | 0 | 0 | - | - |
| Q0 | 0 | 0 | - | - | 0 |
| D | 1 | 0 | - | - | 0 |
| CLK | 0 | - | 1 | 0 | 1 |

$$D = 0.115 \cdot D_{392}$$

$$3. (543)_{10} \Rightarrow [1000011111]_2$$

$$1. 2481. [100110110001]$$

$$\text{1's complement} = [011001001110]$$

$$\text{2's complement} = [011001001111]$$

$$(2^{12}-1) - 2481$$

$$\Rightarrow (4096-1) - 2481$$

$$\Rightarrow 4095 - 2481$$

$$1's \Rightarrow 1614$$

$$2's = 1615$$

$$(10^4 - 1) - 2481$$

$$(10000 - 1) - 2481$$

$$9's = 9999 - 2481$$

$$9's = 7518$$

$$10's = 7519$$

$$2. (1376)_{10} = (10101100000)_2$$

$$\text{1's} = (2^{11}-1) - 1376$$

$$\Rightarrow (2048-1) - 1376$$

$$\Rightarrow 2048 - 1376$$

$$1's \Rightarrow 672$$

$$2's = 673$$

$$9's = (10^4 - 1) - 1376$$

$$\Rightarrow 9999 - 1376$$

$$9's \Rightarrow 8623$$

$$10's \rightarrow 8624$$

$$1's \Rightarrow 982$$

$$9's = (10^3 - 1) - 543$$

$$\Rightarrow 999 - 543$$

$$9's \Rightarrow 456$$

$$10's \Rightarrow 457$$

$$4. (978)_{10} \Rightarrow [1111010010]_2$$

$$1's \Rightarrow (2^{10}-1) - 978$$

$$\Rightarrow (1024-1) - 978$$

$$1's \Rightarrow 1023 - 978 \Rightarrow 45$$

$$1's \Rightarrow 45$$

$$2's \Rightarrow 46$$

$$9's = (10^3 - 1) - 978$$

$$\Rightarrow (1000-1) - 978$$

$$9's \Rightarrow 999 - 978 \Rightarrow 21$$

$$10's \Rightarrow 22$$

$$5. (6154)_{10} \Rightarrow [1100000001010]_2$$

$$1's = (2^{13}-1) - 6154$$

$$\Rightarrow 8192 - 6154$$

$$1's \Rightarrow 2038$$

$$2's \Rightarrow 2039$$

$$9's = (10^4 - 1) - 6154$$

$$\Rightarrow 9999 - 6154 \Rightarrow 4845$$

$$9's \Rightarrow 3845$$

$$10's \Rightarrow 3846$$

CHAPTER-6

INFORMATION REPRESENTATION

ARITHMETIC OPERATIONS

Fixed-point Addition & Subtraction

$$\begin{array}{r}
 \text{AS} \\
 + \\
 (+) \quad -13 \\
 \hline
 -15
 \end{array}
 \quad
 \begin{array}{r}
 \text{BS} \\
 + \\
 B \\
 \hline
 1101
 \end{array}$$

[STRUCTION III] $(A + B) = A + B$

AS \oplus BS

$$\begin{array}{r}
 \text{SF} : (1-010) \rightarrow 2^1 \\
 1 \oplus 1 = 0
 \end{array}$$

$$\text{SFP} : (1-0001) \rightarrow 2^1$$

$$EA \leftarrow \begin{array}{r} 0010 \\ + 1101 \\ \hline 1111 \end{array}$$

$$EA \leftarrow \begin{array}{r} 1111 \\ - 1111 \\ \hline 0000 \end{array}$$

$$\begin{array}{r}
 \text{AS} \\
 + \\
 1 \\
 1111 \\
 - \\
 15
 \end{array}$$

Ex-OR gate

| A | B | A \oplus B |
|---|---|--------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Addition

Subtraction of (+210)

AS \oplus B is A $- B$ AS \oplus BS

$$\begin{array}{r}
 -2 \\
 (-) -13 \\
 \hline
 +11
 \end{array}
 \quad
 \begin{array}{r}
 \text{AS} \\
 + \\
 1 \\
 1101 \\
 \hline
 B \\
 1101
 \end{array}
 \quad
 \begin{array}{r}
 \text{BS} \\
 + \\
 B \\
 \hline
 1101
 \end{array}$$

$$EA \leftarrow A + B + 1$$

$$B \leftarrow 1101 - 1101$$

$$B' \leftarrow 0010$$

$$B' + 1 \leftarrow 0011$$

$$A + B' + 1 \xrightarrow{\text{LSD}} 00101001 \quad \text{RESULT } 23 \times 19$$

$$\begin{array}{r} 0010 \\ 0101 \\ \hline 0101 \end{array}$$

$$EA \leftarrow A + B' + 1 \quad \text{SHR } EA = A$$

$$E = 0 \quad \text{Result } \leftarrow EA$$

$$A = 0101 \quad \text{LSD } \leftarrow 1 + 0$$

$$A' = 1010 \quad \text{LSD } \leftarrow 1 + 0$$

$$A' + 1 = 1011$$

| AS | A |
|-----|------|
| 0 | 1011 |
| + 1 | 11 |

Fixed Point in Multiplication

$23 \rightarrow 10111$

SHR \rightarrow SHIFT RIGHT

$19 \rightarrow 10011$

SC \rightarrow Sequence Counter.

| E | A | Q | SC |
|---|-------|-------|----|
| 0 | 00000 | 10011 | 5 |
| 0 | 11110 | 10011 | 4 |
| 0 | 00000 | 10011 | 3 |
| 0 | 10111 | 10011 | 2 |
| 0 | 00010 | 10011 | 1 |
| 0 | 11110 | 01100 | 0 |
| 0 | 01000 | 01010 | 0 |
| 0 | 00100 | 01011 | 0 |
| 0 | 01011 | 01011 | 0 |
| 0 | 11011 | 01011 | 0 |
| 0 | 01011 | 10101 | 0 |

$$\frac{23 \times 19}{487}$$

$$\text{RESULT } 0110110101 \Rightarrow 437$$

FIXED POINT DIVISION

dividend \downarrow 198 (15 → quotient)

Division $\frac{13}{68}$ $\frac{65}{3}$ → Remainder

$A = 448 \rightarrow \underline{\underline{0111000000}}$

$B = 17 \rightarrow 10001$

$B' = 01110 + 1 \rightarrow 01111$

$$Q_5 \leftarrow A_5 \oplus B_5$$

$$0 \oplus 0$$

$$Q_5 \leftarrow 0$$

Division

$$E \quad A$$

$$0 \quad 01110$$

$$Q$$

$$00000$$

$$\text{Add } B' + 1 \rightarrow \underline{\underline{01111}} \\ \underline{\underline{0}} \quad \underline{\underline{11101}}$$

$$E.A \leftarrow A + B$$

$$\begin{array}{r} 10001 \\ \times 01110 \\ \hline 01110 \end{array}$$

$$00000$$

$$\text{SHL EAQ}$$

$$\begin{array}{r} 01111 \\ \times 01011 \\ \hline 01011 \end{array}$$

$$\begin{array}{r} 00000 \\ \downarrow \text{extra} \\ 00001 \end{array}$$

$$\text{Add } A + B' + 1$$

$$11001$$

$$4$$

$$Q_n \leftarrow 1$$

$$11001$$

$$00010$$

$$\text{SHL EAQ}$$

$$11001$$

$$00011$$

$$\text{Add } A + B' + 1$$

$$11001$$

$$00000 \rightarrow A_3$$

$$Q_n \leftarrow 1$$

$$11001$$

$$00110$$

$$\text{SHL EAQ}$$

$$11001$$

$$00110$$

$$\text{Add } A + B' + 1$$

$$11001$$

$$00110$$

$$E \leftarrow A + B$$

$$11001$$

$$00110$$

$$\text{SHL EAQ}$$

$$11001$$

$$01100$$

$$\text{Add } A + B' + 1$$

$$11001$$

$$01101$$

$$Q_n \leftarrow 1$$

$$11001$$

$$01101$$

FLOATING POINT

Addition / Subtraction

1. Checking for zero's

2. Align mantissas

3. Add mantissa

4. Normalize the result.

Example 1:- $0.1101 e^{\frac{0110}{b}}$

$0.1001 e^{\frac{0011}{a}}$

$0.01001 e^4$ a:b

$0.001001 e^5$ 3:b

$0.0001001 e^6$ 4:b

$0.00001001 e^7$ 5:b

$0.1101 e^6$ 6:b

$0.00001001 e^6$ 6:b

As $A + B = 0.0001001$

$0 + 0 = 0.1101$

$\frac{0}{+} \quad 0.1110001$

0 0.1110001

+VE

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