Digital IC Design

EE5311

Implementing 8×8 unsigned multiplier using the Dadda tree

Group: 17

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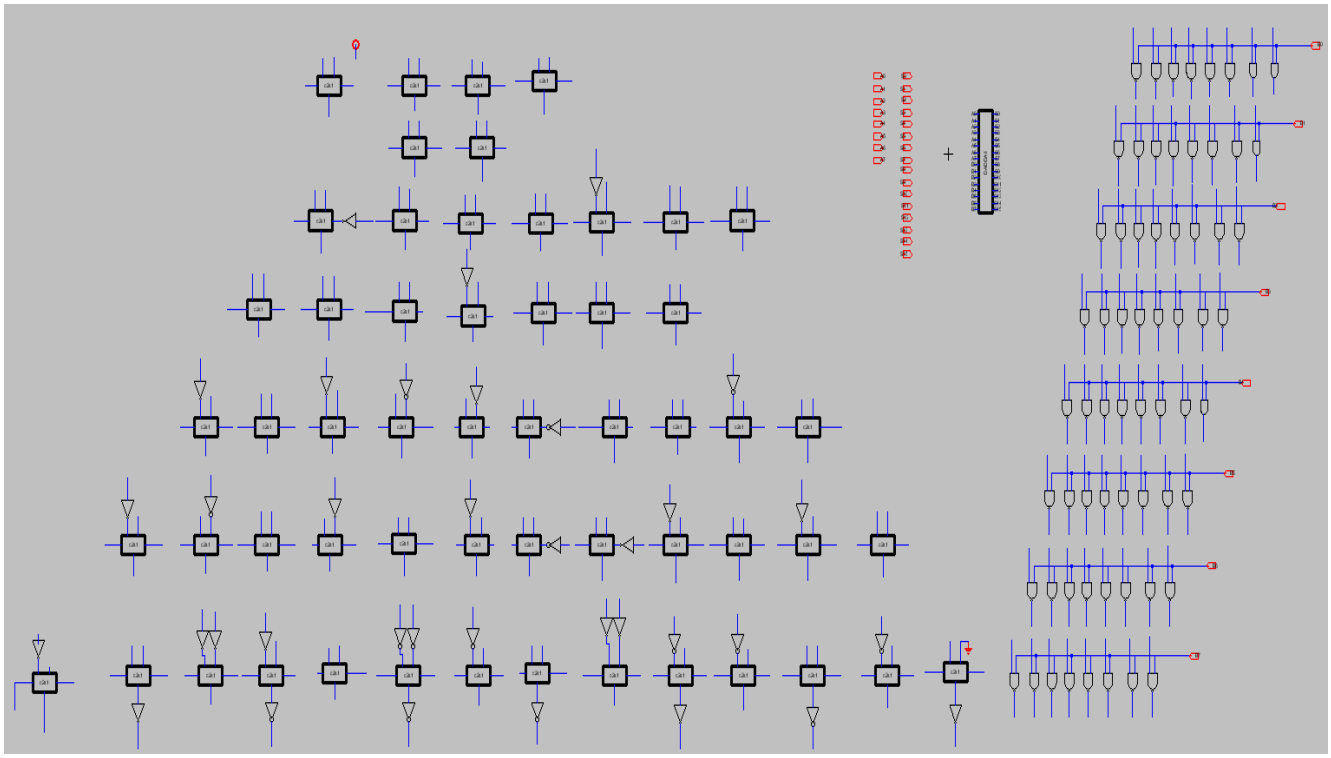
DEPARTMENT: ELECTRICAL ENGINEERING

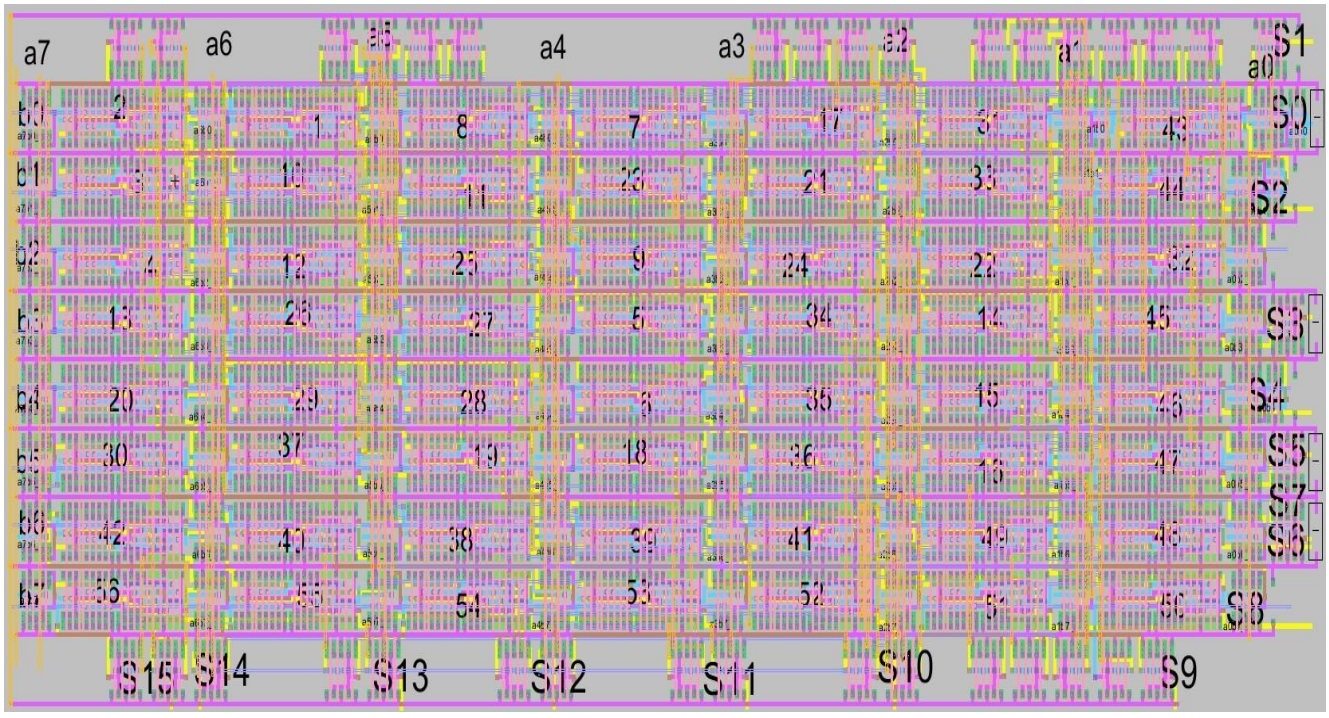
PROGRAM: INTEGRATED CIRCUITS AND SYSTEM

I. Implementation using Ripple carry in vector Merge stage

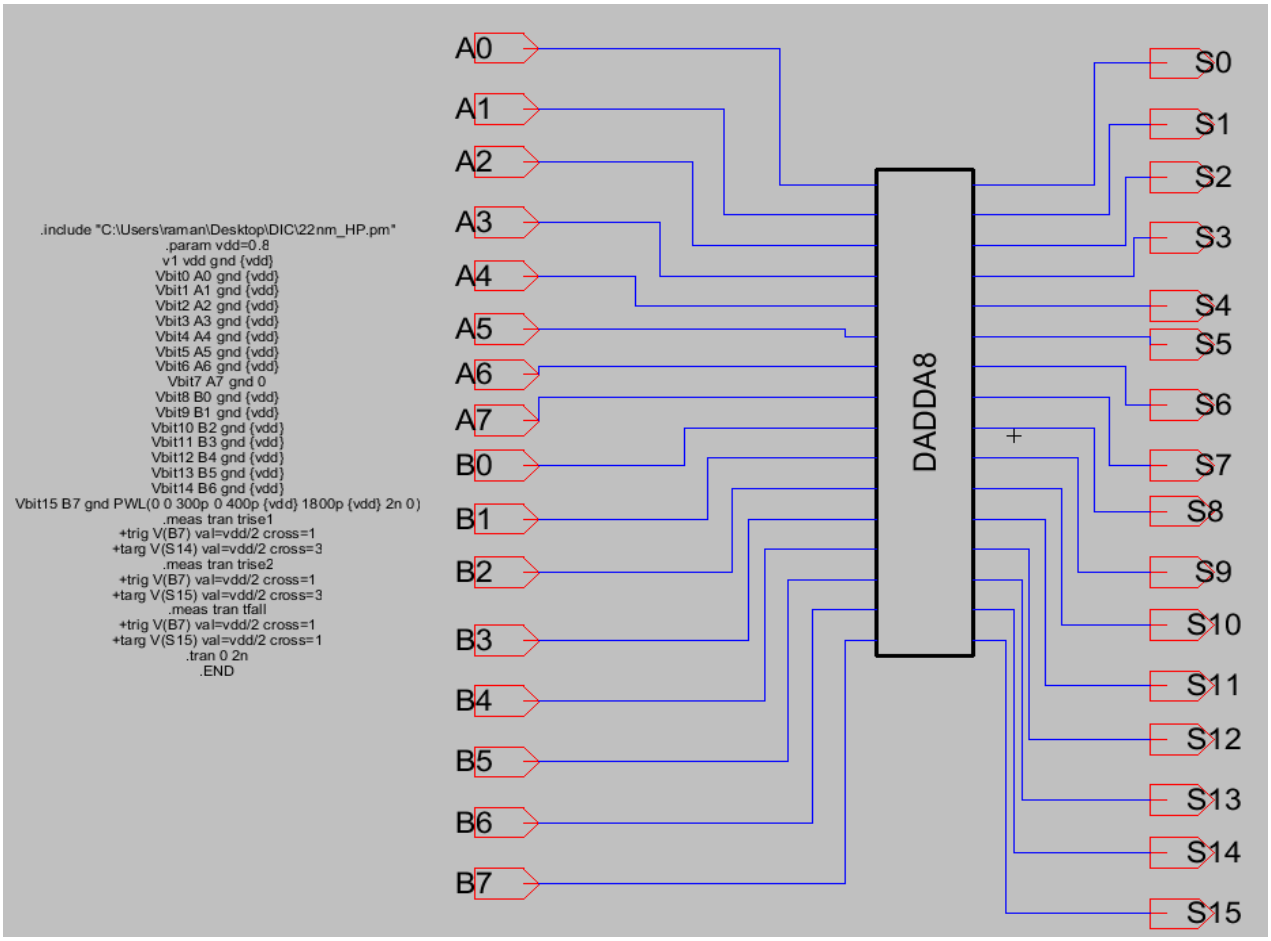
Schematic:



Layout:



Test Bench:



DRC:

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 231 networks
0 errors and 0 warnings found (took 0.047 secs)
```

LVS:

```
Hierarchical NCC every cell in the design: cell 'DADDA8{sch}'  cell 'DADDA8{lay}'
Comparing: DADDA8:Inverter8X{sch} with: DADDA8:Inverter8X{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: DADDA8:and4{sch} with: DADDA8:and4{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: DADDA8:c2s1{sch} with: DADDA8:c2s1{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: DADDA8:nand4{sch} with: DADDA8:nand4{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: DADDA8:DADDA8{sch} with: DADDA8:DADDA8{lay}
  exports match, topologies match, sizes not checked in 0.015 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.031 seconds.
```

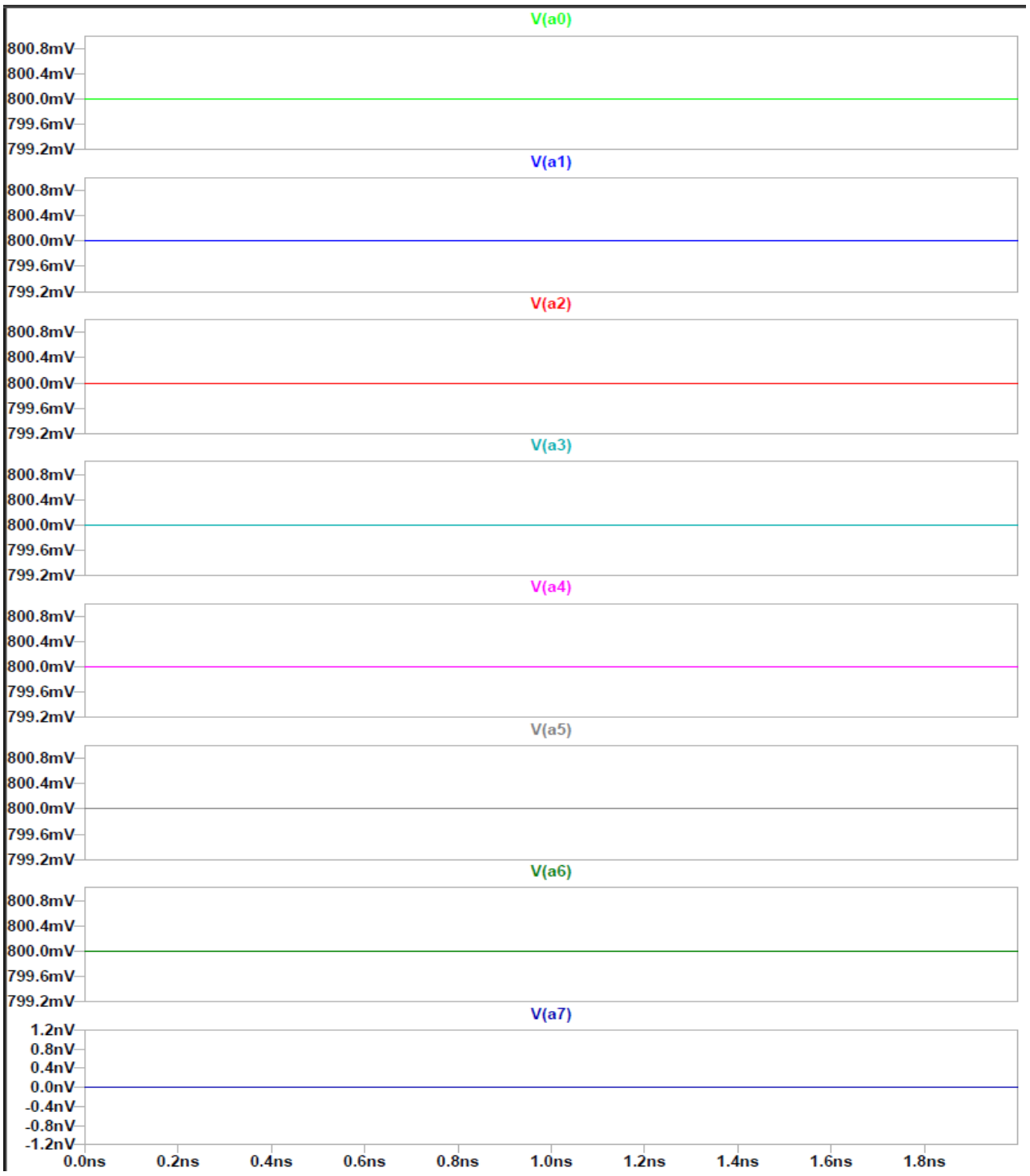
Functionality Test:

Input A: 01111111 (127)

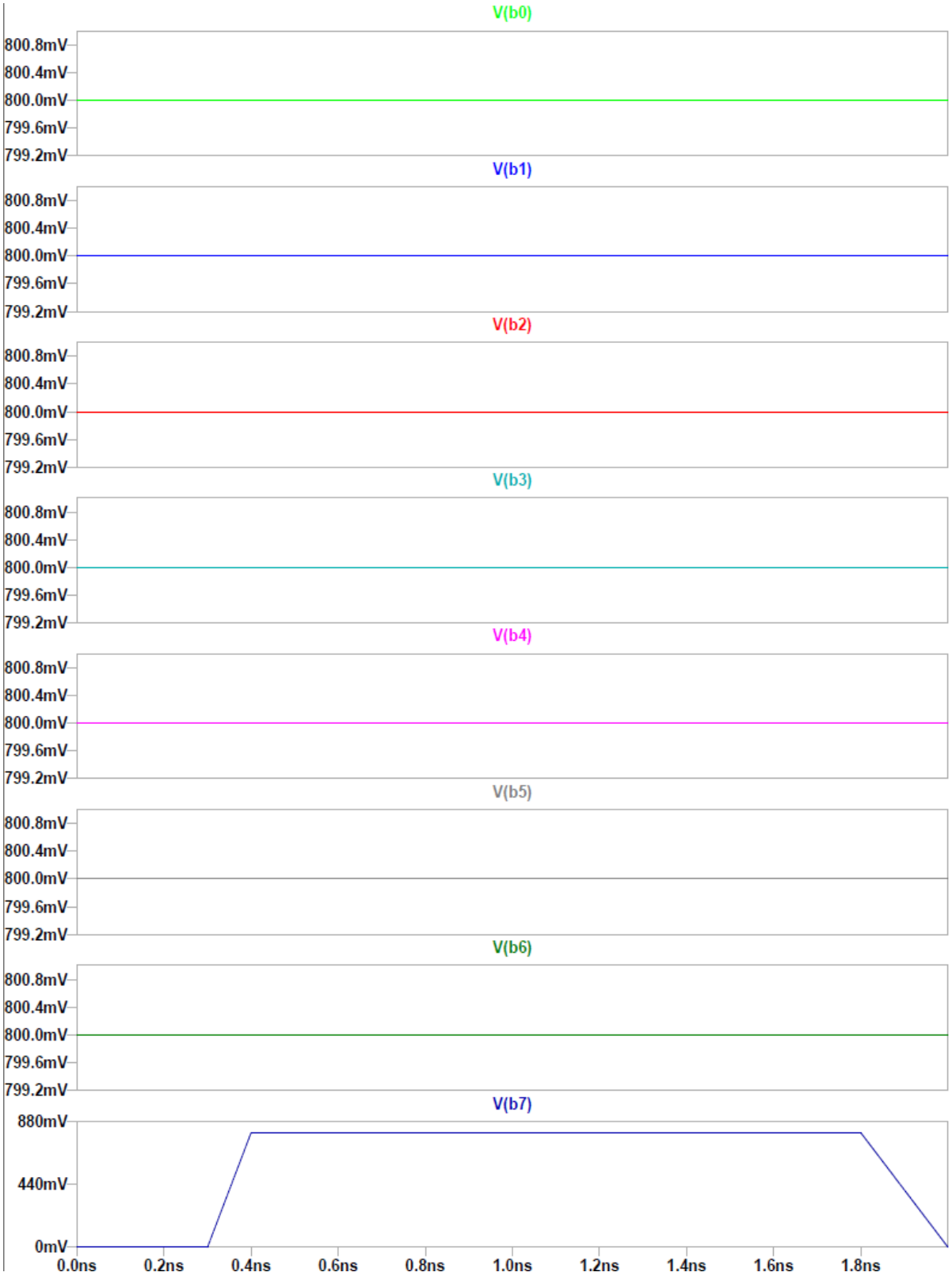
Input B: 11111111 (255)

Output: 0111111010000001 (32385)

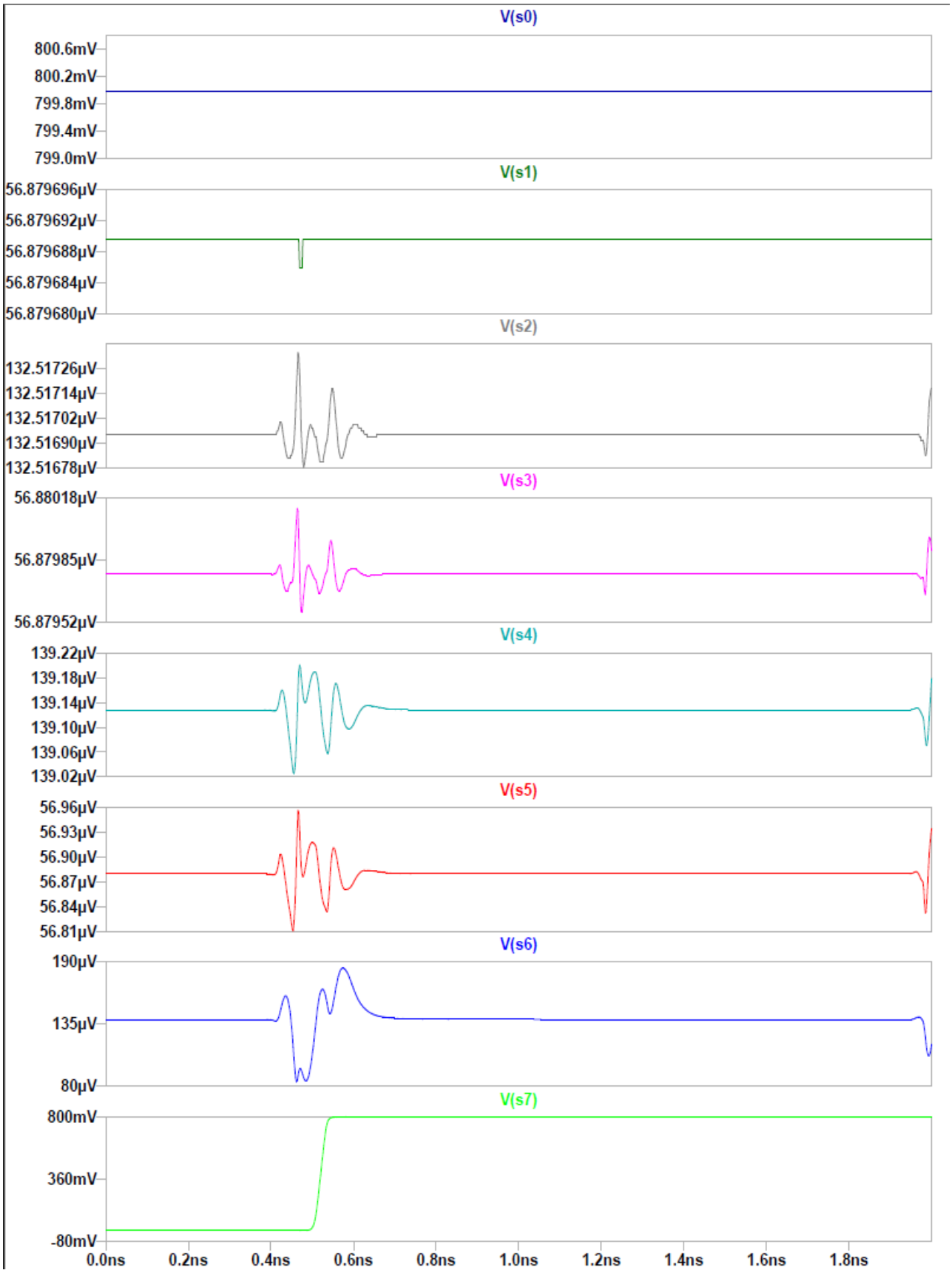
I/P waveform {A}:

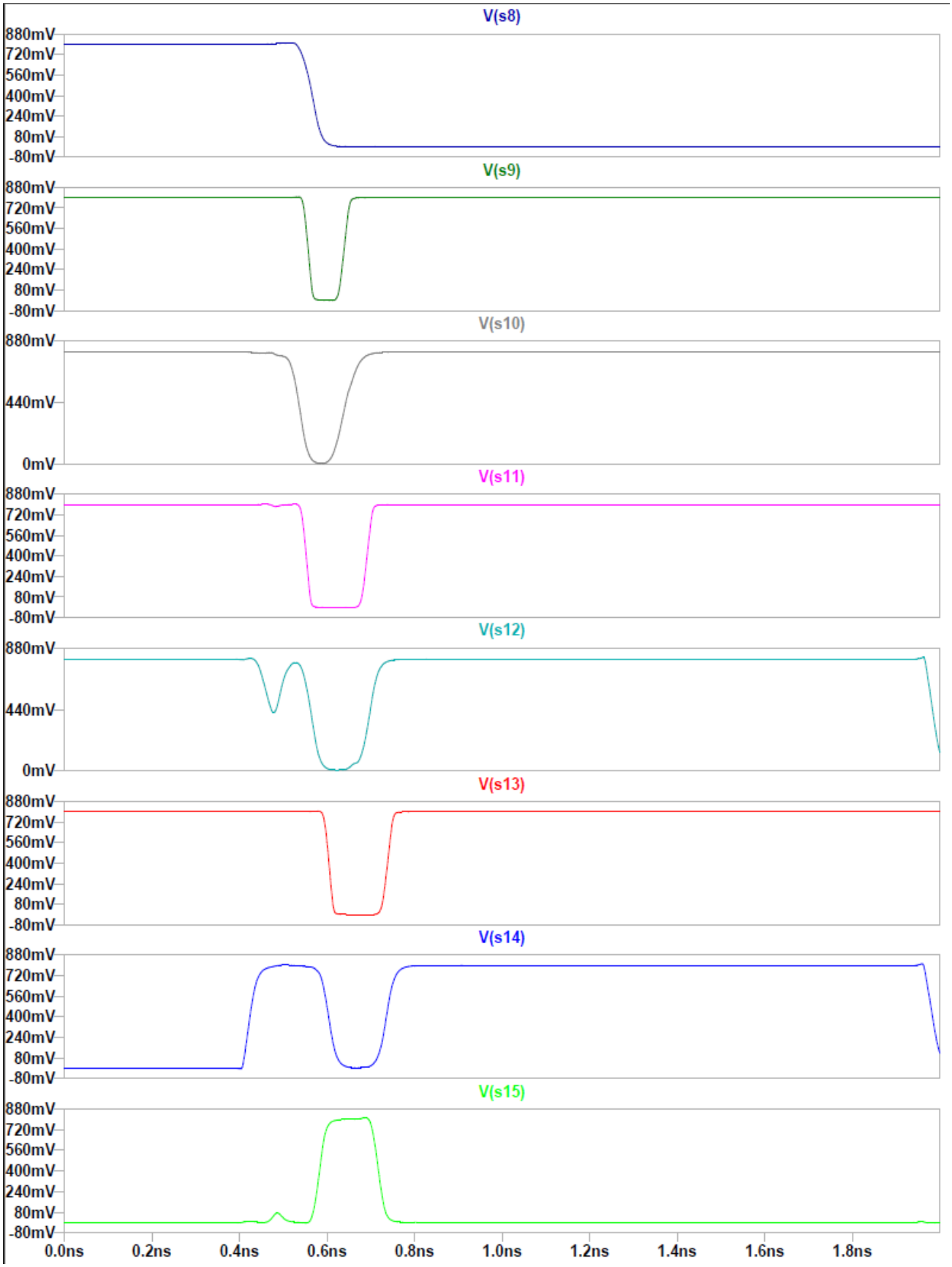


I/P waveform {B}: Used PWL for last bit (b7) to show transitions in output waveforms.

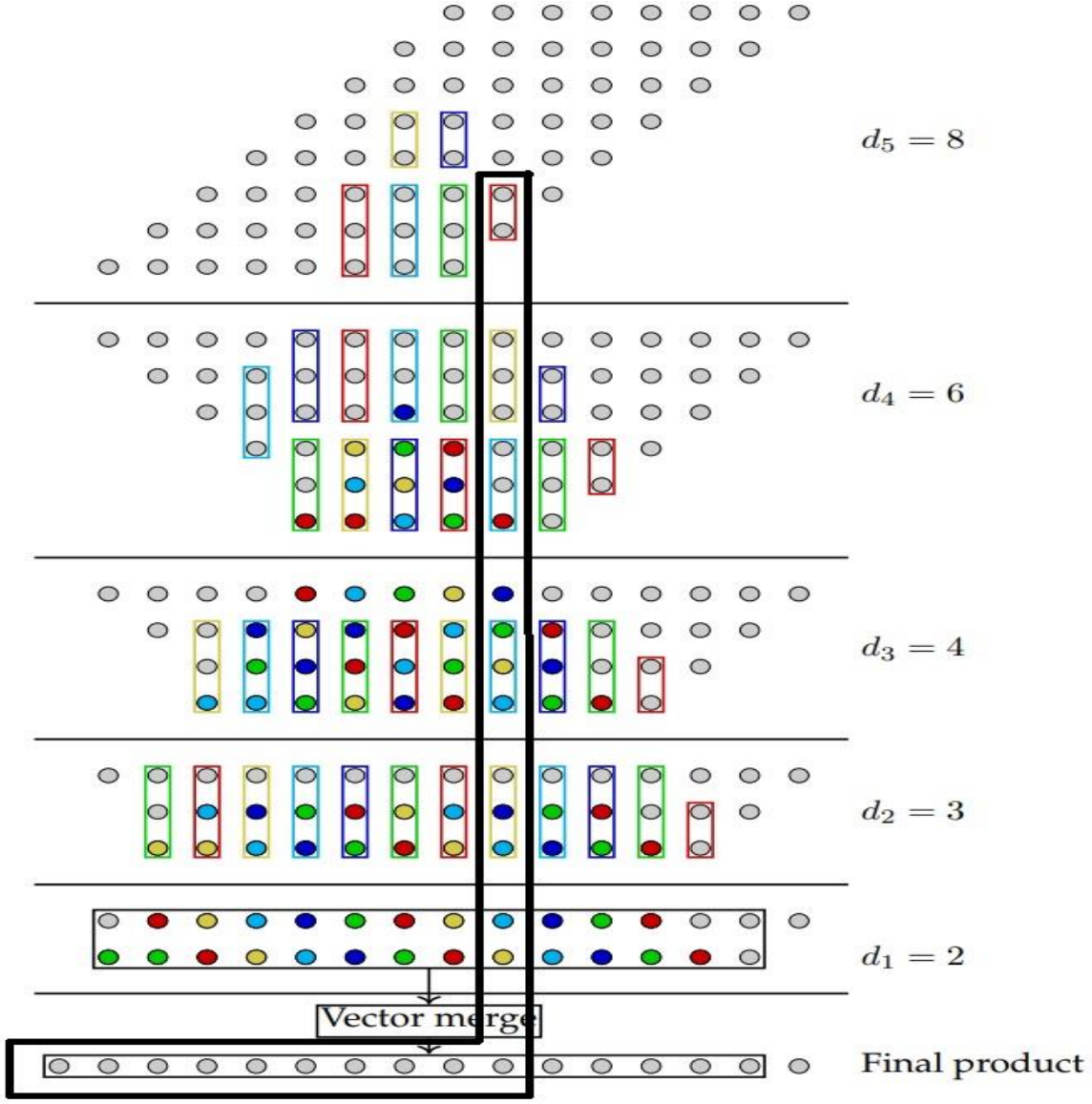


O/P waveform: (MSB) 0111111010000001 (LSB)




V(s8)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s9)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s10)
880mV
440mV
0mV
V(s11)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s12)
880mV
440mV
0mV
V(s13)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s14)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s15)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
0.0ns
0.2ns
0.4ns
0.6ns
0.8ns
1.0ns
1.2ns
1.4ns
1.6ns
1.8ns

Critical Path:



Delay Measurements:

<u>Input combination:</u>

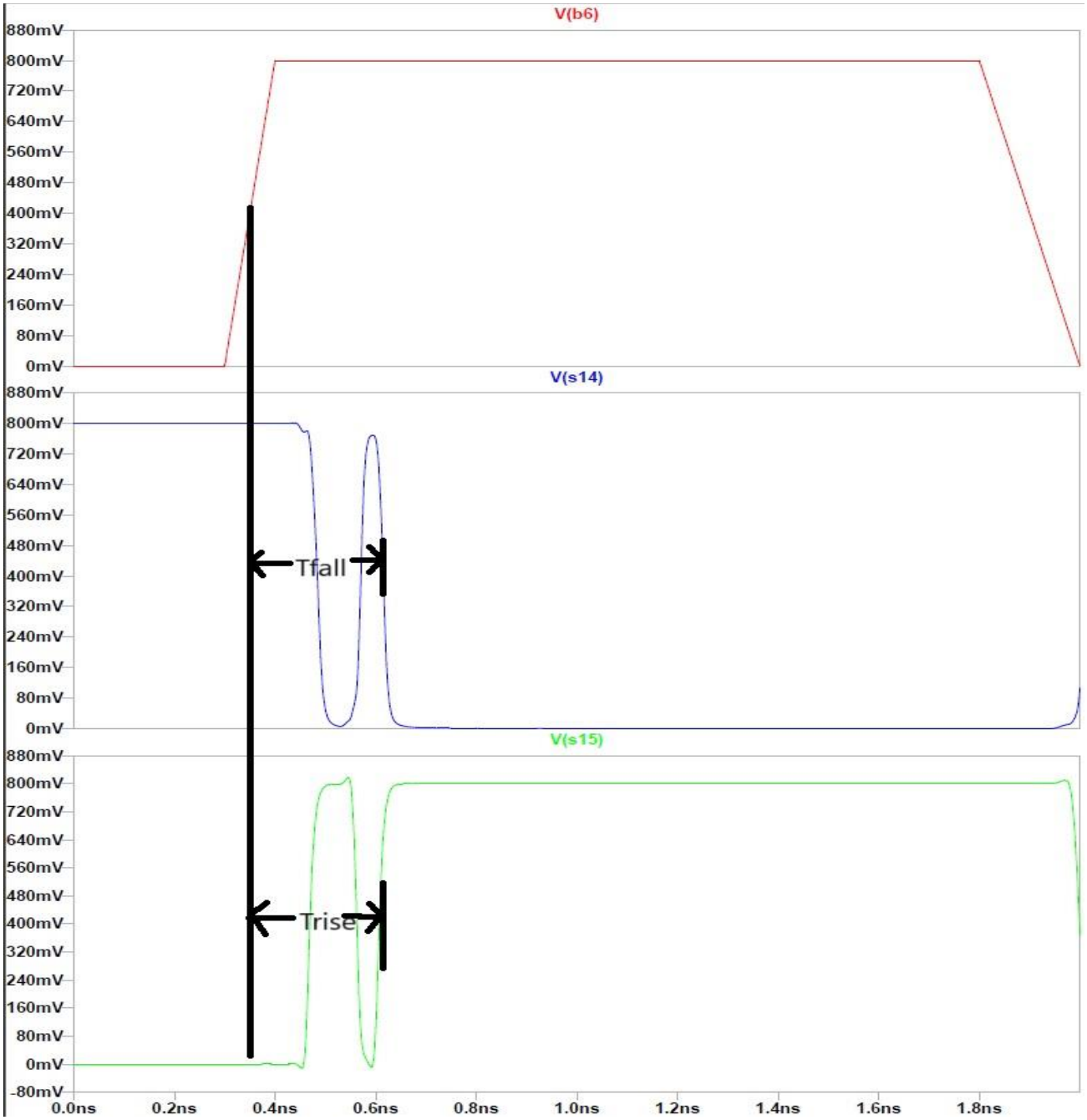
A:10010101(149)

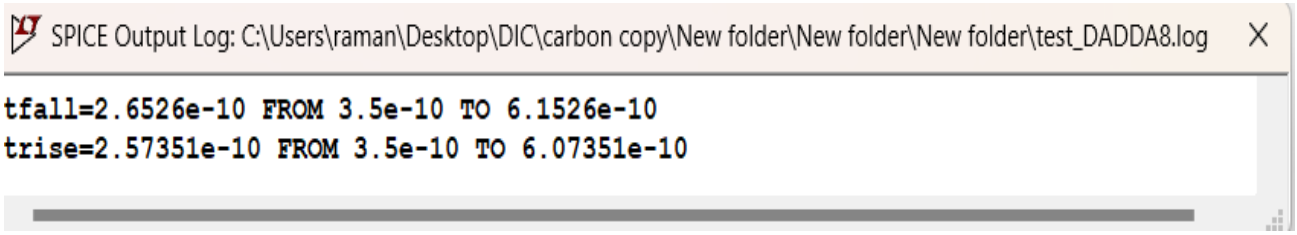
B:10011100(156) → 11011100(220)

Given input 149 to A and 220 to B. Pulse given to b6 bit so that rise delay will be propagation delay between inputs 149 and 220 and output 32780.

- Rise delay measured between b6 bit and S15.
- Fall delay measured between b6 bit and S14.

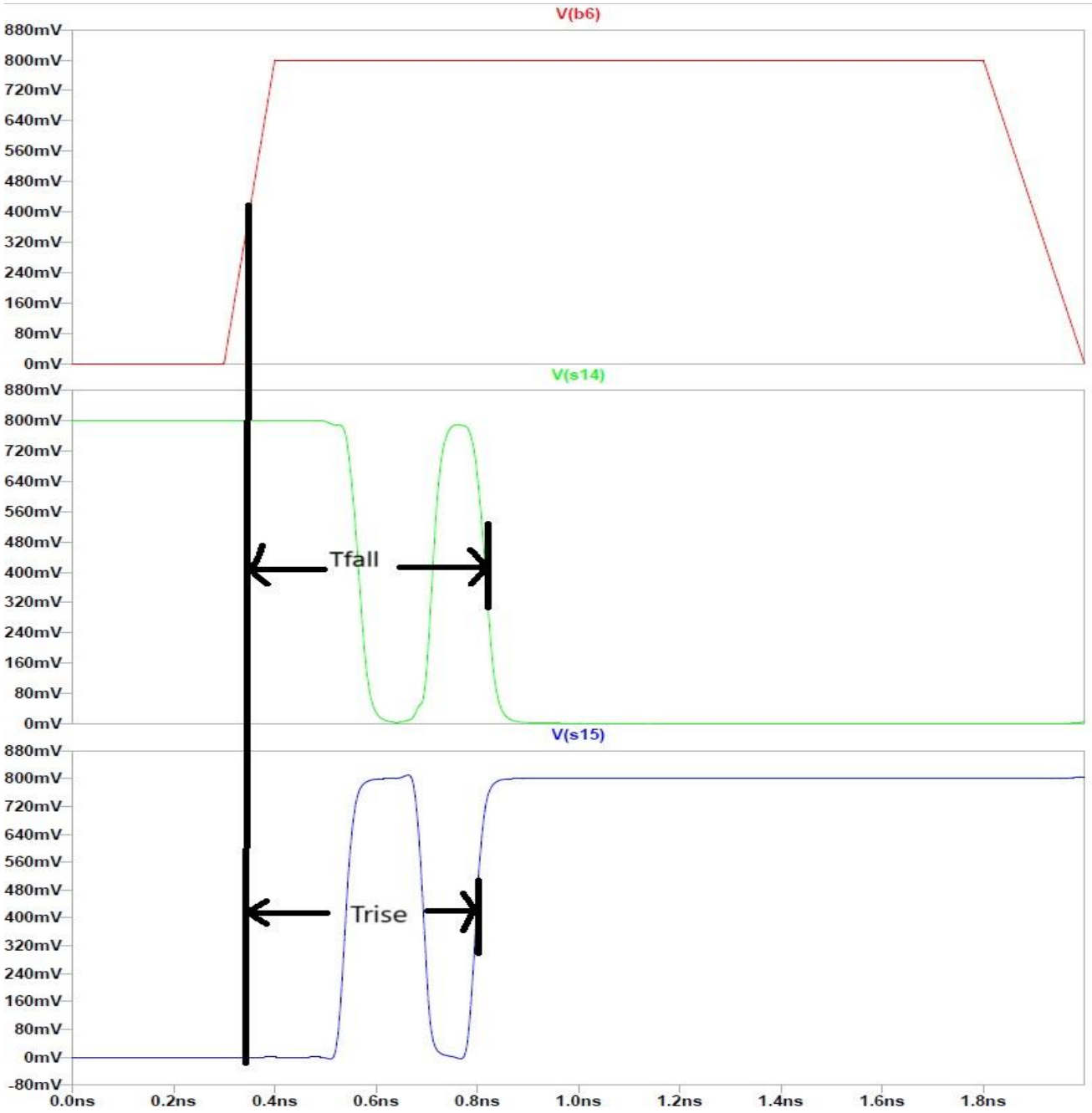
Delay between Input and Output(schematic):





Rise delay(schematic) = 257.3pS

Delay between Input and Output (Layout):



SPICE Output Log: C:\Users\raman\Desktop\DIC\carbon copy\New folder\New folder\New folder\New folder\test_...

```
tfall=4.66531e-10 FROM 3.5e-10 TO 8.16531e-10
trise=4.47909e-10 FROM 3.5e-10 TO 7.97909e-10

Total elapsed time: 581.777 seconds.
```

Rise delay (with RC extraction) = 447.9pS

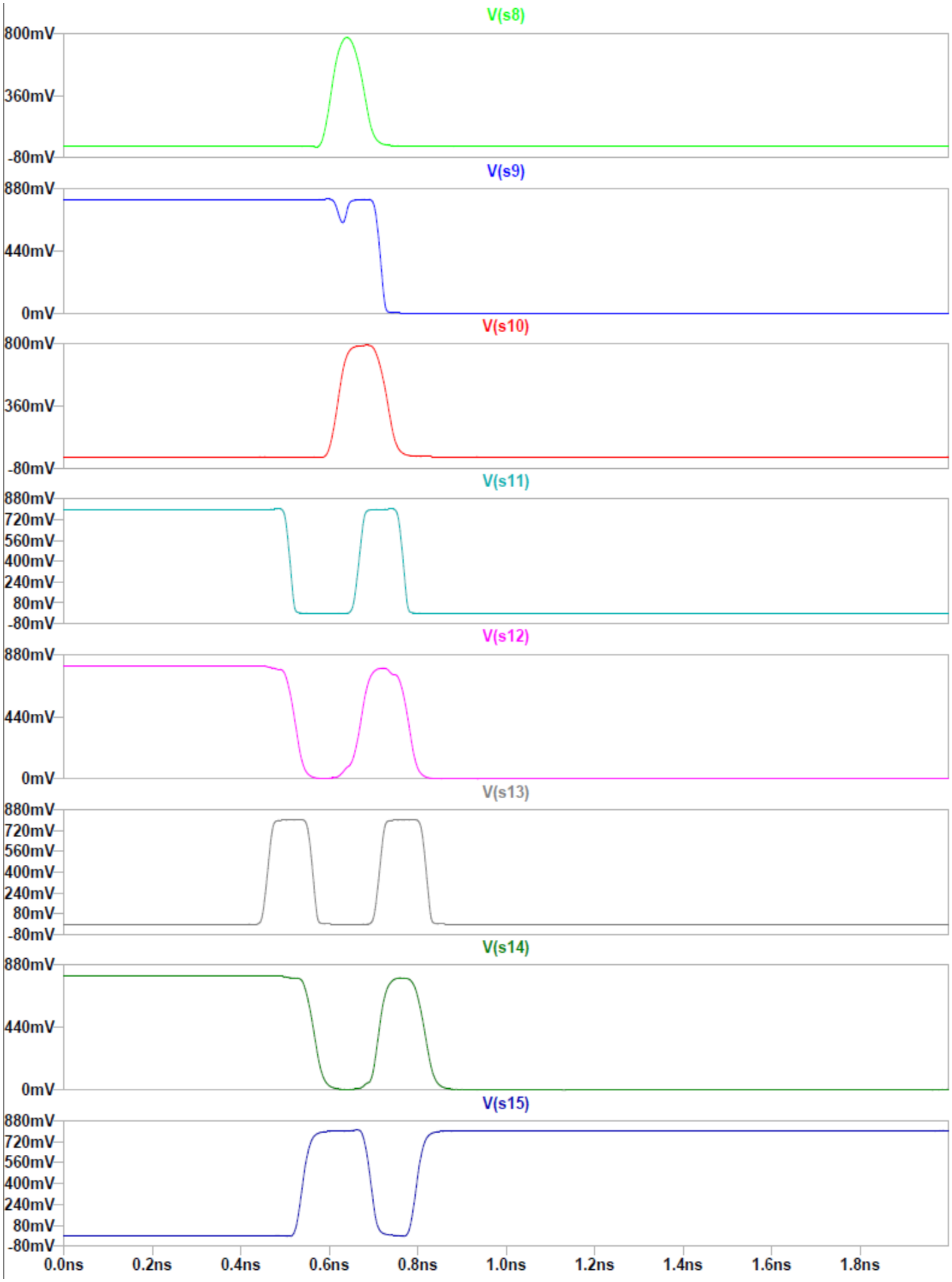
Ratio of layout to schematic rise delay

=447.909ps/257.351ps =1.74

Input A: 10010101(149)

Input B: 11011100(220)

Output waveforms: 1000000000001100(32780)


V(s8)
800mV
360mV
-80mV
V(s9)
880mV
440mV
0mV
V(s10)
800mV
360mV
-80mV
V(s11)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s12)
880mV
440mV
0mV
V(s13)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
V(s14)
880mV
440mV
0mV
V(s15)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
0.0ns
0.2ns
0.4ns
0.6ns
0.8ns
1.0ns
1.2ns
1.4ns
1.6ns
1.8ns


Thank You