EE6320 RF Integrated Circuits Project: VCO Design

VCO Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output Amplitude (Vpp/2)	freq = 1850 MHz	1.33V	≥ 1.2 V
	freq = 1885 MHz	1.35V	≥ 1.2 V
	freq = 1920 MHz	1.4V	≥ 1.2 V
Phase Noise (1 MHz Offset)	freq = 1850 MHz	-128.56dBc/Hz	≤ -125 dBc/Hz
	freq = 1885 MHz	-125.12dBc/Hz	≤ -125 dBc/Hz
	freq = 1920 MHz	-126.992dBc/Hz	≤ -125 dBc/Hz
Phase Noise (20 MHz Offset)	freq = 1850 MHz	-158.03dBc/Hz	≤ -157 dBc/Hz
	freq = 1885 MHz	-158.83dBc/Hz	≤ -157 dBc/Hz
	freq = 1920 MHz	-160.327dBc/Hz	≤ -157 dBc/Hz
Tuning Range	Total Tuning Range	1.849GHz-1.94GHz=**91Mhz**	≥ 70 MHz
	Nunber of bits in coarse tuning	NA	-
	Voltage range in fine tuning	NA	-
	Average KVCO	75.47MHz/V	70 MHz/V
	% variation in KVCO	7.8%	minimal
Power Consumption (1885 MHz)	VCO average power consumption (excluding bias)	7.618mW (excluding divider)	minimal
	Bias circuit	0.969mW	minimal
	Divider circuit	2.235mW	minimal
Other	Sum of all capacitances (in capacitor bank)	NA	-
	Net inductance used	1 inductor – 4nH split as differential to 2nH	-
	Simulator used	virtuoso	-

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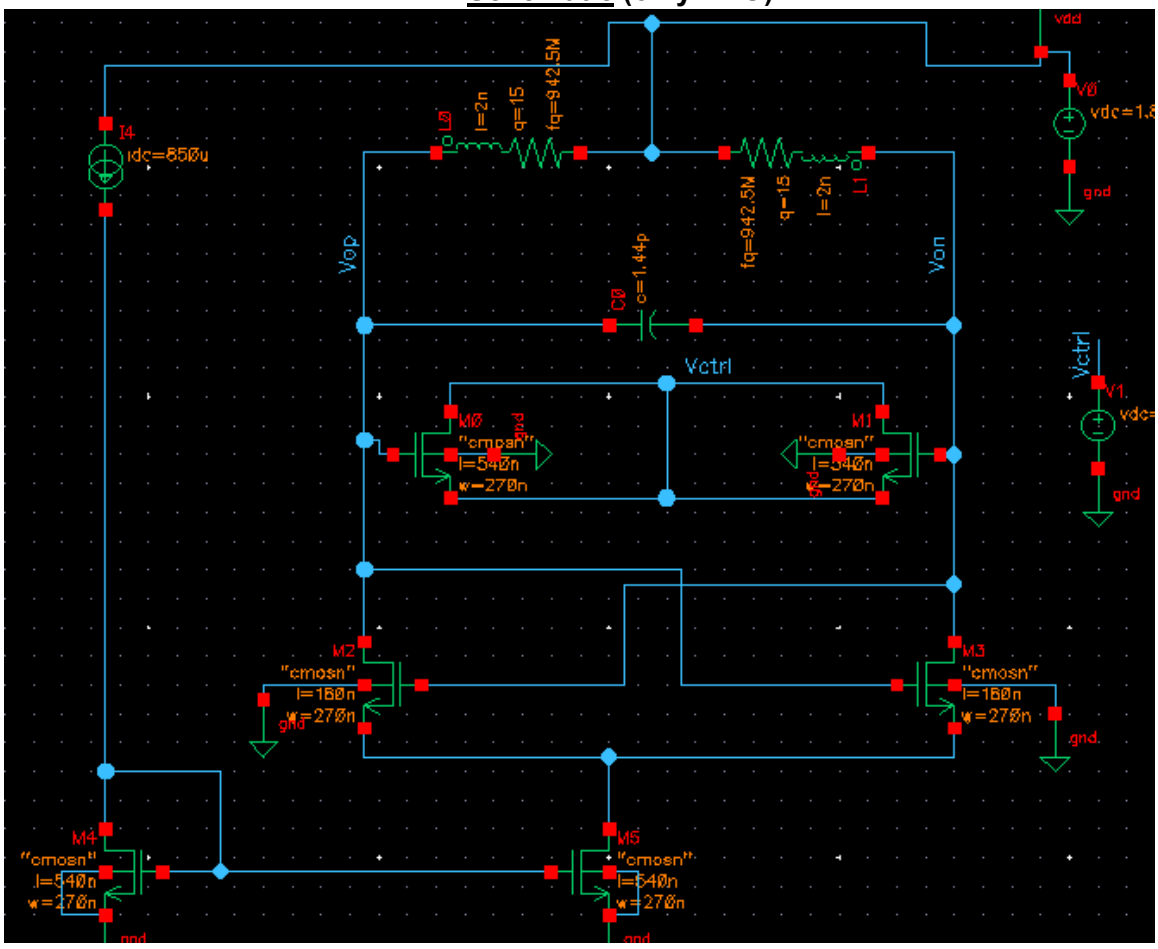
Component Values Table

Component	Value
(W, L) Current Mirror MOS	215x270nm,540nm
(W, L) Tail MOS	875x270nm,540nm
(R, C) Low Pass Noise Cancelling Filter	Na
Tail Capacitance	Na
(L, C) Tail Tank	Na
(W, L) Cross Coupled MOS(s)	15x270nm,180nm
(W, L) Switching MOS(s)	Na
(C1, C2) Capacitor Bank	Na
(W, L) Varactor MOS	550x270nm,540nm
Fix Capacitance	1.44p
(R, L) Drain Tank	2nH
(V bias, I bias)	1.8Vsupply, 850uA

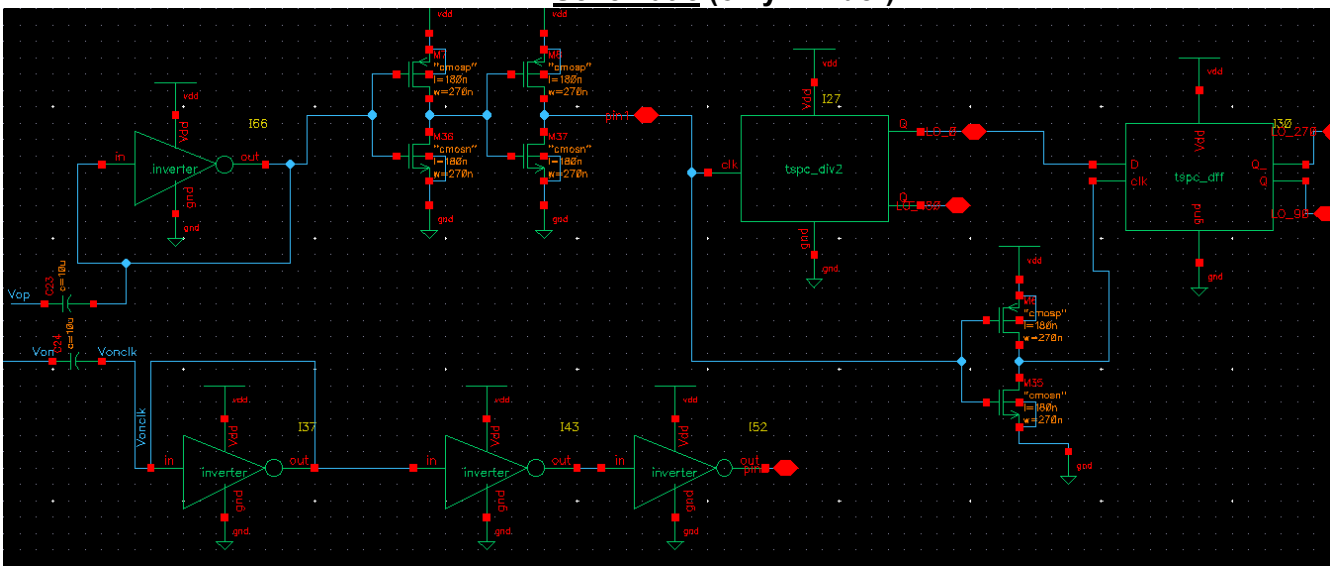
Divide by Two circuit Component values

Component	Value
Back-to-back connected inverters	PMOS W, L = 3x270n,180n NMOS W=270n, L=180n
Buffer stages	PMOS W, L = 15x270n,180n NMOS W=5x270n, L=180n
Clock inverter	PMOS W, L = 15x270n,180n NMOS W=5x270n, L=180n
TSPC logic	Unit sized

Schematic (only VCO)

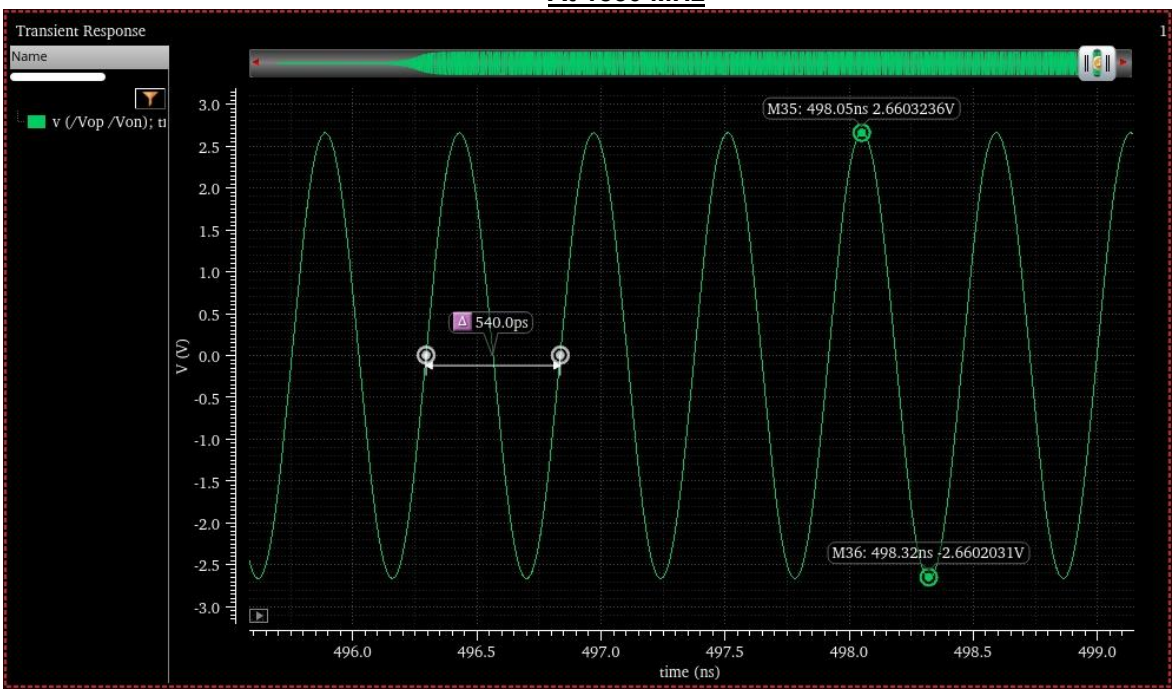


Schematic (only Divider)

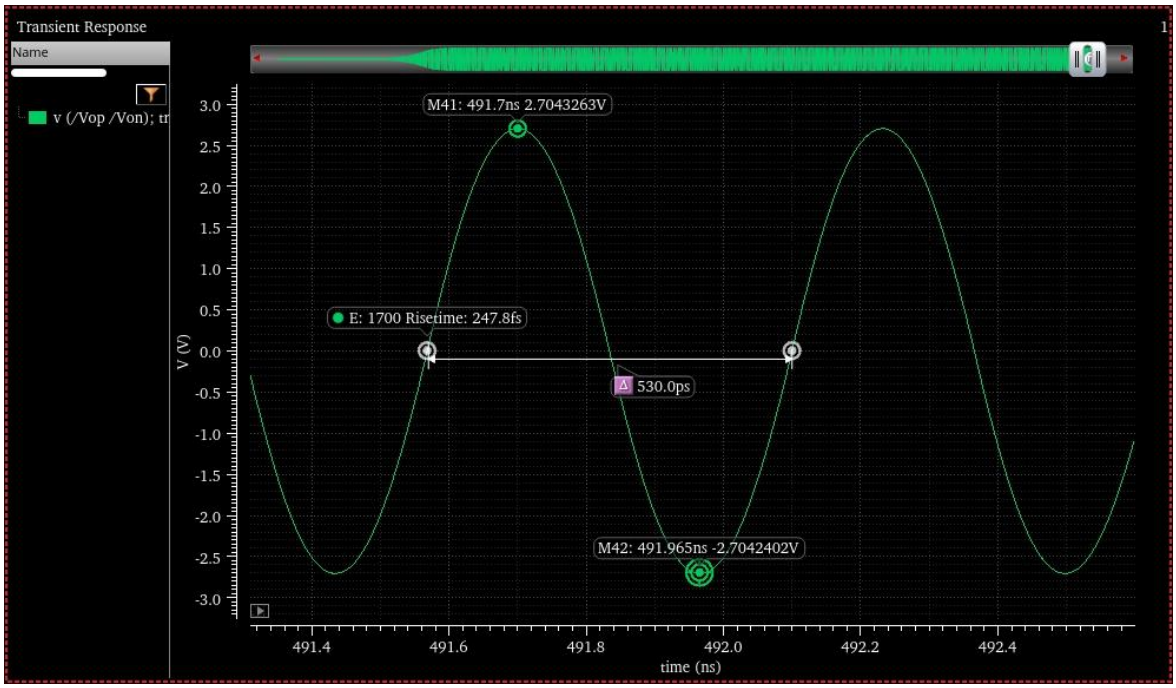


Output Amplitude Plots (unloaded)
(differential settled waveforms)

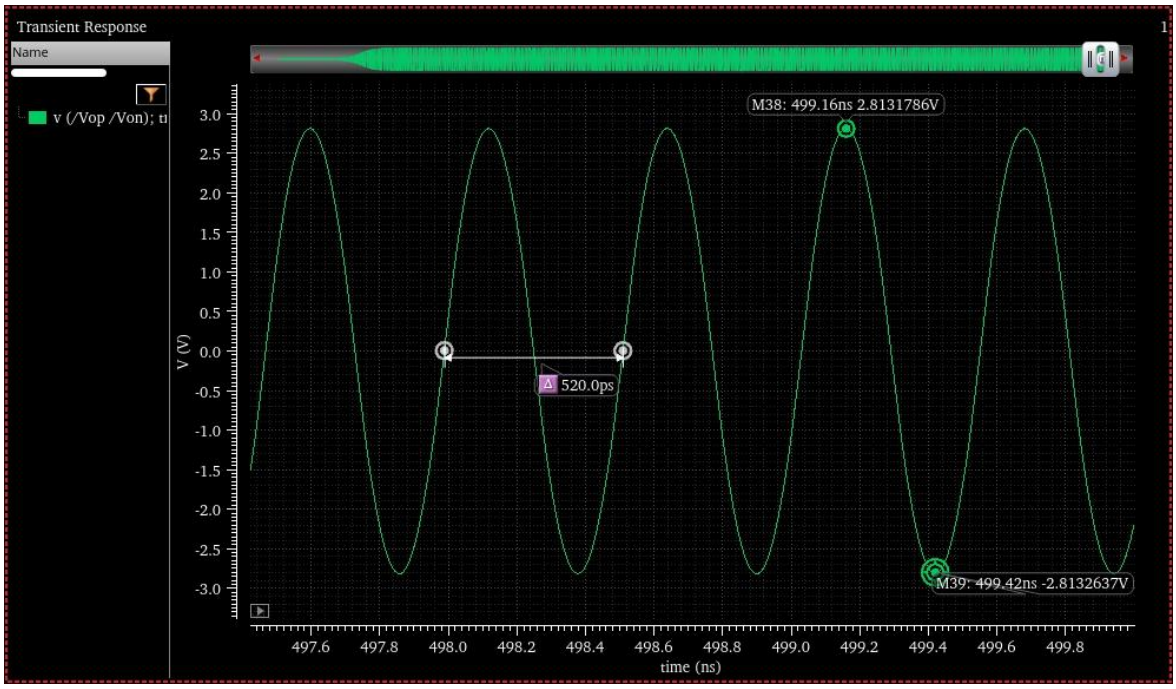
At 1850 MHz



At 1885 MHz

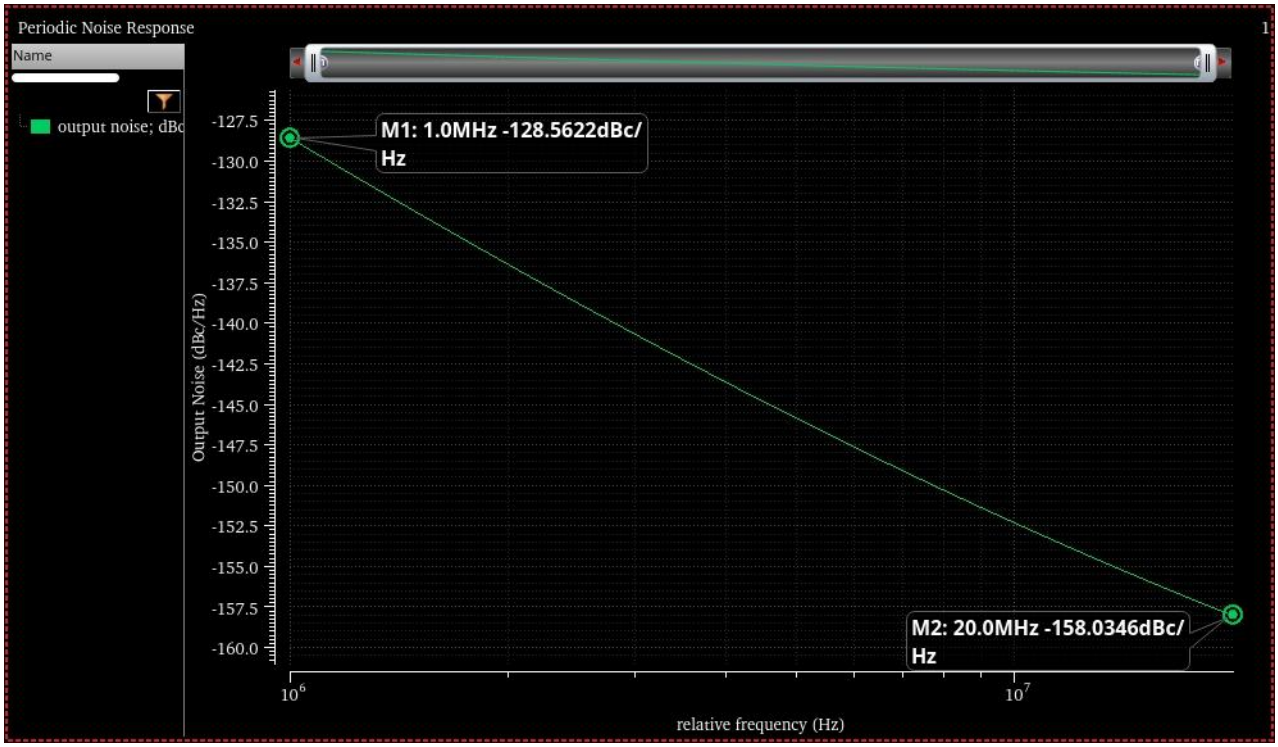


At 1920 MHz

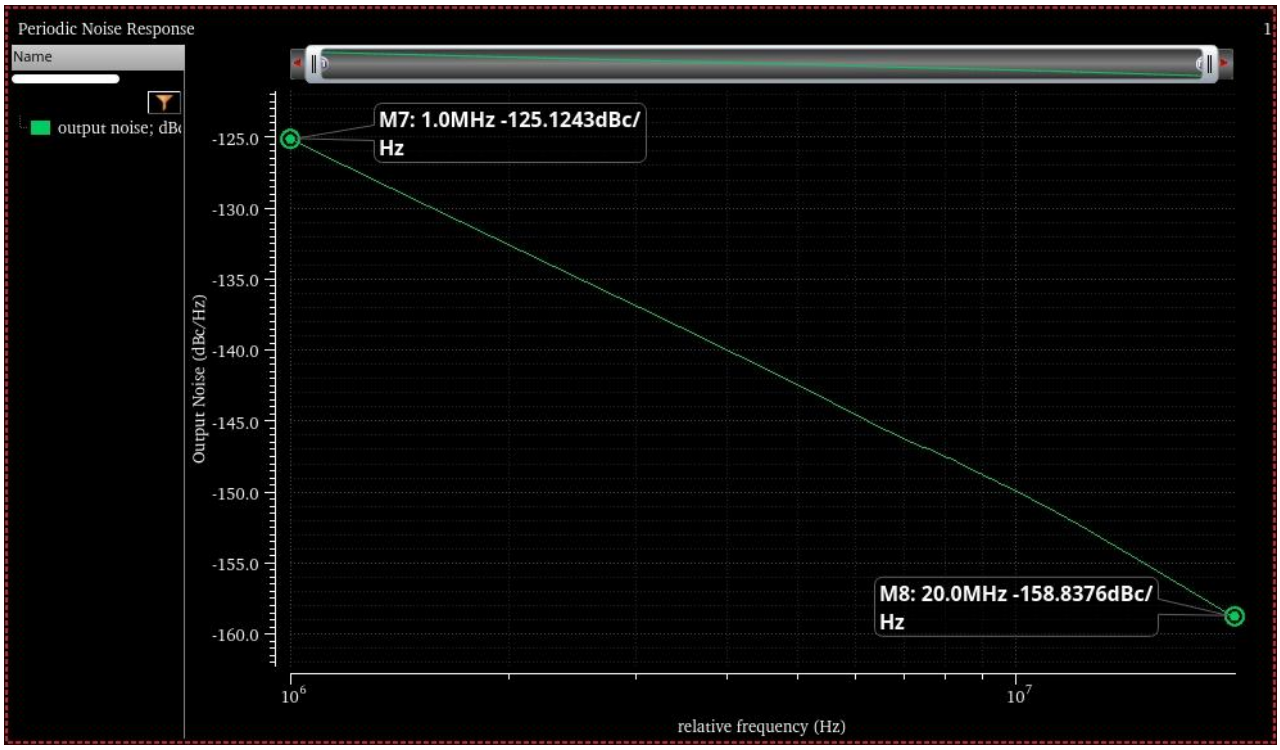


Phase Noise Plots (after loading)
(at 1 MHz and 20 MHz)

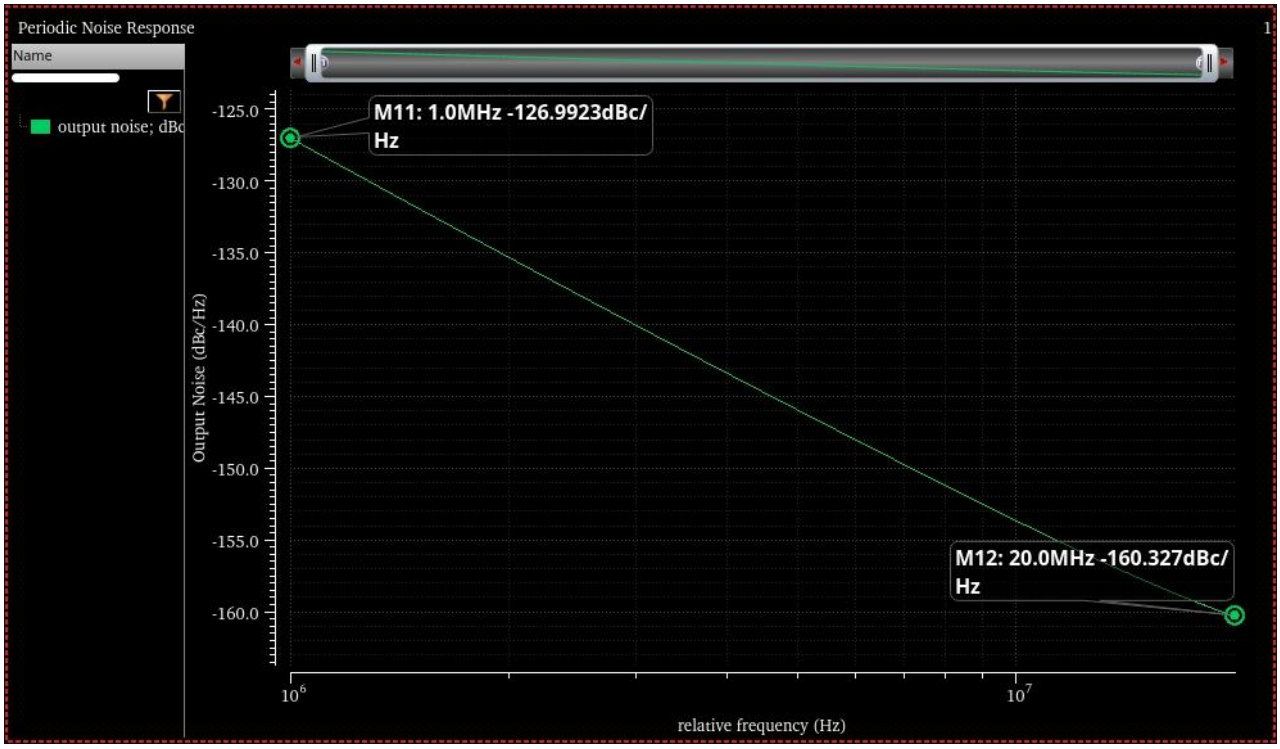
At 1850 MHz



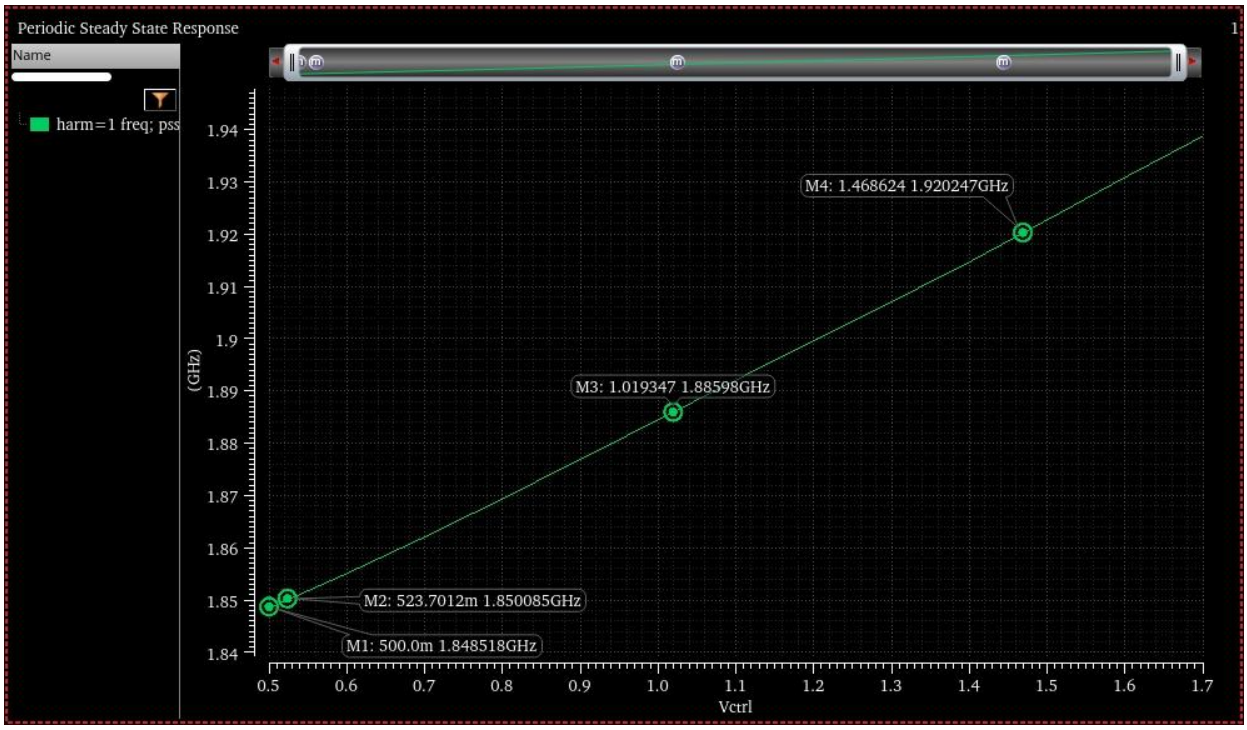
At 1885 MHz



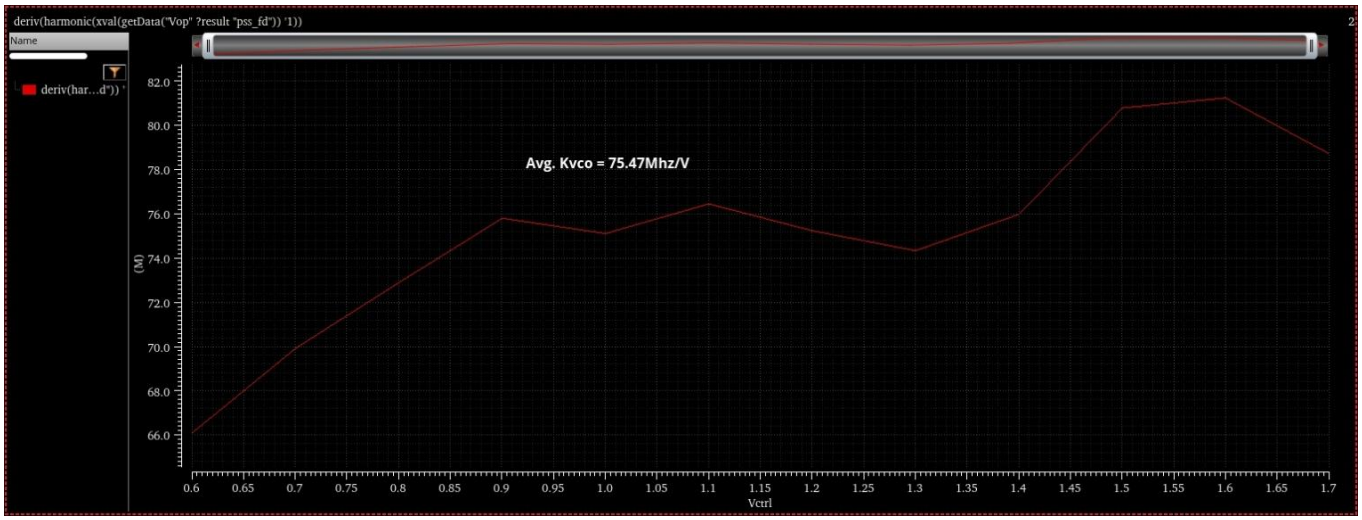
At 1920 MHz



Frequency Tuning Range Plot

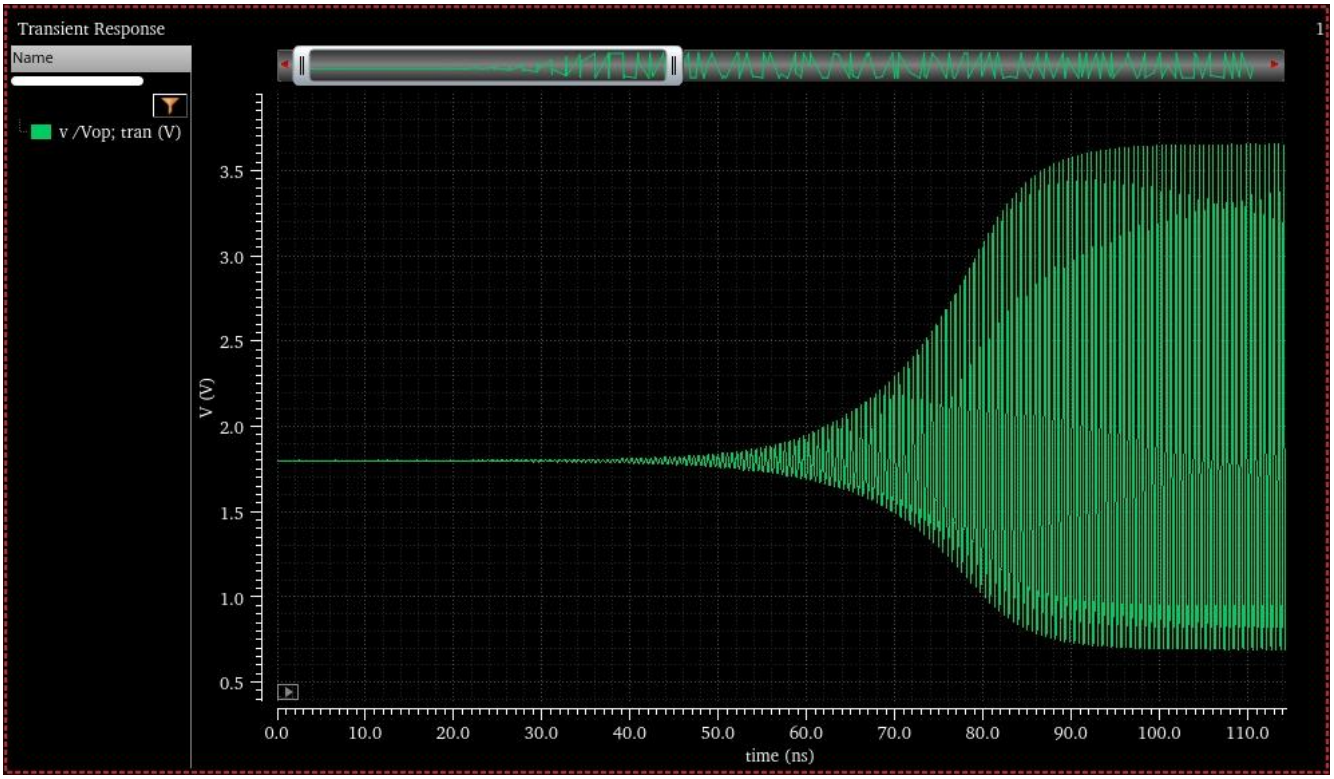


KVCO Plot



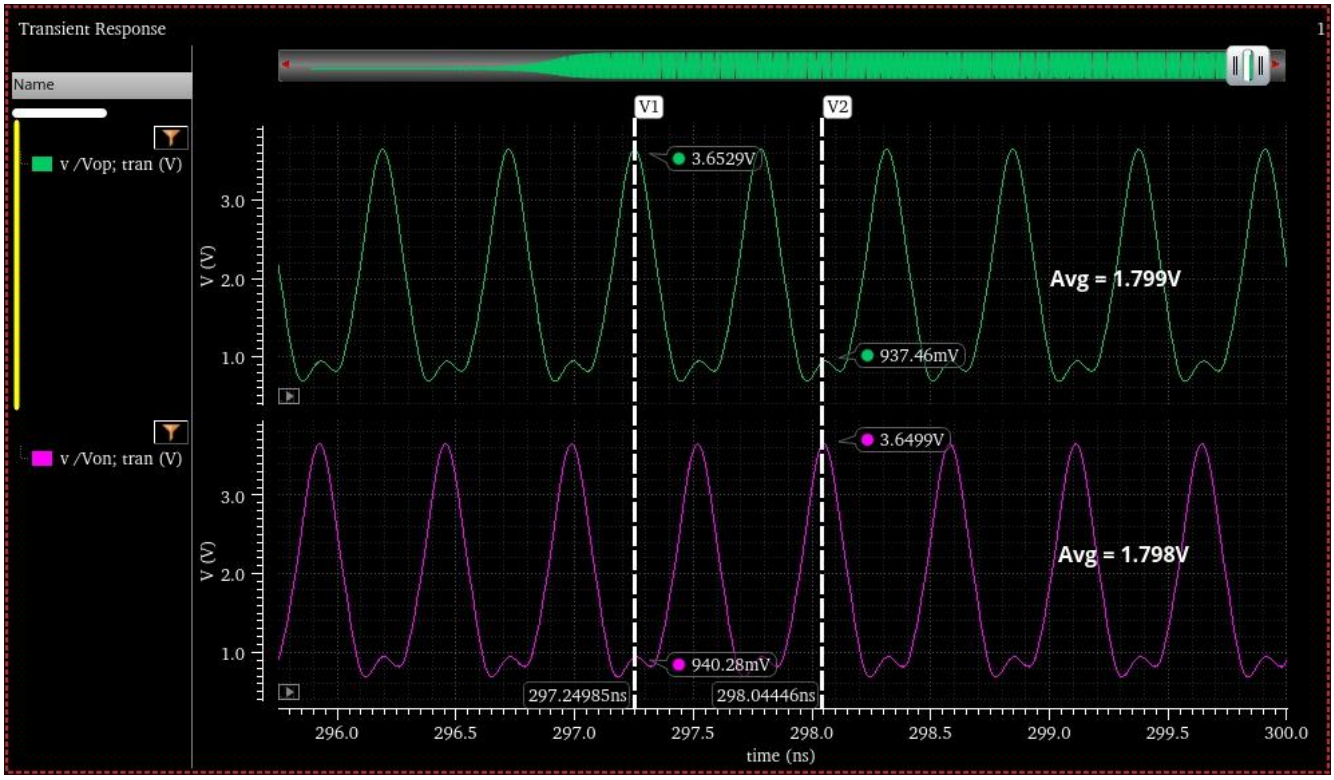
Initial Transient Response Plot (unloaded)

(for Vop at 1885 MHz)

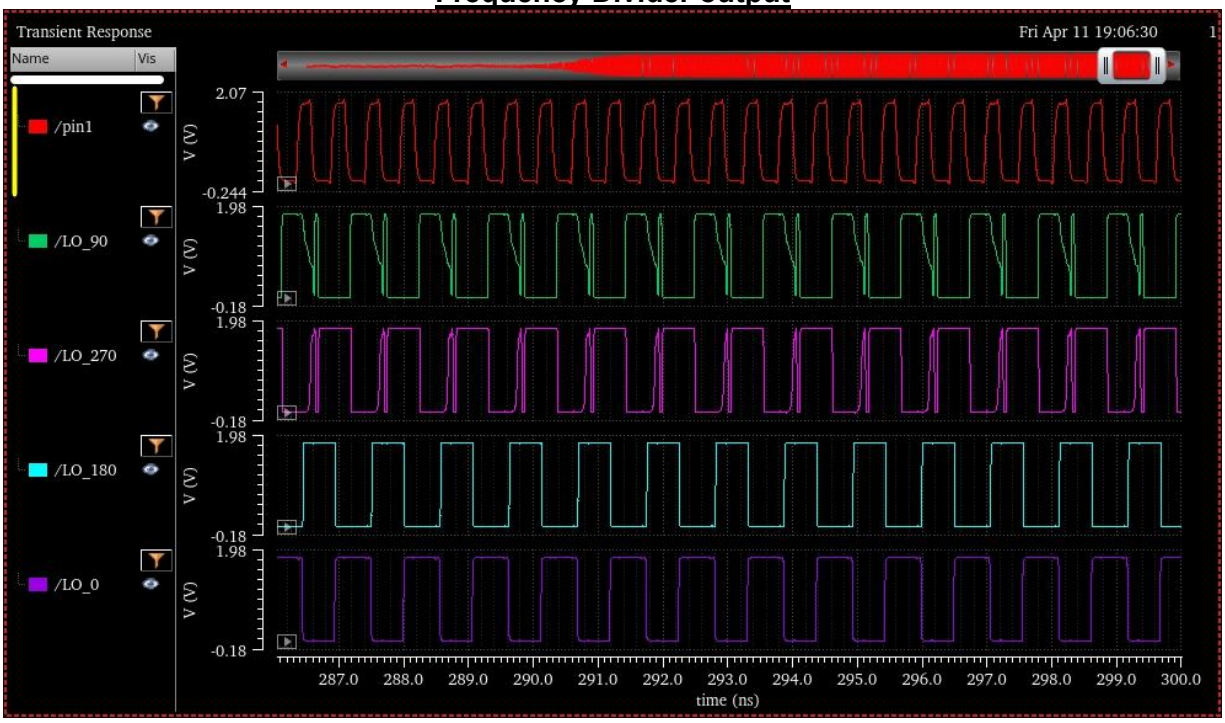


Single Ended Output Plot (Vop & Von)(unloaded)

(at 1885 MHz)



Plots for 0, 90, 180 and 270 degree signals of Frequency Divider output



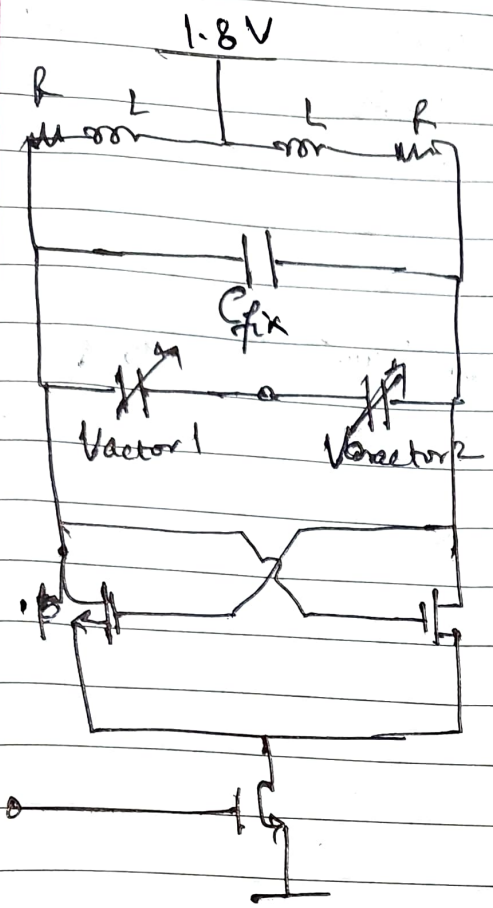
Design Procedure

1. Hand Calculations were performed to find the initial starting point of design
2. Using the hand calculations, the simulation was performed. Specifications were not met.
3. Design was started taking fix capacitor, capacitor bank along with varactor. The varactor size was small therefore required Kvco was not achieved. The varactor size was increased by characterization, and required Kvco was achieved but tuning point was less.
4. Fix capacitor was tweaked to get correct tuning point. Since correct tuning point and Kvco was achieved the Capacitor bank was removed and simplistic design was attained.
5. Divider was designed as per TSPC dynamic logic taught by Prof. Saurabh Saxena in PLL course.
6. Even without LC tail tank the phase Noise spec was met for standalone VCO but not for divider cascade with VCO, additional tweaking in the circuit was done based on the noise summary to get the Phase noise spec correct.
7. The overall design is kept constringent to the Frequency tuning range and Phase Noise in order to minimize Power consumption, every possibility was made to cut down the margins while meeting the specs.
8. More tuning Range and lower Phase noise could have been attained at the cost of Power.

Path to Project Files

/home/ee24m106/cadence_project/RFIC_courseproject/vco_new

VCO Hand Calculations



$$\frac{2}{\pi} I_t R \geq 1.2$$

Now for building oscillation and stabilizing

$g_m R \geq 1$ or 2x, 3x

we take $g_m R = 2$

Now fix $L = 2nH$

$\Rightarrow R = 280.275$

$g_m = 7.12 mS$

$$I_t \text{ req} \geq 1.2 \times \frac{\pi}{2} / 280.27$$

$$I_t \geq 6.72 mA$$

freq. Acquisition :

$$f_{max} = \frac{1}{2\pi\sqrt{L C_{min}}}$$

$$1920 \times 10^6 = \frac{1}{2\pi\sqrt{L \times C_{min}}}$$

$$C_{min} = \frac{1}{(2\pi)^2 (1920 \times 10^6)^2 \times 2 \times 10^{-9}}$$

$$C_{min} = 3.43 pf$$

$$f_{min} = \frac{1}{2\pi\sqrt{L C_{max}}}$$

$$C_{max} = \frac{1}{4\pi^2 (1850\times10^6)^2 \times 2\mu H}$$

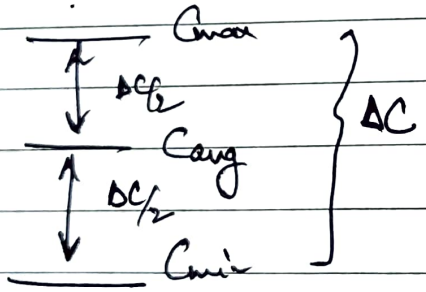
$$C_{max} = 3.7\,pF$$

So we need $\Delta C = C_{max} - C_{min}$

$\Delta C = 270\,f$ To achieve required tuning

To find a justifiable value of $C_{fix} = \left(\frac{C_{max}+C_{min}}{2}\right)/2$

$$C_{fix} = \frac{3.7 + 3.43}{4} \Rightarrow 1.78pf$$



$C_{avg} = 1.78 \times 2$
(Differential)

→ The Varactor is adjusted to give required tuning range.

→ C_{fix} actual came to be 1.44pf as L shows on ESR too!!