EE6320 RF Integrated Circuits Project:
PA Design

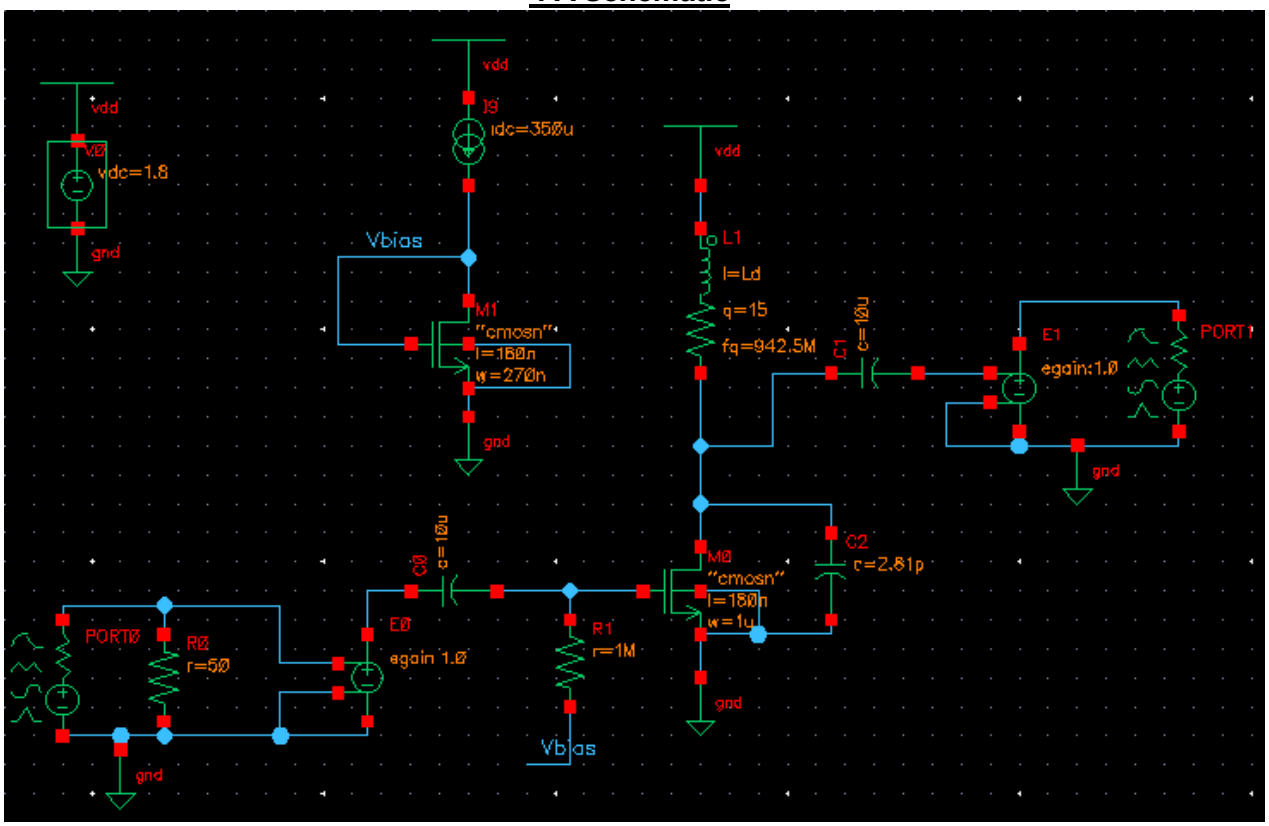
PA Performance Summary Table

Design Parameter	Design Metric	Performance	Specification
Output P1dB	f_o = 925 MHz	13.0668dBm	$\geqslant$ +13 dBm
	f_o = 942.5 MHz	13.319dBm	$\geqslant$ +13 dBm
	f_o = 960 MHz	13 dBm	$\geqslant$ +13 dBm
AM-PM Deviation (at P1dB)	f_o = 925 MHz	1.51 degrees	$\leqslant$ 3 degrees
	f_o = 942.5 MHz	0.3 degrees	$\leqslant$ 3 degrees
	f_o = 960 MHz	1.087 degrees	$\leqslant$ 3 degrees
Voltage Gain (from Gate to Drain)	f_o = 925 MHz	14.32	$\geqslant$ 2
	f_o = 942.5 MHz	14.95	$\geqslant$ 2
	f_o = 960 MHz	14.16	$\geqslant$ 2
Power (at 942.5 MHz)	PA Average Consumption (excluding bias)	7.768mW	Minimize
	Bias Circuit Consumption	0.63mW	Minimize
Other	Sum of all Capacitances (including ac coupling)	20µF + 2.81pF	-
	Inductance Used	10nH	-

	Device Width	1µm	-
	Simulator Used	Cadence Virtuoso	-

Name: RESHUL JINDAL
Roll No: EE24M106

PA Schematic

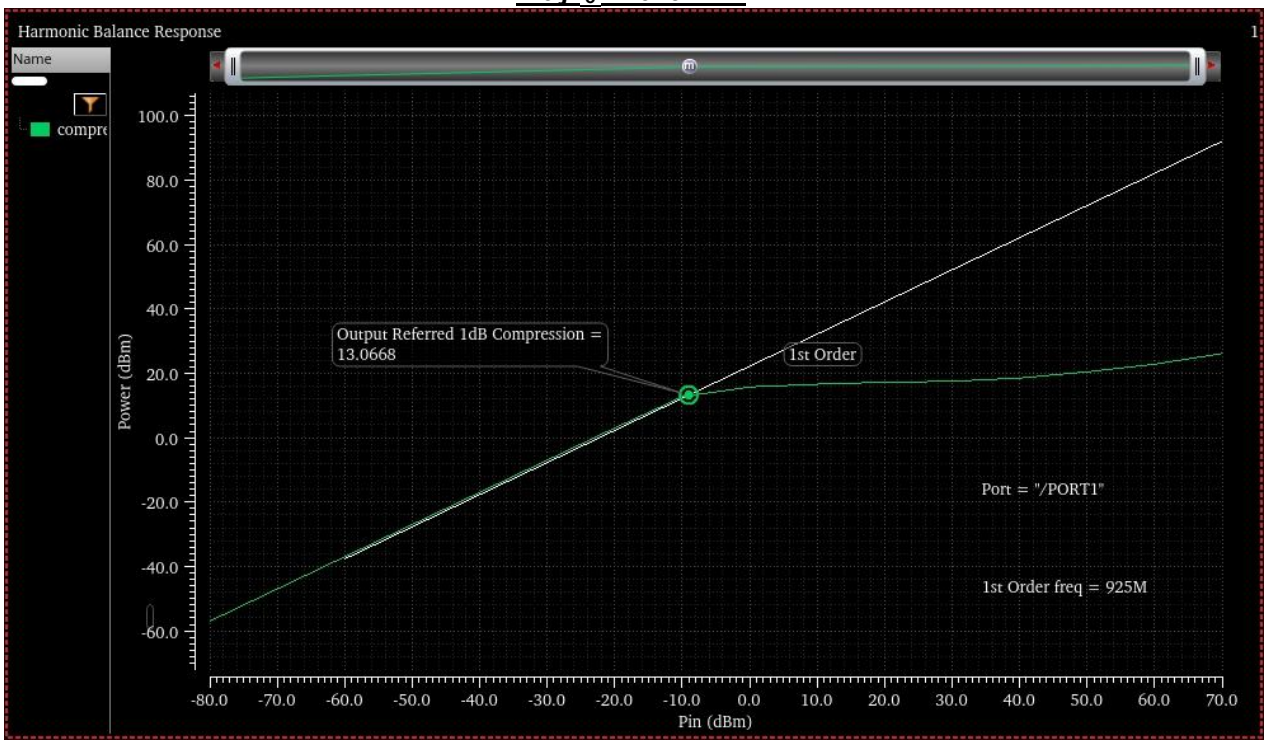


Component Values Table

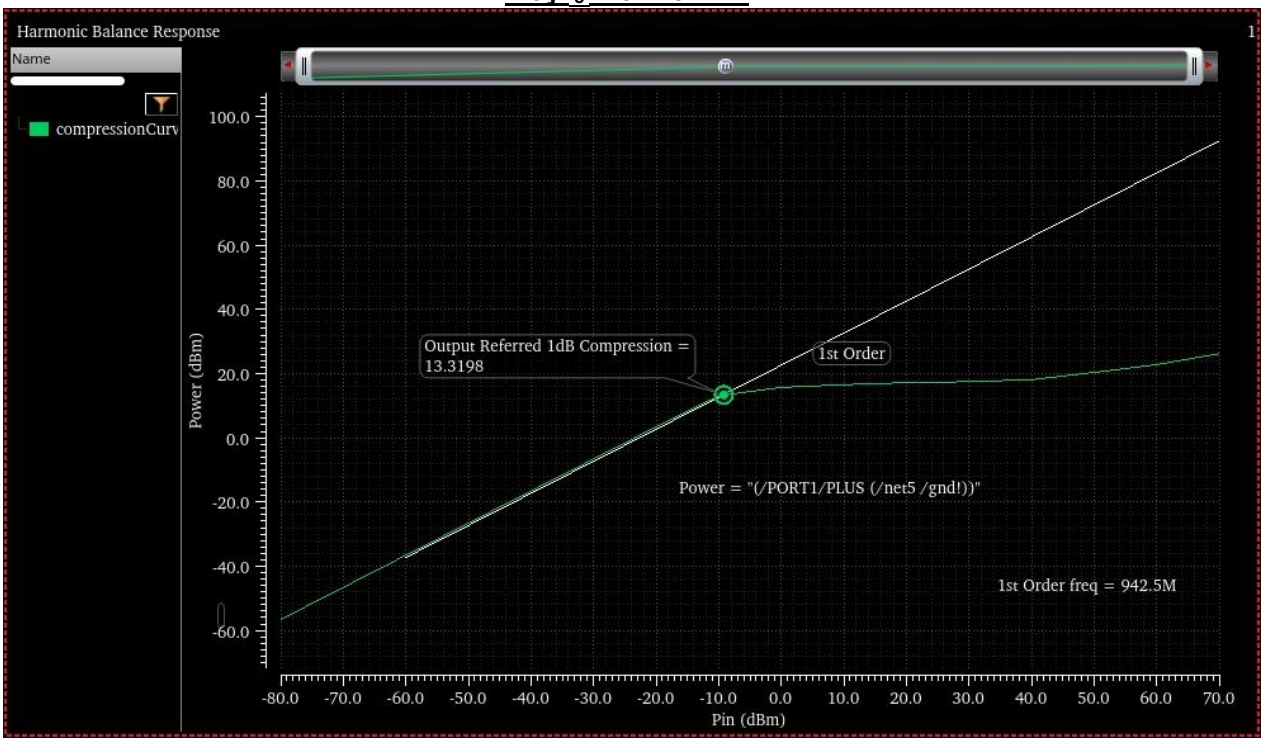
(W, L) MOS Amplifier = 70x1µm, 180nm	(L, C) Drain Tank = 10nH, 2.81pF
(W, L) Current Mirror MOS = 15x270nm, 180nm	Bias Current = 0.35mA
R_bias = 1 MΩ, C_coupling = 10uF	V_DD = 1.8V, R_load = 50Ω

Output 1dB Compression Point Plots

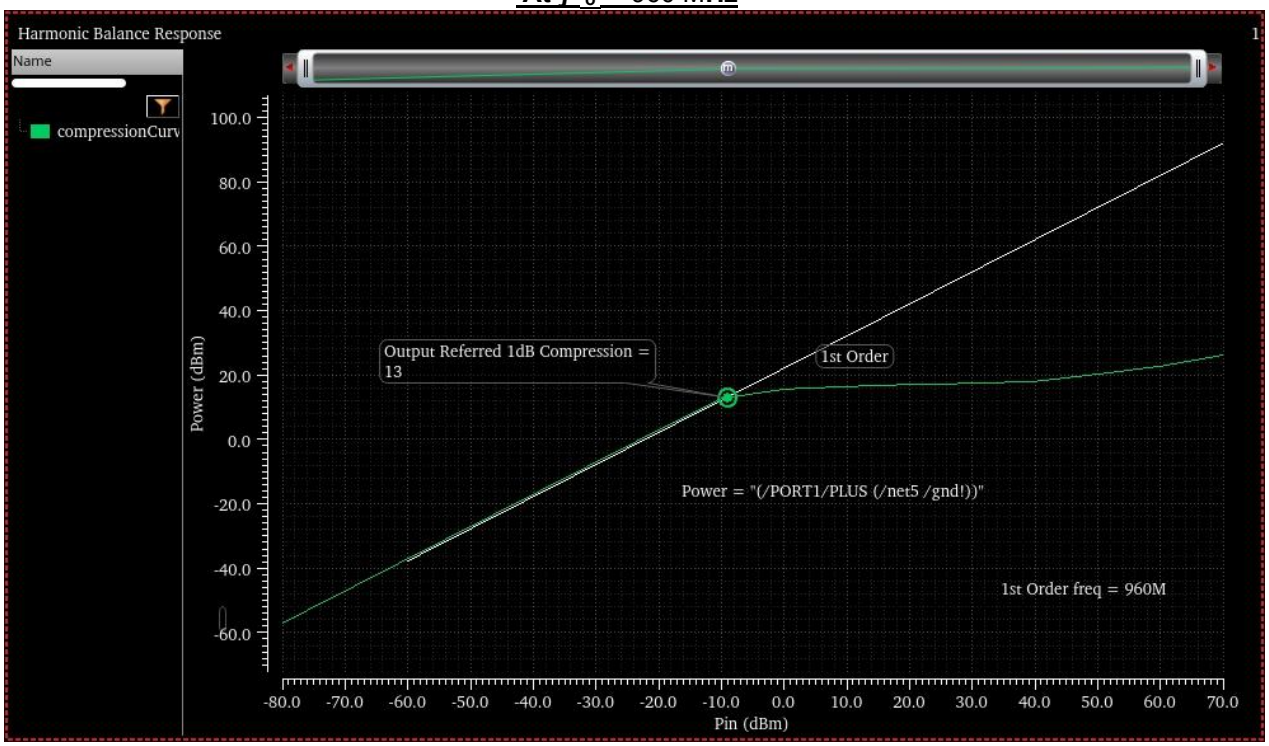
At f_o = 925 MHz



At f_o = 942.5 M**Hz**

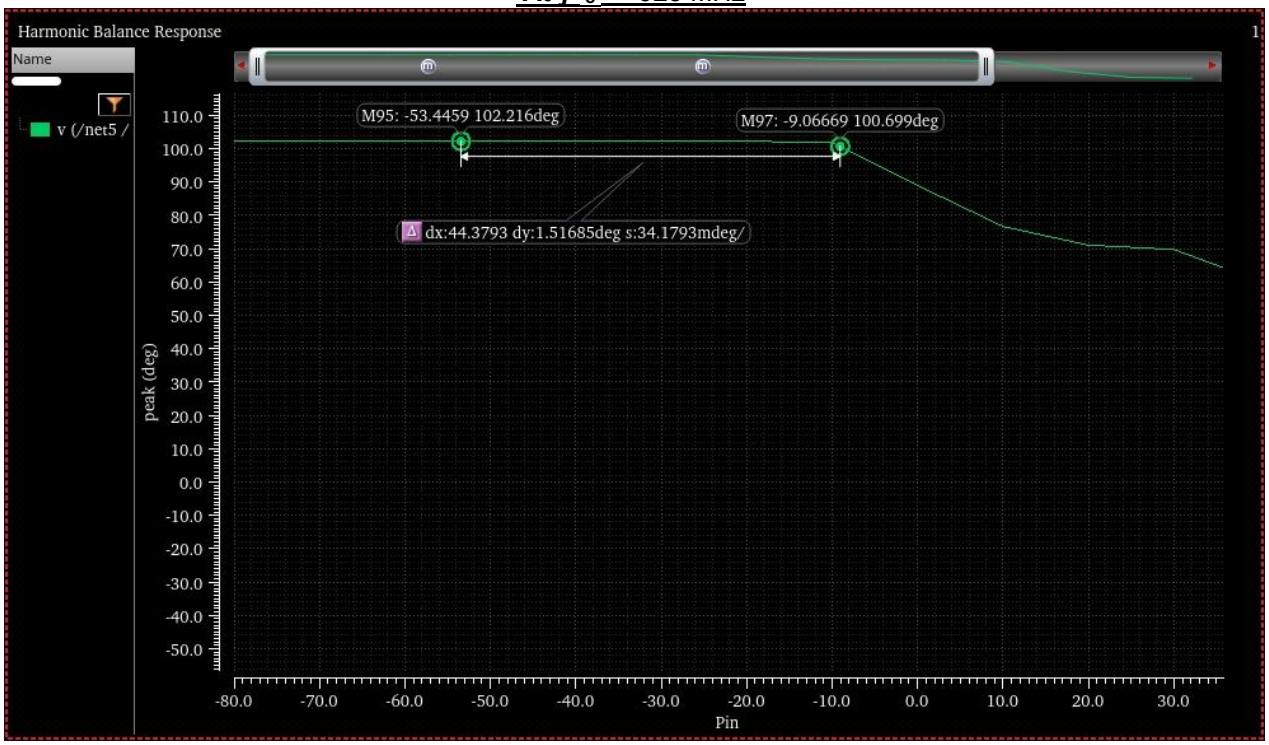


At f_o = 960 MHz

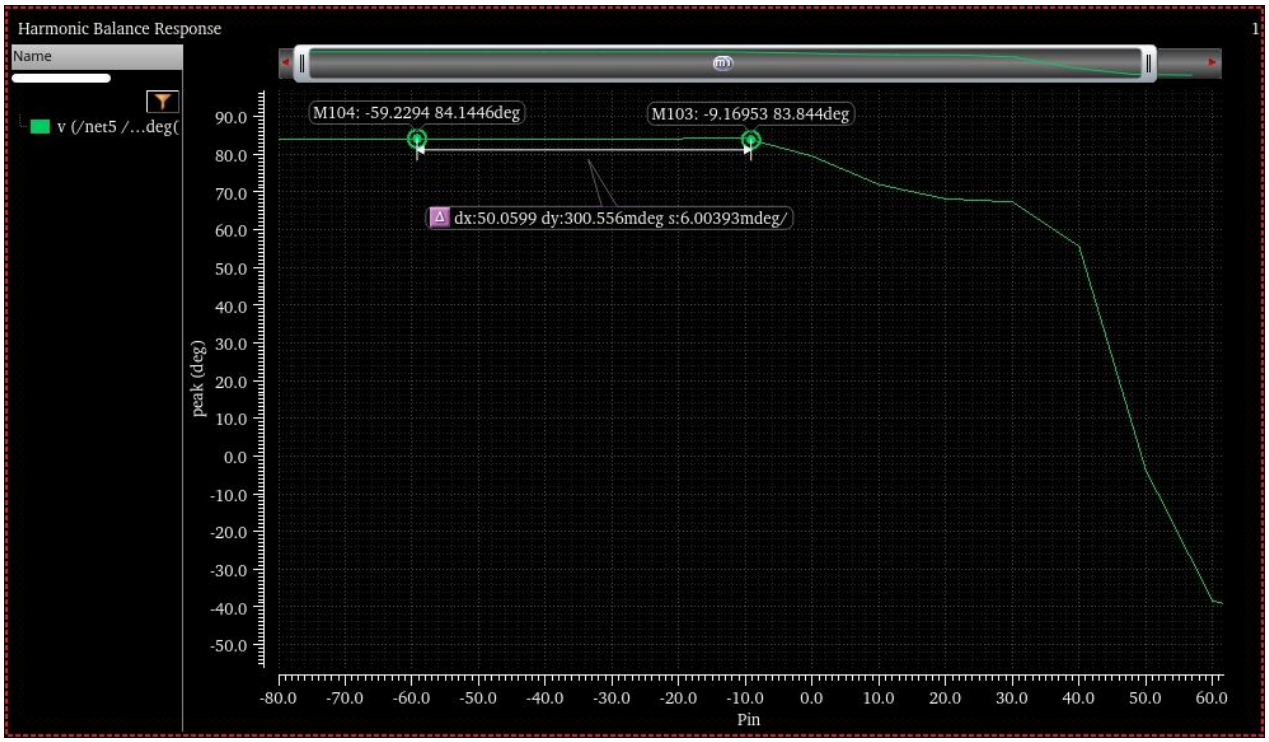


AM-PM Deviation Plots

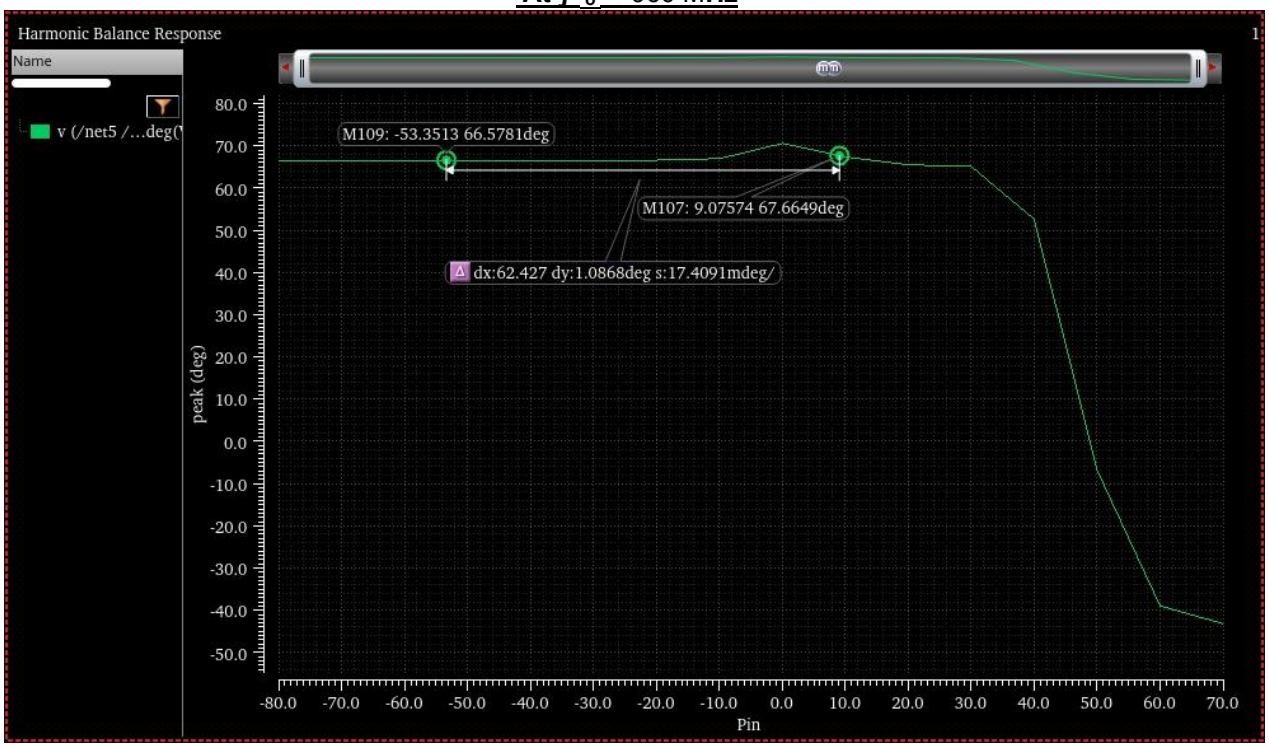
At f_o = 925 MHz



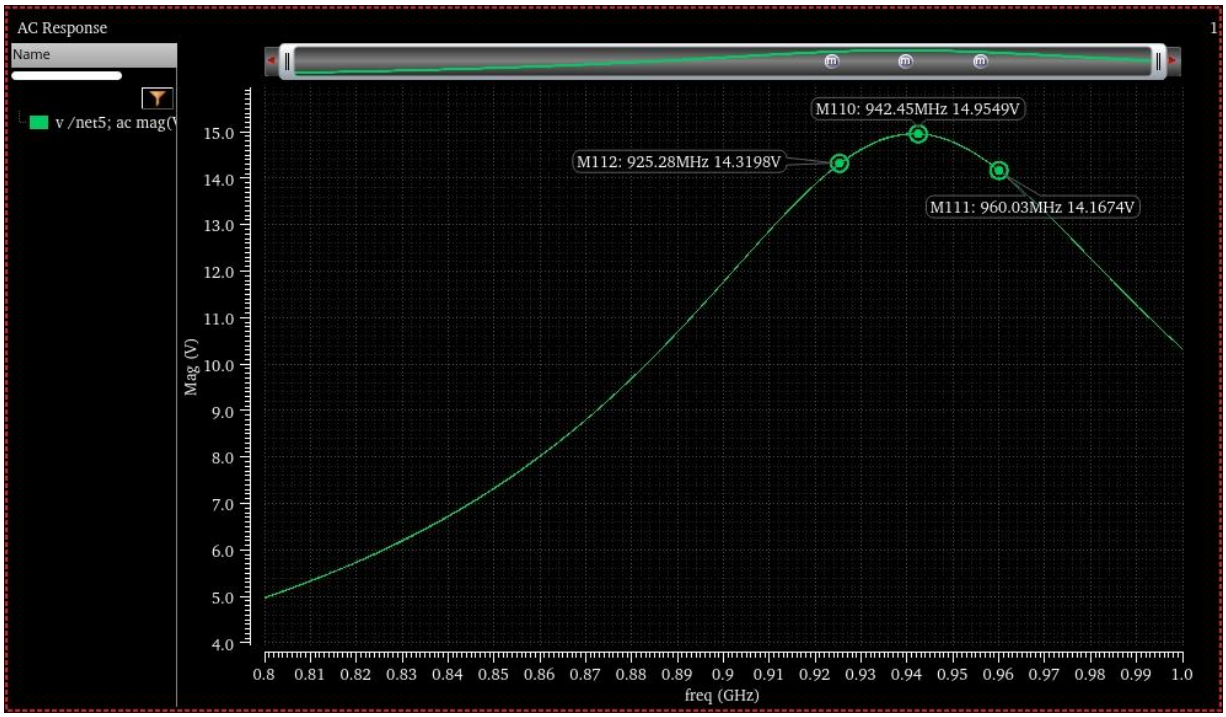
At f_o = 942.5 MHz



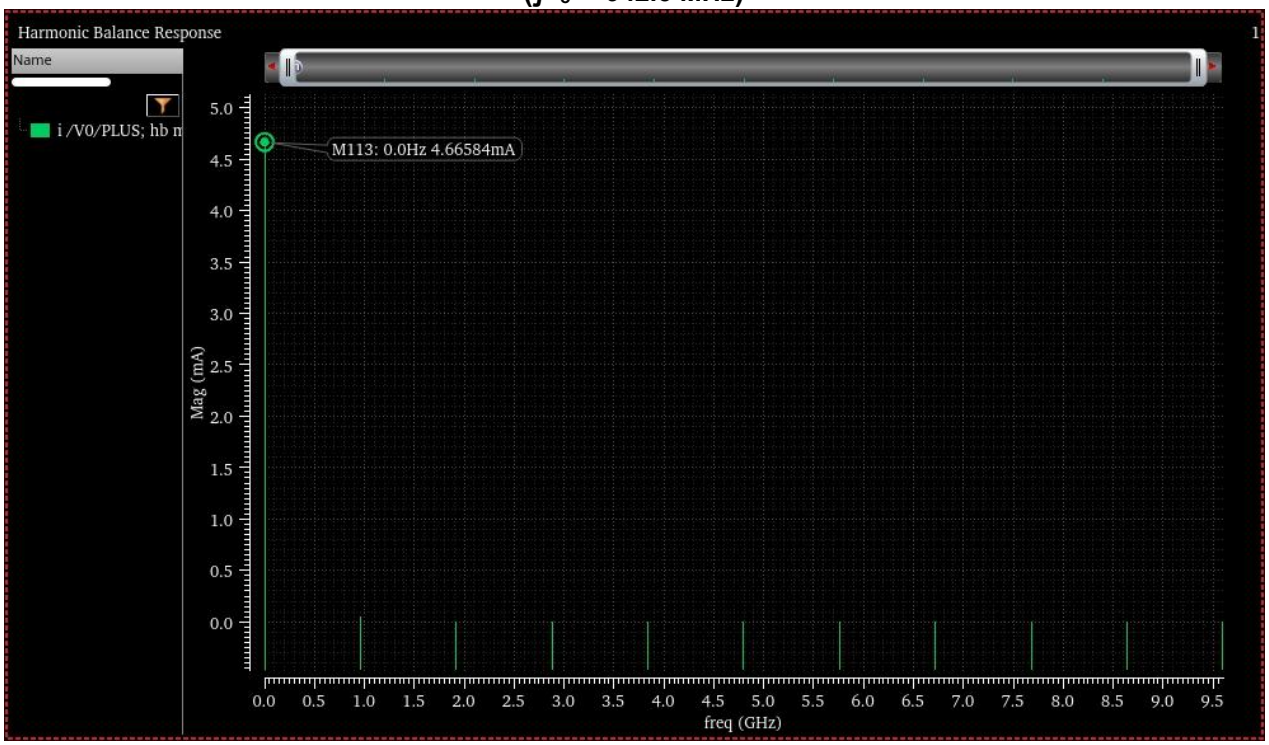
At f_o = 960 MHz



PA Volatge Gain Plot
(from Gate to Drain)



Current through VDD Plot
(f_o = 942.5 MHz)



Design Procedure

1. Rough Hand calculations to get an idea of voltage gain, transconductance and other parameters was done. MOS characterization was performed on the basis of calculations.
2. Voltage gain spec was just met at the desired frequency 5G-n8 band, but peak came to be 35V/V at some 5GHz frequency. So the Ld inductor was tweaked to get the peak at 942.5MHz.
3. During this attempt the Ld came out to be large 220nH to resonate out the Cdb, so an extra 2.81pF Cdb was added to get Ldmax=10nH.
4. Voltage gain spec was just met with peak at desired frequency but the 1db compression point was not good. The Bias voltage was increased deliberately to get more Ibias and therefore more gain to meet 1dB compression point spec.
5. Phase deviation spec was naturally met once 1dB compression point spec was met.
6. Every possible iteration and tweak are done to cut the corners and met specs at their verge to minimize power consumption.
7. Input and output VCVS were added to curb the in/out Matching, since no spec were defined for those.

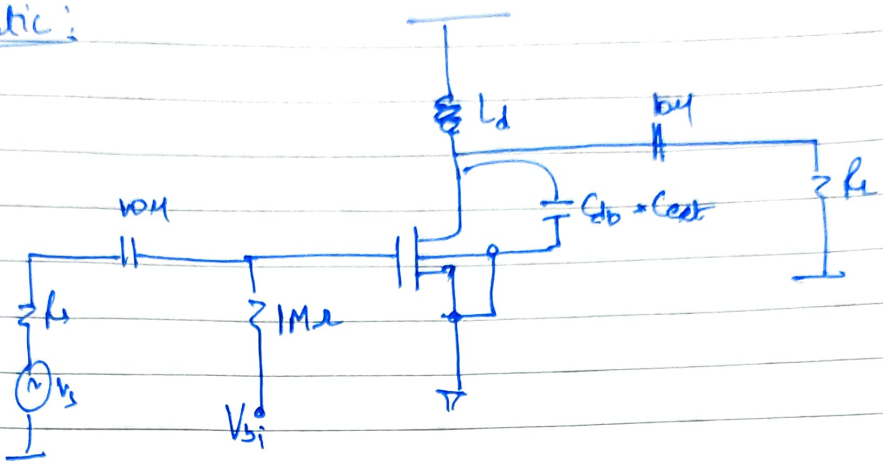
Path to Project Files

/home/ee24m106/cadence_project/RFIC_courseproject/PA_test

RESHUL JINDAL
EE24M106

RFIC - PA Project
Hand Calculations

Schematic:



$$g_m R_L = 2$$

$$g_m = \frac{2}{50} = 40\,mA/V$$

for resonating C_{DB} and C_{out}

$$f_0 = \frac{1}{2\pi\sqrt{L_d(C_{DB}+C_{out})}}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_d(23.6fF + C_{DB})}} \qquad (C_{out} = 2.81\,pF)$$

$L_d = 10nH$ (Max allowed)

$\Rightarrow C_{DB} = 23.6fF$

The MOS has to be appropriately sized to get $C_{DB} = 23.6ff$ and $g_m = 40mA/V$ to get gain

→ I_D (bias) was checked at this arrangement and appt. V_{GS} applied through V_{bi}