EE6320 RF Integrated Circuits Project: Mixer Design

Mixer Performance Summary Table

	Design Metric	Performance	Specification
Conversion Gain	Minimum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	22.915dB	>20 *dB*
	Maximum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	22.933dB	>20 *dB*
	Peak Gain flatness in specified band [Max-Min Gain]	0.02dB	-
	3*dB* RF Bandwidth [From the plot of $f_{RF} = f_{LO}$]	3.35GHz	-
	Minimum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	22.91dB	>20 *dB*
	Maximum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	22.93dB	>20 *dB*
Noise Figure	Maximum SSB Noise Figure for $f_{LO} = 925\ MHz$	6.97544dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 942.5\ MHz$	6.99216dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 960\ MHz$	7.0044dB	≤ 10 dB
Linearity - IIP_2	Input power used for extrapolation	-40dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-22dBm	-
	Power of IM_2 Tone at output (at chosen input power)	-90dBm	-
	Extrapolated IIP_2	31.7466dBm	≥ +30*dBm*
Linearity - IIP_3	Input power used for extrapolation	-40dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-20.5dBm	-
	Power of IM_3 Tone at output (at chosen input power)	-100dBm	-
	Extrapolated IIP_3	0.216dBm	≥ 0 *dBm*
Power	Mixer DC power consumption [Excluding Bias]	1.44mW	Minimize
	Bias circuit power consumption	42.3µW	Minimize
Other	Sum of all resistances [excluding bias]	2KΩ	-
	Sum of biasing resistances	2MΩ	-
	Sum of all capacitances [Including AC coupling]	2µF	-
	Sum of all inductances	NA	

	Load chosen (each R_load)	1KΩ	-
	Differential Mixer Input Capacitance (C_gs Caps)	118fF	-
	Simulator Used	Cadence Virtuoso	-

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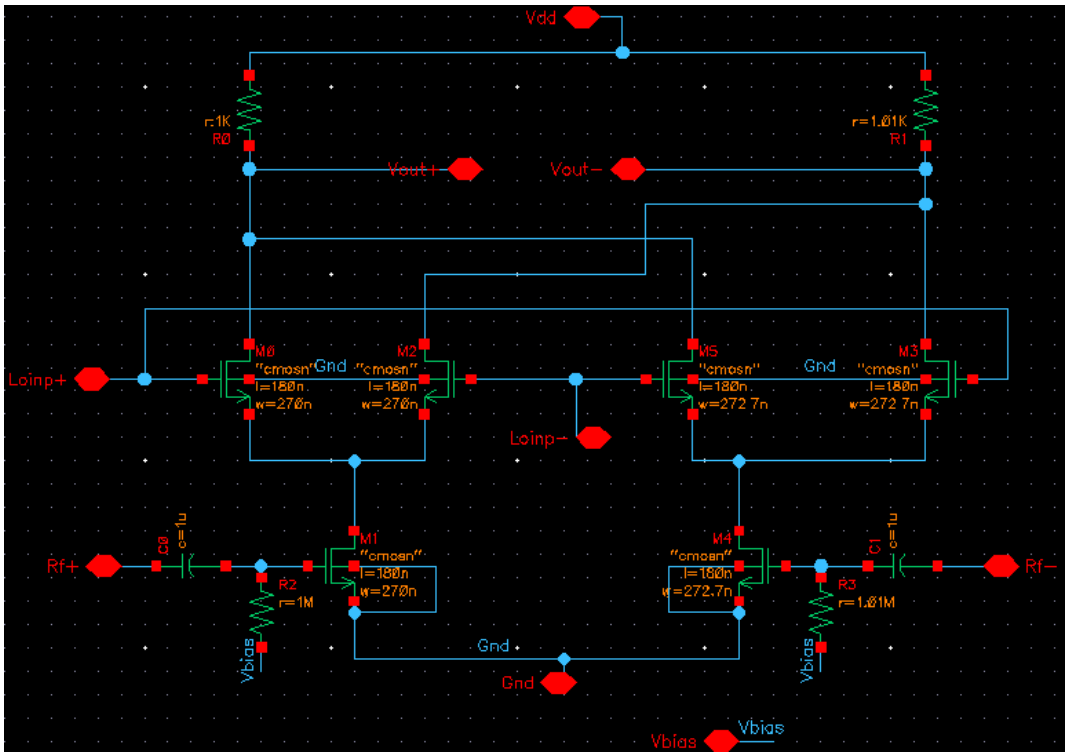
LNA + Mixer Performance Summary Table

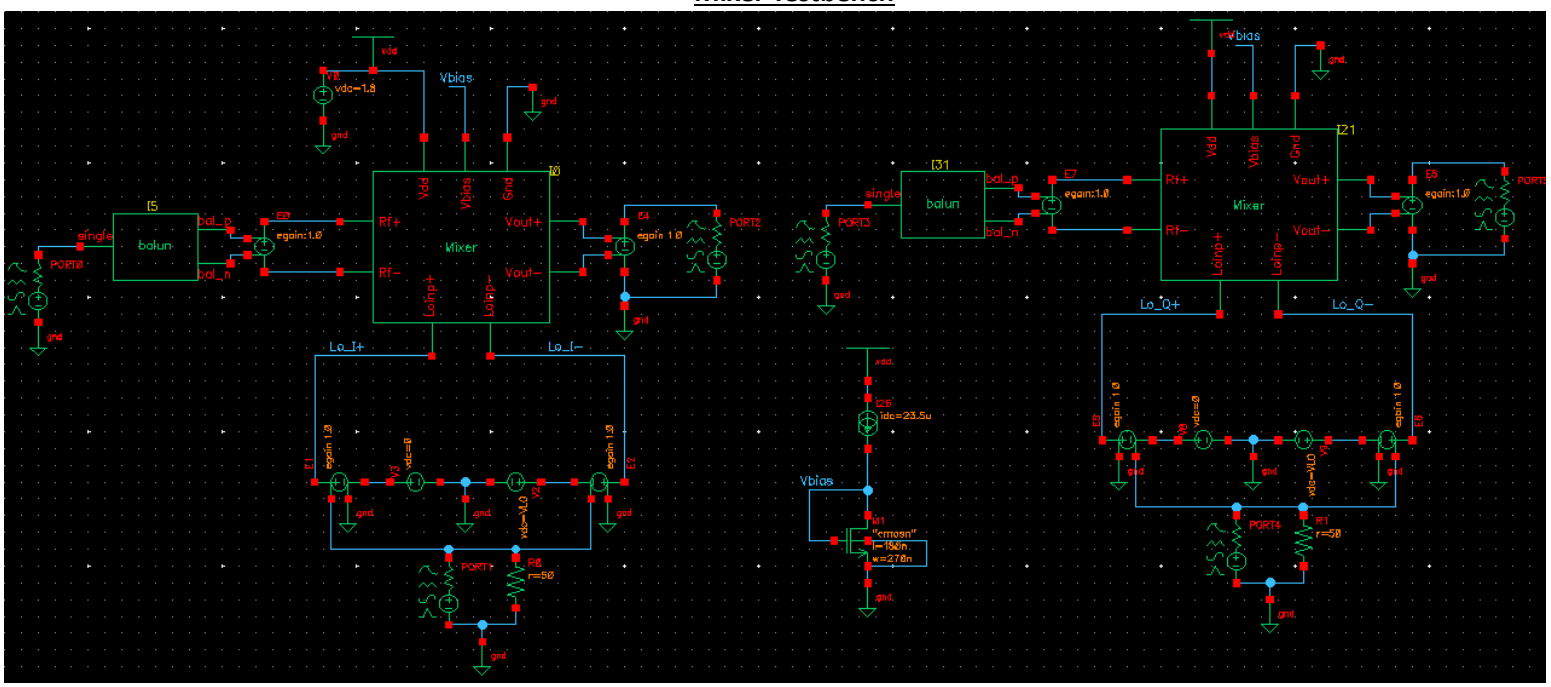
	Design Metric	LNA	Mixer	Cascade	
				Expected	Simulated
Conversion Gain	$f_{IN} = f_{LO}$, f_{LO} = 925 MHz	40.453dB	22.933dB	63.386dB	59.9dB
	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 925 MHz	40.705dB	22.93dB	63.635dB	60.4dB
	$f_{IN} = f_{LO}$, f_{LO} = 942.5 MHz	40.86dB	22.924dB	63.784dB	60.72dB
	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 942.5 MHz	41.03dB	22.92dB	64dB	61.1dB
	$f_{IN} = f_{LO}$, f_{LO} = 960 MHz	41.12dB	22.95dB	64.07dB	61.325dB
	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 960 MHz	41.2dB	22.91dB	64.11dB	61.575dB
Noise Figure	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 925 MHz	1.94dB	6.97544dB	2.03dB	1.937dB
	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 942.5 MHz	1.92dB	6.99216dB	2.047dB	1.924dB
	$f_{IN} = f_{LO}$ + 10MHz, f_{LO} = 960 MHz	1.927dB	7.0044dB	2.046dB	1.922dB
Linearity IIP3	Input power used for extrapolation	-60dBm	-40dBm	-	-70dBm
	Power of Fundamental Tone at output (at chosen input power)	-40.24dBm	-20.5dBm	-	-8.91dBm
	Power of IM_3 Tone at output (at chosen input power)	-160.486dBm	-100dBm	-	-65.61dBm

	Extrapolated IIP_3	0.123dBm	0.216dBm	-	-41.4dBm
Power	Total power consumption [Excluding Bias]	74.704mW	1.44mW	76.144mW	76.122mW
	Bias circuit power consumption	2.736mW	42.3µW	2.7783mW	2.7783mW

Mixer Schematic



Mixer Testbench



Design Variable Values

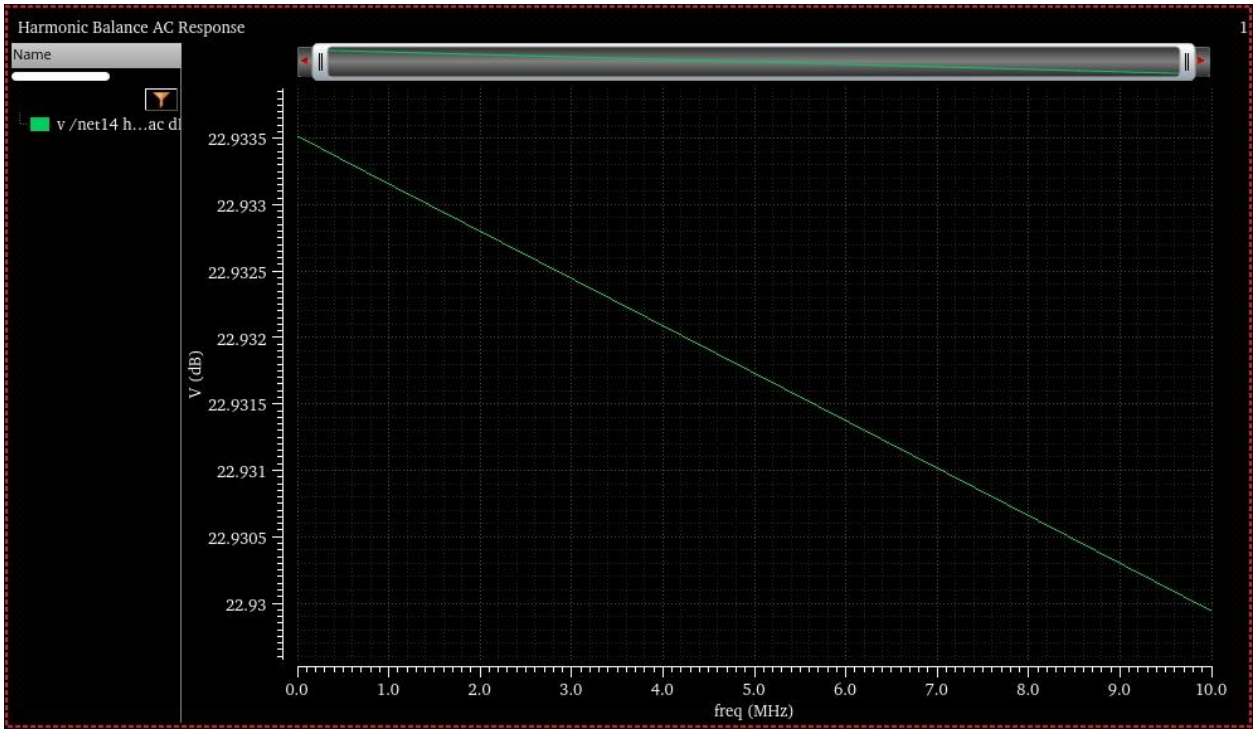
Design Variable	Value
Resistance (load, each side)	1KΩ
Length of all MOS	180nm

Width of Switch MOS (all 4)	**90 x 270nm = 24.3µm**
Width of Transconductance MOS (both MOS)	**280 x 270nm = 75.6µm**
Bias Current	**23.5µA**
V_LO Amplitude	**0.95V**

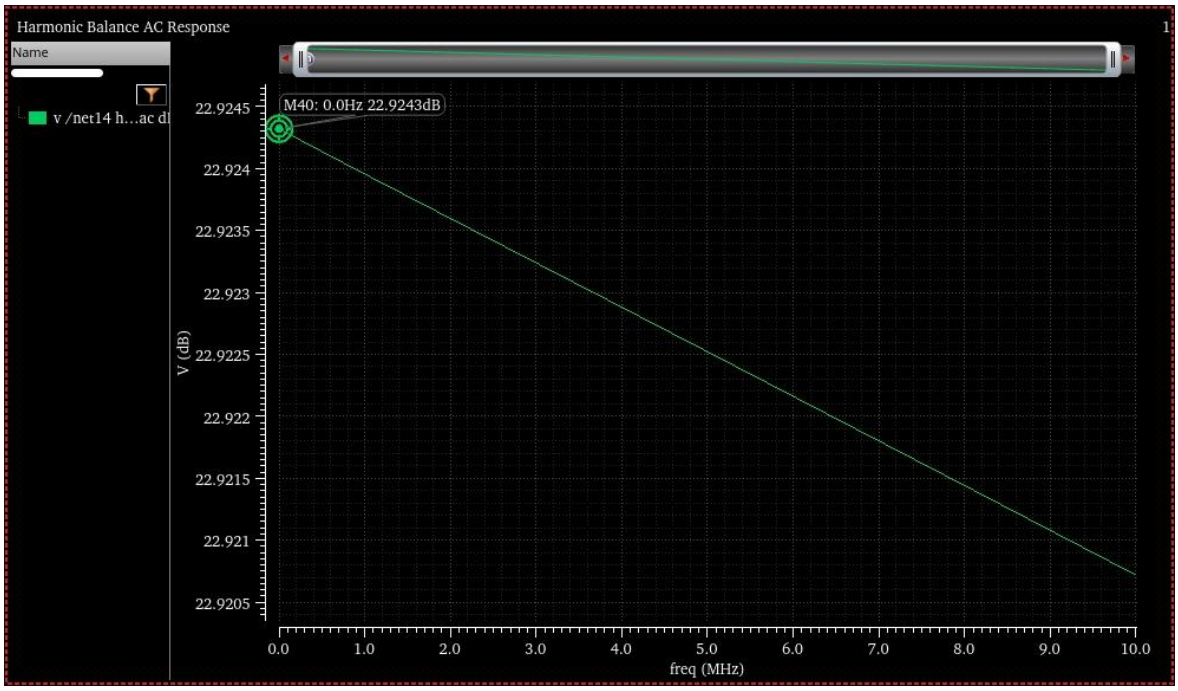
Fixed Constant Parameters

- **Transconductance MOS C_gs: 118fF**
- **Current Mirror MOS: W = 15 x 270nm = 4.05µm, L = 180nm**
- **Coupling capacitances: 1µF (each)**
- **Bias Resistances: 1MΩ (each)**

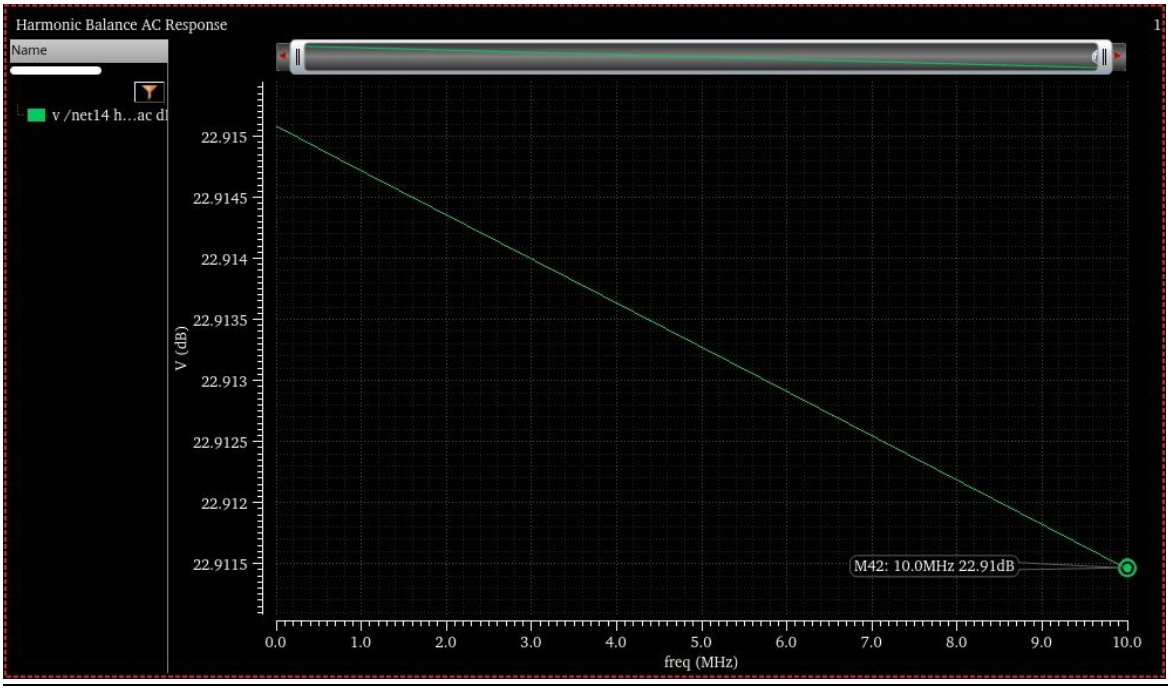
Conversion Gain of Mixer at 925 MHz



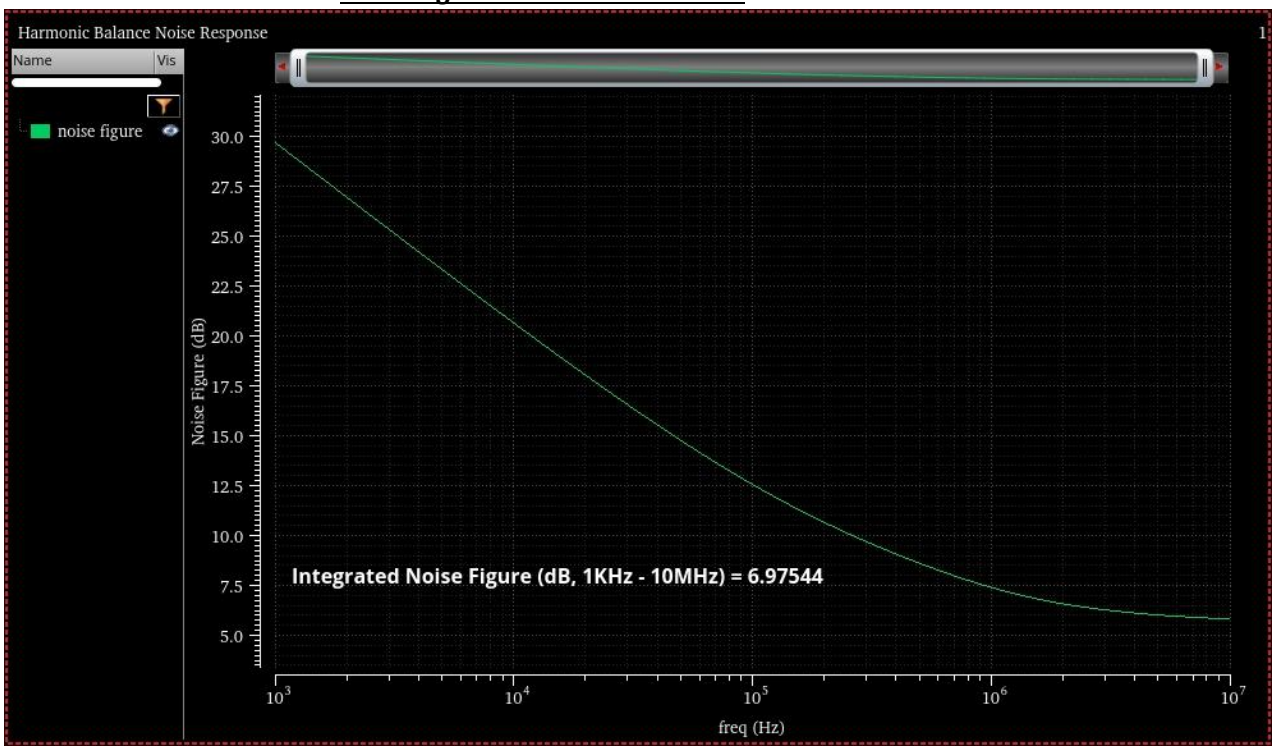
Conversion Gain of Mixer at 942.5 MHz



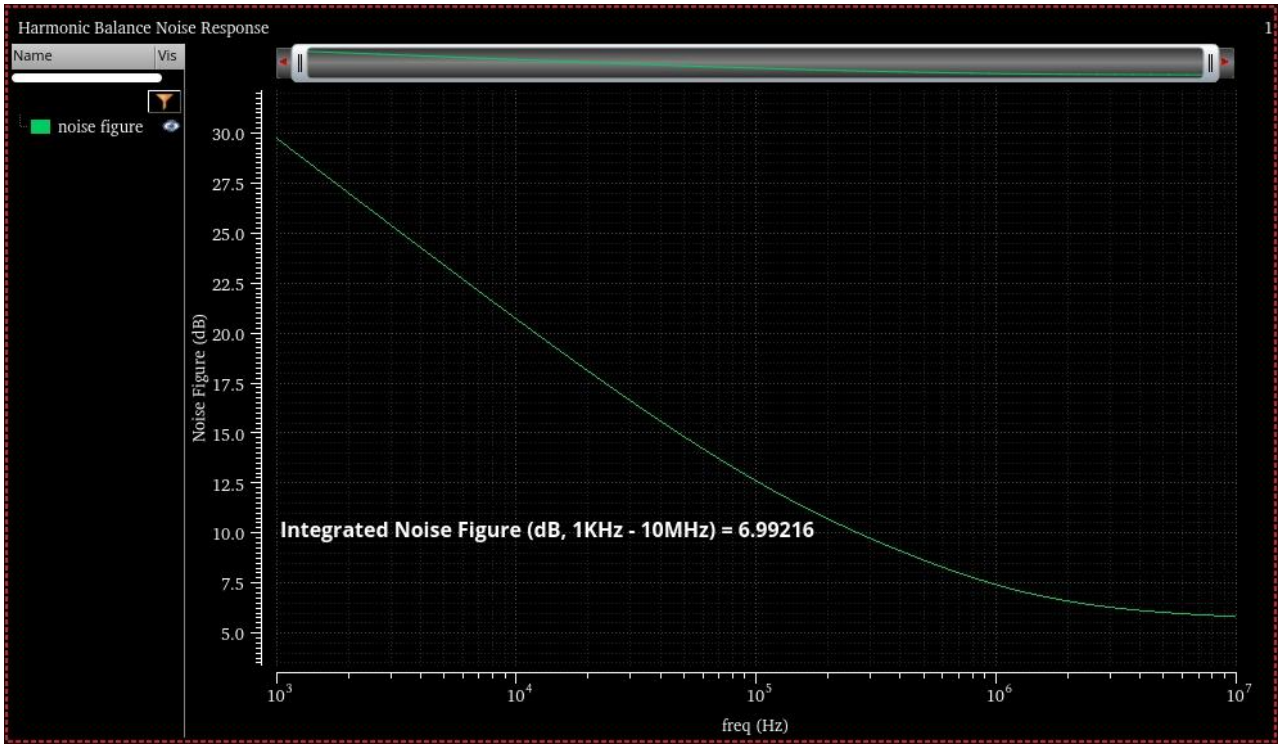
Conversion Gain of Mixer at 960 MHz



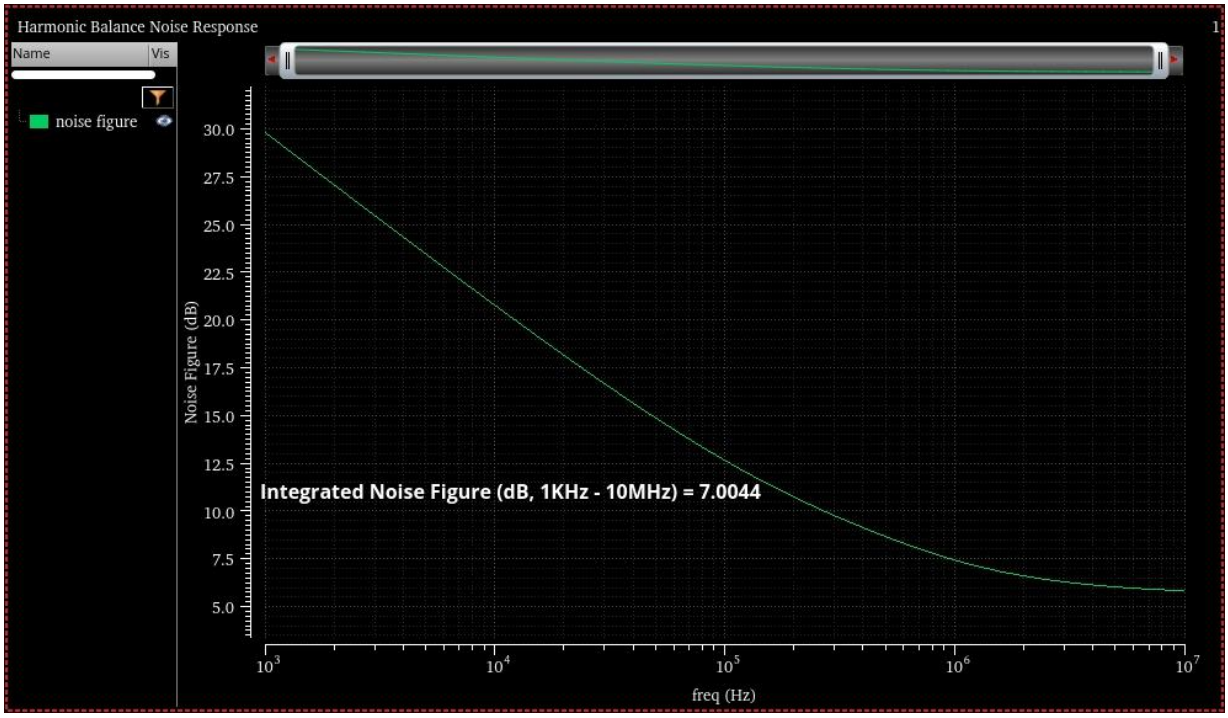
Noise Figure of Mixer at 925 MHz



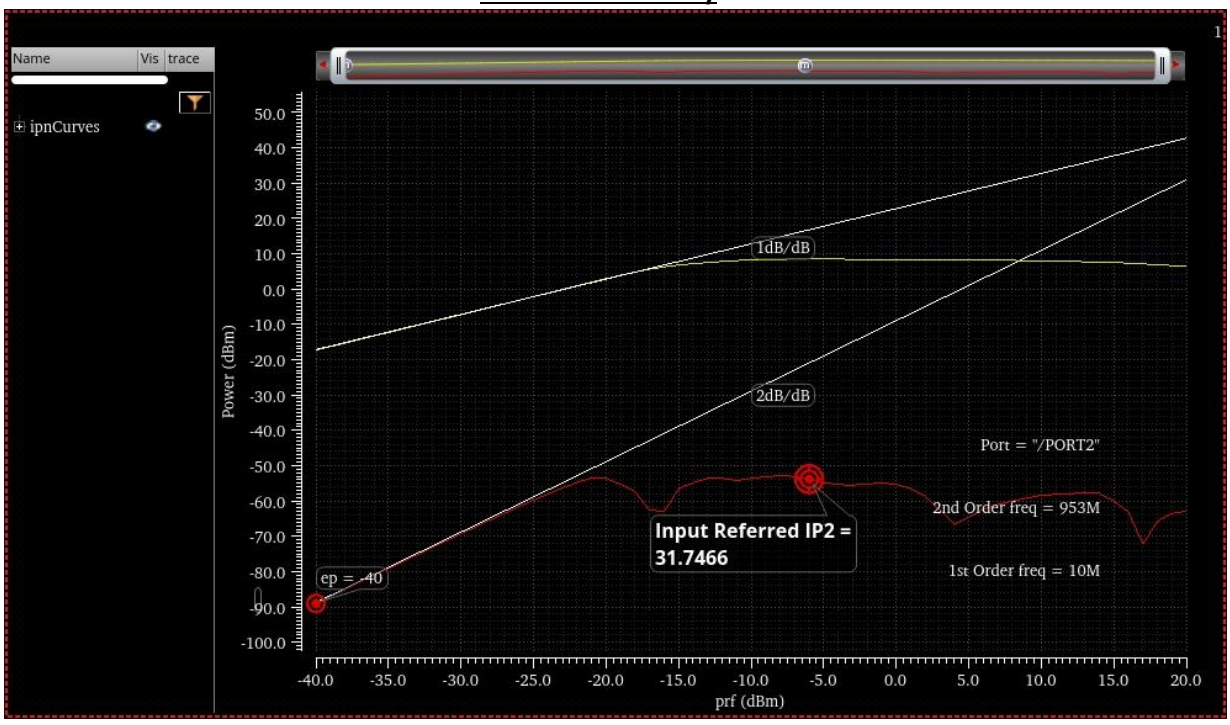
Noise Figure of Mixer at 942.5 MHz



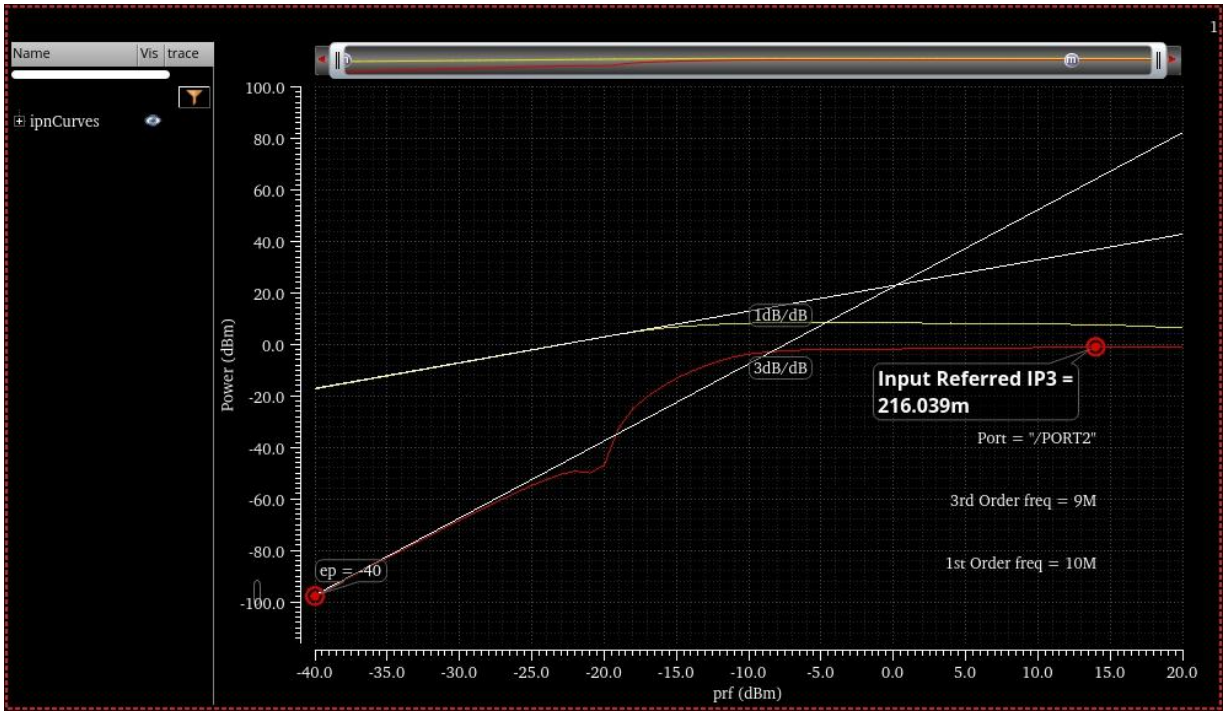
Noise Figure of Mixer at 960 MHz



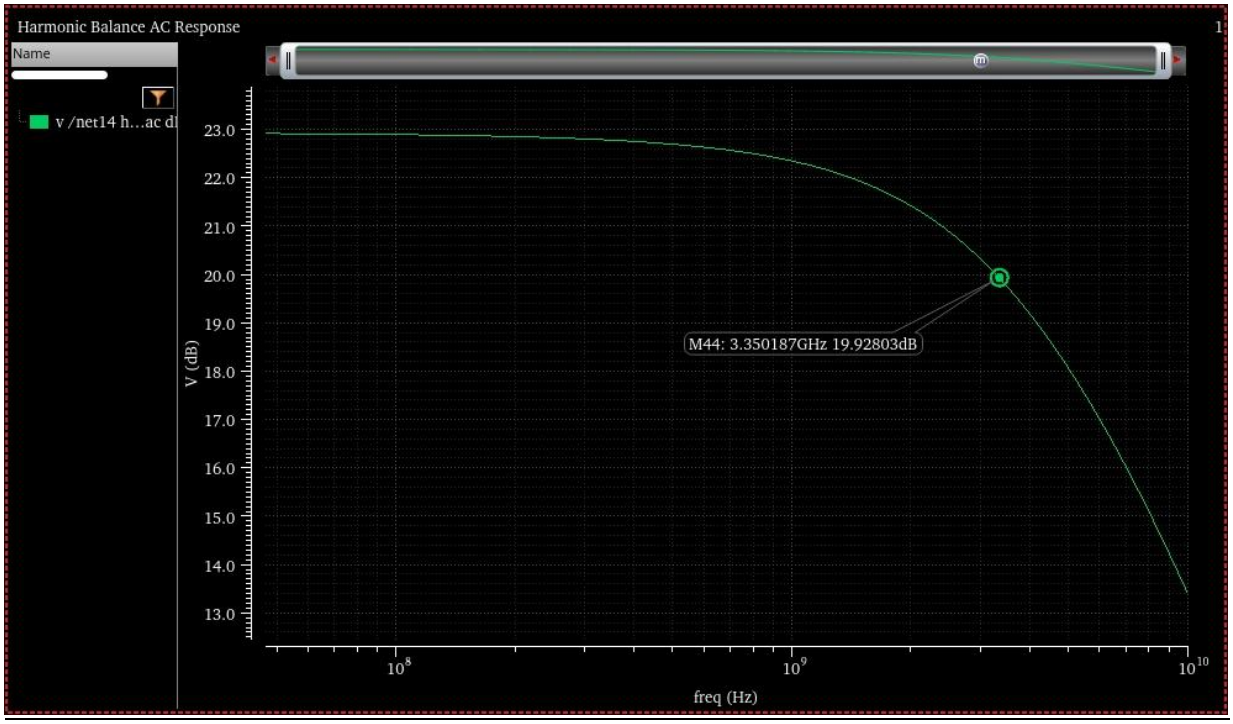
Mixer IIP2 Linearity



Mixer IIP3 Linearity

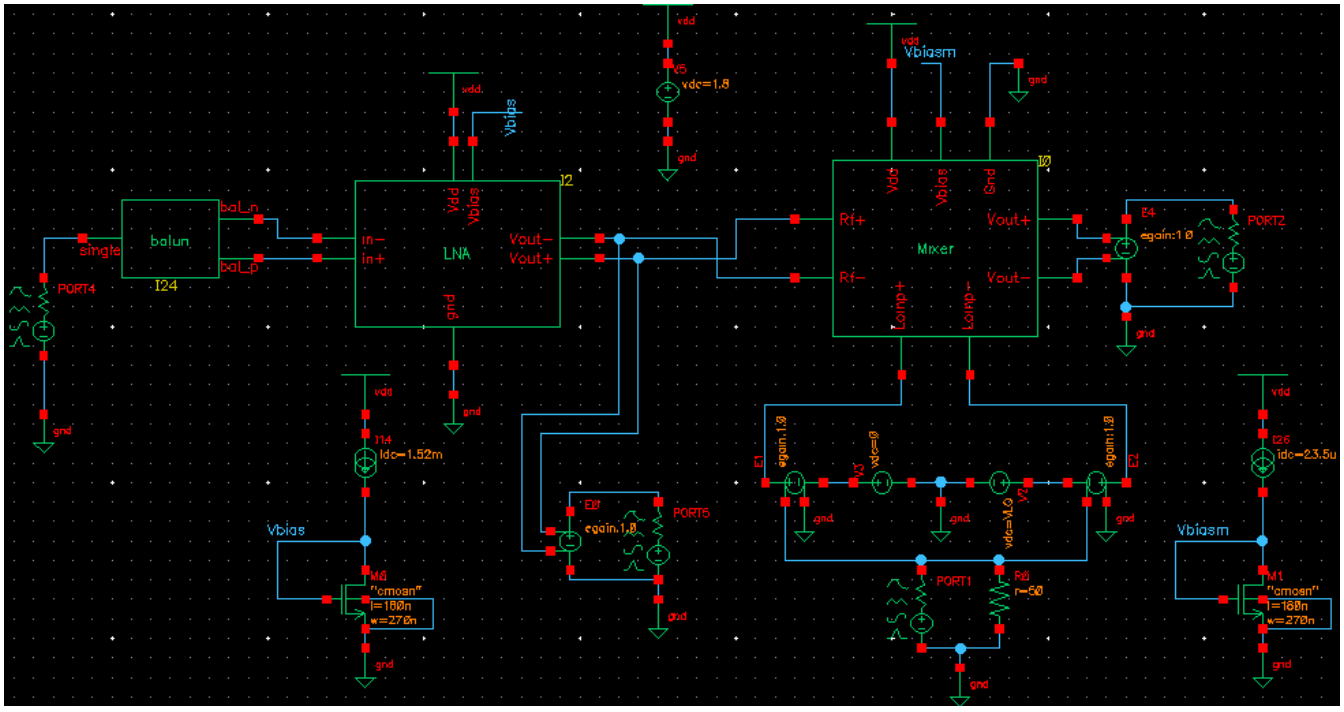


Mixer 3-dB Bandwidth

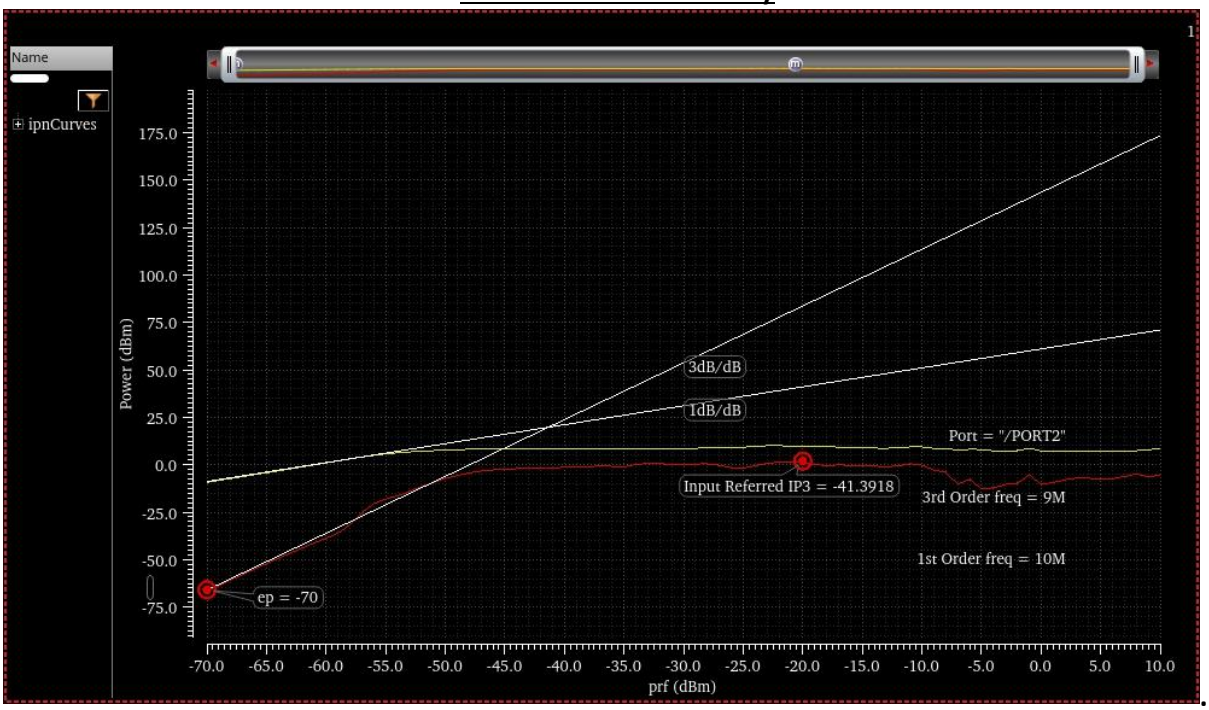


Mixer DC Power Consumption [Excluding Bias]

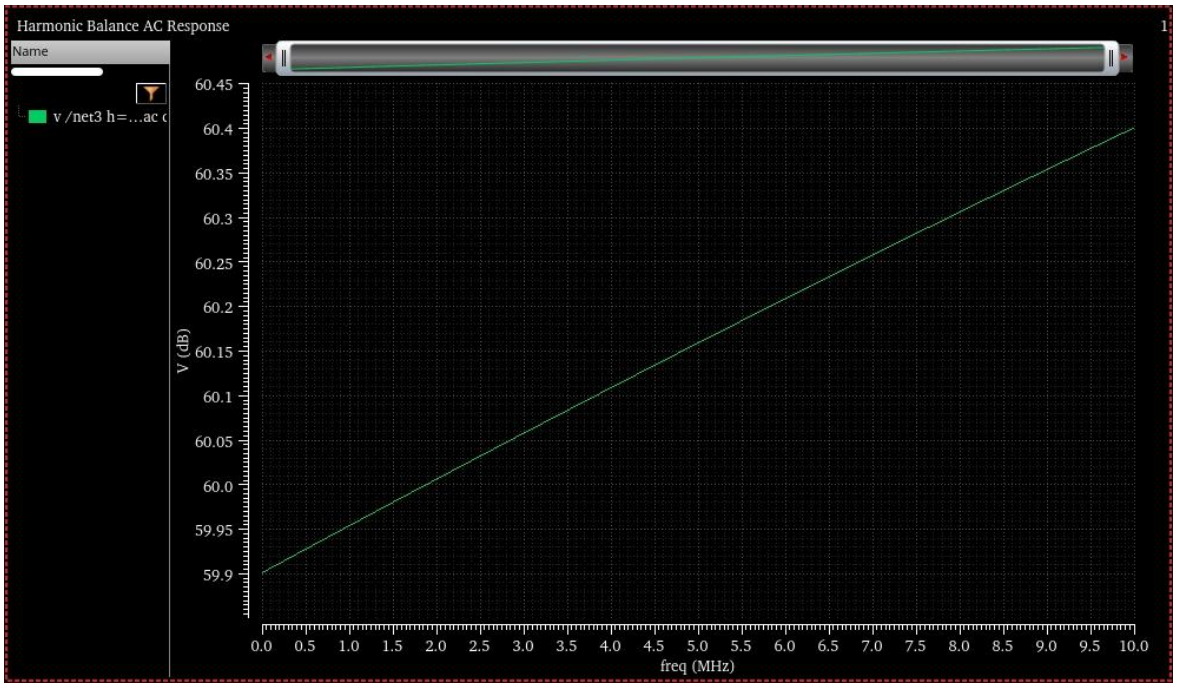
LNA + Mixer Testbench



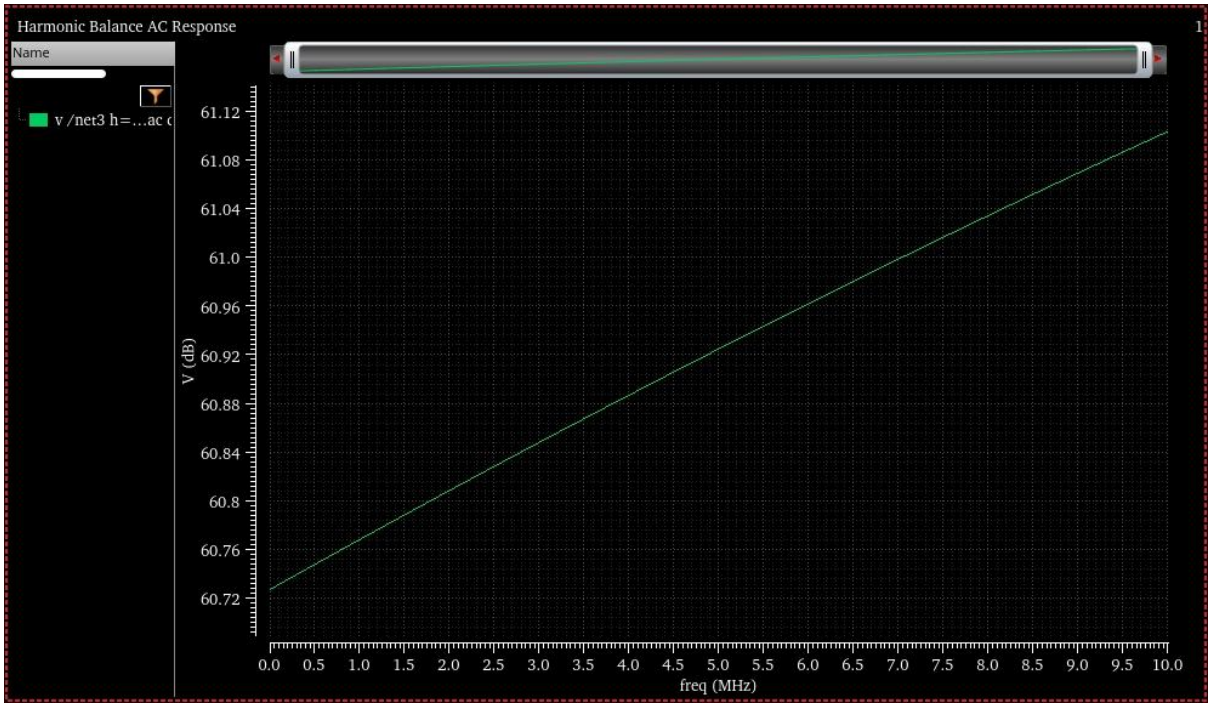
LNA + Mixer IIP3 Linearity



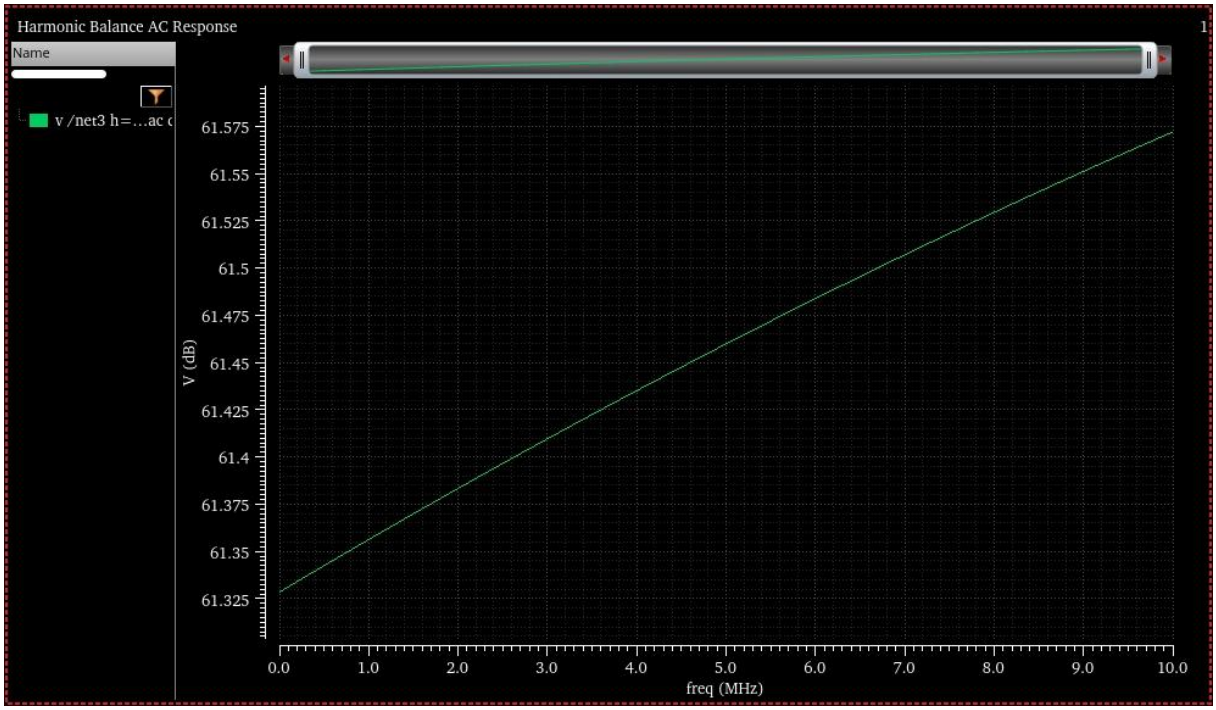
LNA + Mixer Conversion Gain at 925 MHz



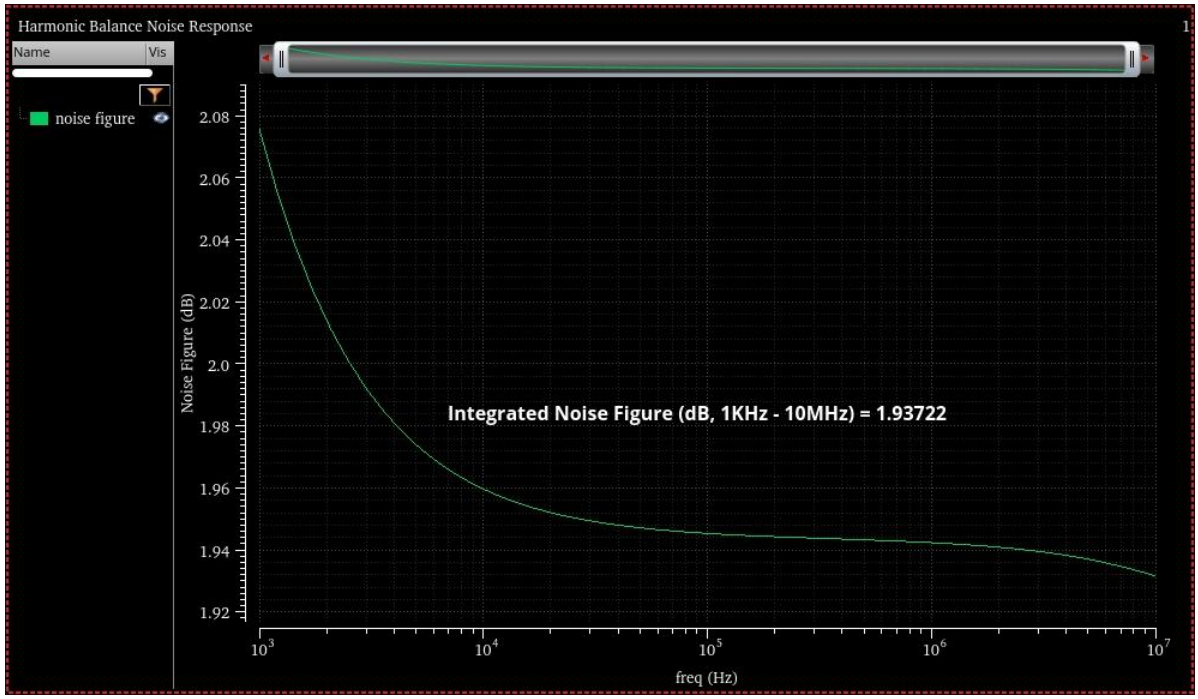
LNA + Mixer Conversion Gain at 942.5 MHz



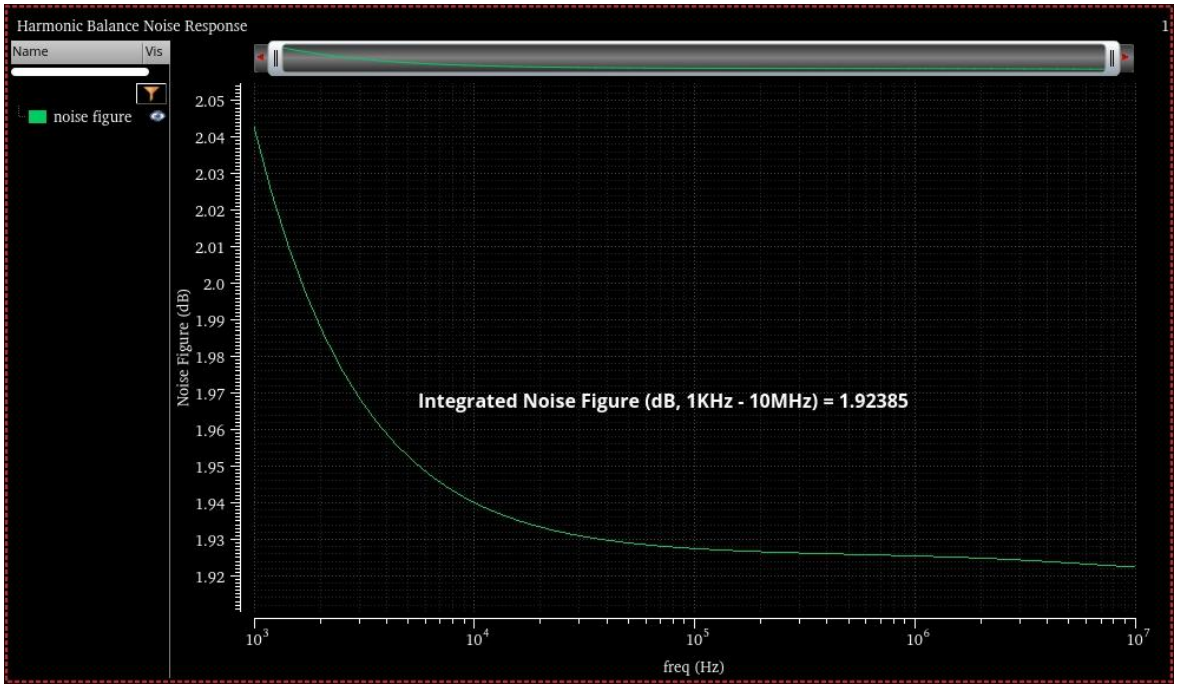
LNA + Mixer Conversion Gain at 960 MHz



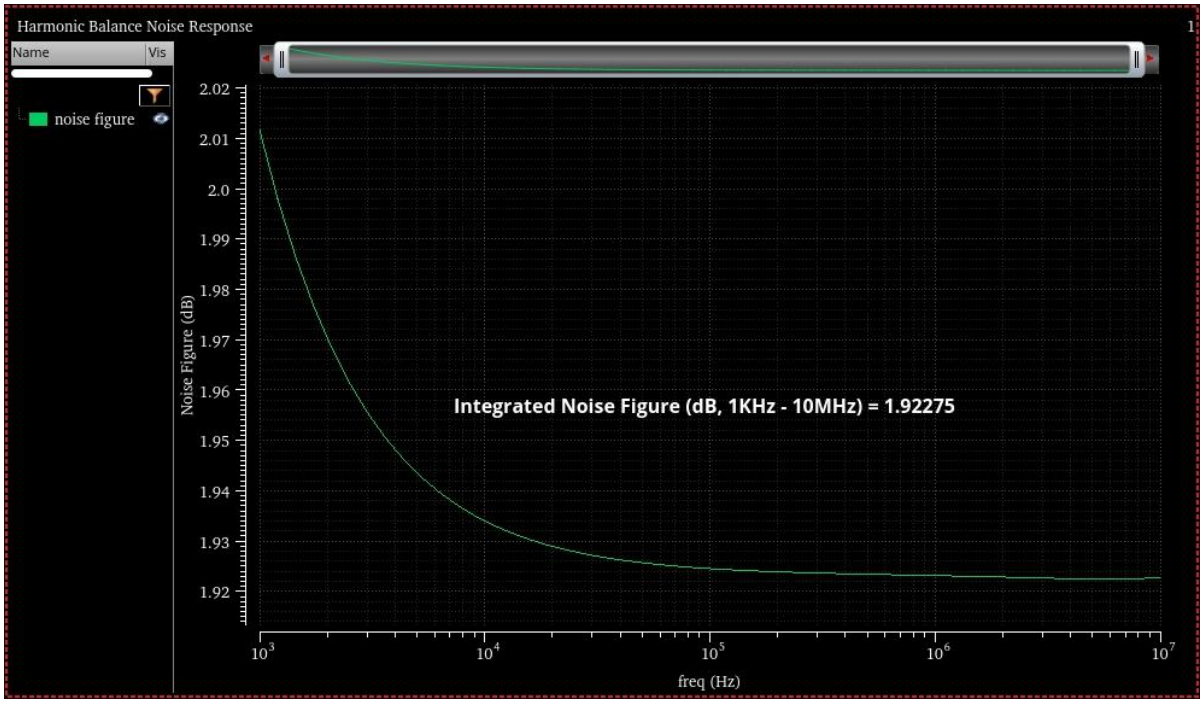
LNA + Mixer Noise Figure at 925 MHz



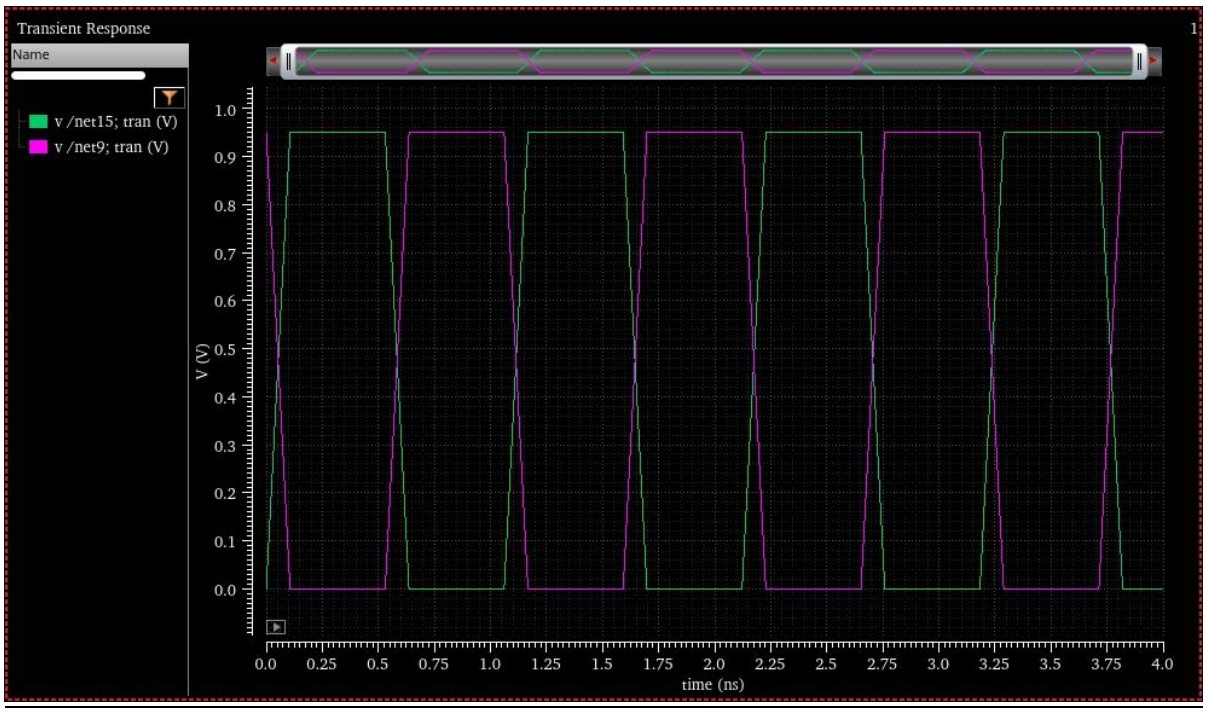
LNA + Mixer Noise Figure at 942.5 MHz



LNA + Mixer Noise Figure at 960 MHz



LO Waveform Characteristics



Characteristics taken are *(for generalized manner, as flo varies for various analysis)***:**

- **Frequency: flo Hz**
- **Time period: 1/flo Hz**
- **Delay time: 0 (for I Lo signal), 0.25/flo (for Q Lo signal)**
- **Pulse Width: 0.40/flo**
- **Rise/Fall Time: 0.10/flo**

Procedure adopted for the Project

1. First, hand calculations were performed to get the conversion gain more than 20dB.
2. The NMOS characterization was done to determine the size of both transconductance as well as switching NMOS, while getting required gm.
3. After making the circuit DC operating point analysis was conducted to verify the DC voltages and the gm.
4. Now we do the HB analysis to find the conversion gain and verify it to be greater than required.
5. HB noise analysis gives the integrated noise figure, it was easily achievable below 10dB.
6. IIP3 linearity is a small bump in the road, we need to check the third order derivative of the current with respect to Vgs for that. We need to bias the transconductance NMOS therefore at the Vgs where we see this derivative is close to zero. Now, this Vgs is generally lower than what we designed the Mixer initially and conversion gain might drop after the change in Vgs, therefore its recommended to design for a conversion gain at least 3dB if not 5dB higher than the required value, initially.
7. IIP2 is met easily, now you cascade the two (LNA + Mixer)
8. All the simulations were performed on the cascaded combination.
9. Everything obtained in the cascade was as desired.

Path to the Project Files

/home/ee24m106/cadence_project/RFIC_courseproject/mixer_rf

Calculations done for the Project

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Date:

Mixer Project
Hand Calculations

1) Conversion Gain $= \frac{2}{\pi} g_m R_d$

Gain $> 20dB$

$\frac{2}{\pi} g_m R_d > 10$

for $R_d = 1k\Omega$

$g_m = 15.7m$

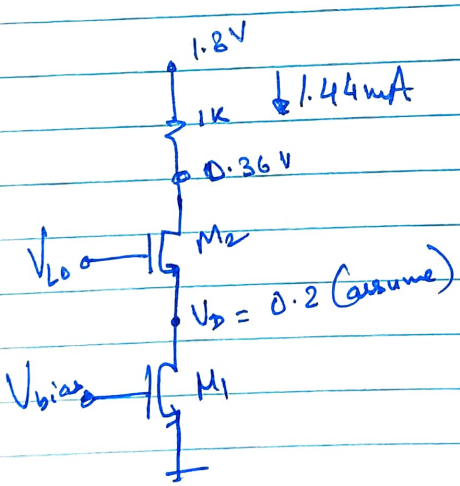
at this $g_m R_d$ we get exact 20dB so we must design for $g_m \simeq 20m$ so that after reduction of V_{GS} due to IIP_2 we still get gain $> 20dB$.

We use a current of 1.44mA to bias the cascode of transistors.

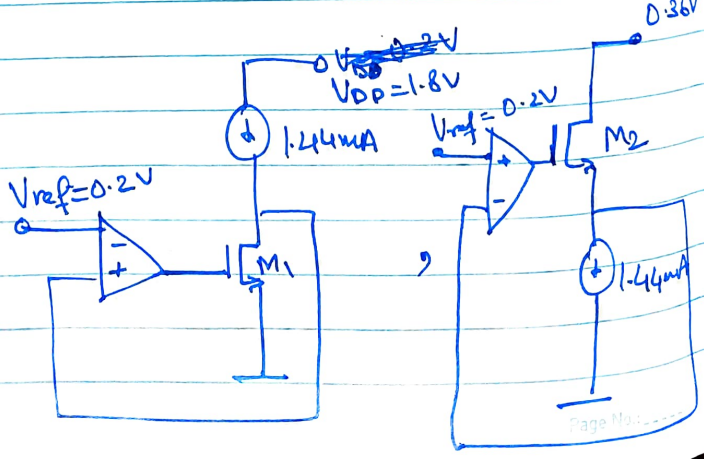
$V_{DD} - IR = 1.8 - 1.44 \Rightarrow 0.36V$

↓

available V_D for the stack of 2 transistors.



M_1 and M_2 must be sized accordingly. This can't be hand calculated but we can simulate it.



We simulate these ckts to find the W of transistors take $L = L_{min} = 180\,nm$.

2) Noise figure expected estimation using formula:

$$f_{eq} = f_1 + \frac{f_2 - 1}{G_1}$$

$$NF_{eq} = 10 \log_{10}(f_{eq})$$

for $f = 925\,MHz$

$10 \log_{10}(f_2) = 6.975$ $\quad \log f_1 = 1.94$

$f_2 = 4.98$ $\quad f_1 = 1.56$

$$f_{eq} = 1.56 + \frac{3.98}{108.45}$$

$$NF_{eq} = 2.03\,dB$$

Similarly we can calculate for other cases as well