EE6320 RF Integrated Circuits
Project: LNA Design

Performance Summary Table

Design metric	Measurement	Simulation Result	Requirement
Input matching	Worst case S11 in the specified band	-18.3 dB	< −15dB
	Band over which S11 ≤ −15dB	917Mhz to 970Mhz	925 to 960 MHz
Voltage Gain	Minimum Gain in the specified band	22.57 dB	≥ 20dB
	Maximum Gain in the specified band	22.86 dB	≥ 20dB
	Gain flatness in specified band [Max-Min Gain]	0.29 dB	≤ 1dB
	3dB Bandwidth	295Mhz	-
	Load Capacitance [Differential]	200f F (400f F single-end)	200f F
Noise Figure	Maximum Noise Figure in the specified band	1.94dB	≤ 2dB
	Minimum Noise Figure in the specified band	1.92dB	-
	Band over which NF ≤ 3dB	712MHz to 1.156Ghz	-
Linearity	IIP3 Tones used	943.5MHz, 944.5MHz	-
	Input power used for extrapolation	-60dbm	-
	Power of Fundamental Tone at output (at chosen input power)	-40.24dBm	-
	Power of IM3 Tone at output (at chosen input power)	-160.486dBm	-
	Extrapolated IIP3	0.123dBm	≥ 0 dBm
Power	LNA DC power consumption [Excluding Bias]	74.704mW	Minimize
	Bias circuit power consumption (power supplied by i_bias)	2.736mW	Minimize
Other	Sum of all on-chip inductances	61.004nH	-
	Sum of all off-chip inductances (2 Lg's)	107.2nH	-
	Sum of all resistances [Including bias]	2MΩ	-
	Sum of all capacitances [Including AC coupling, excluding load]	4μF	-
	Simulator Used	Cadence Virtuoso	-

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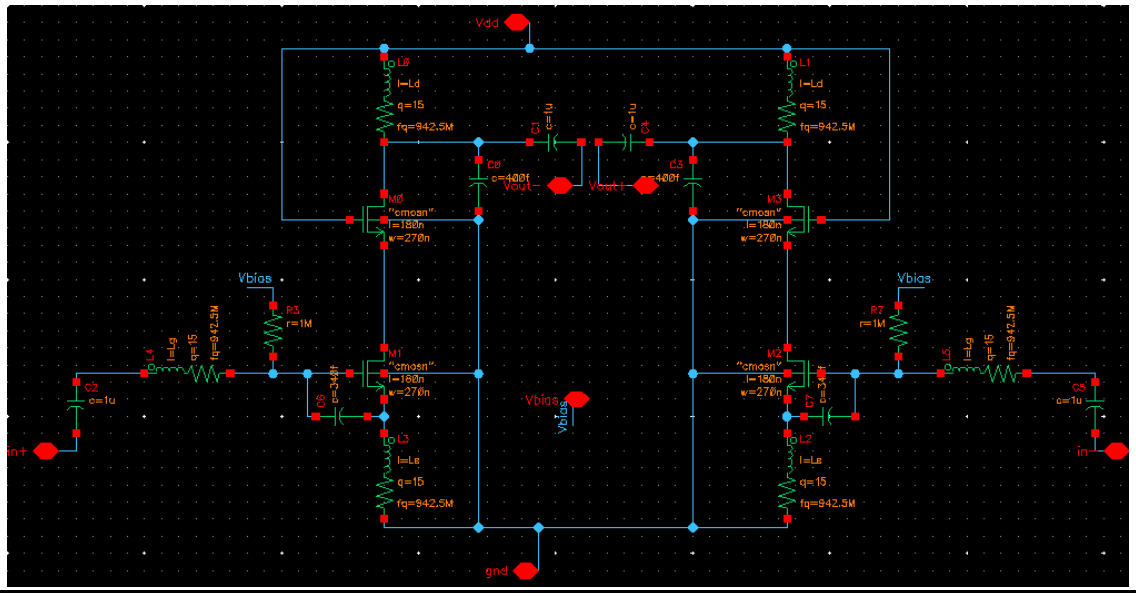
Roll No: EE24M106

LNA Schematic



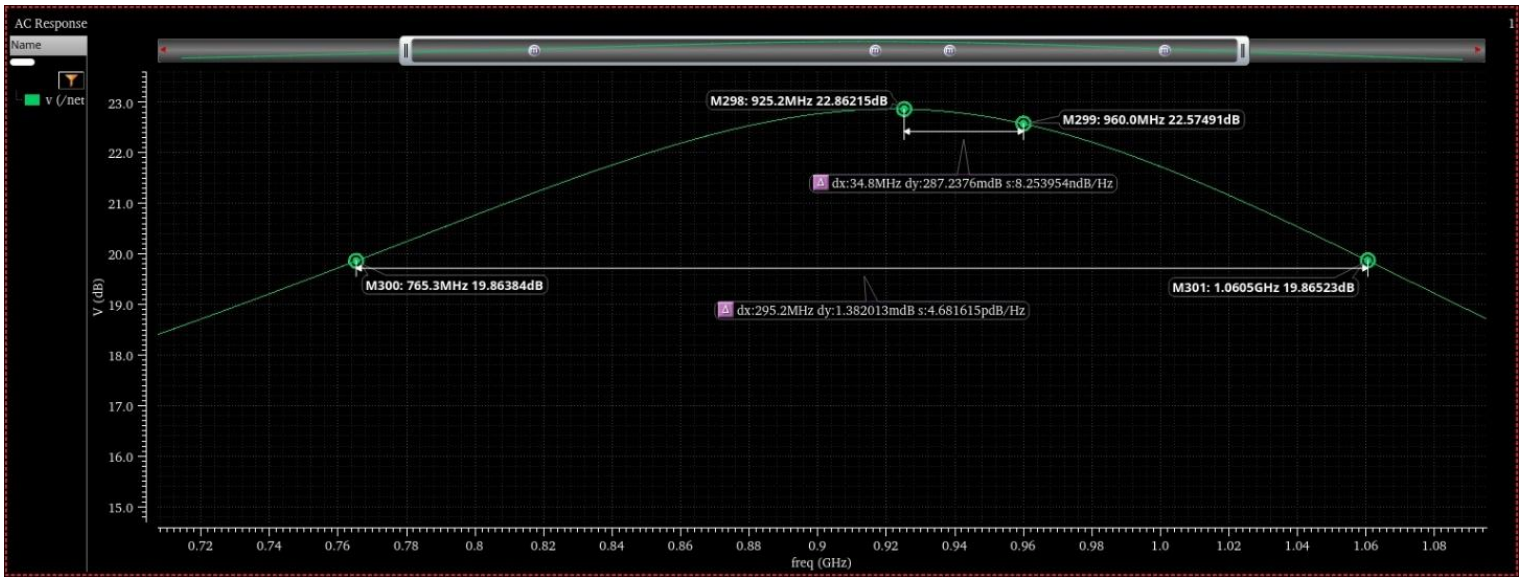
Component Values (one side values)		
Design Component	**Hand Calculated Value**	**Simulated Value**
Lg (gate inductance)	56.96nH	53.6nH
Ls (source inductance)	225.9pH	502pH
Ld (drain inductance)	71.28nH	30nH
Rd* (drain resistance)	6.33KΩ	2.66KΩ
R_ls* (res. parallel with Ls)	20Ω	49.6Ω
Rg* (res. parallel with Lg)	5.06KΩ	4.76KΩ

Fixed Constant Parameters

- LNA MOS parameters: W = 225x270nm, L = 180nm
- Current Mirror MOS parameters: W =15x270nm, L = 180nm
- I_bias (current): 1.52mA
- C_coupling: 1µF

* - intrinsic resistance to respective inductors (doesn't come in net resistance on/off the chip)

Gain Plot



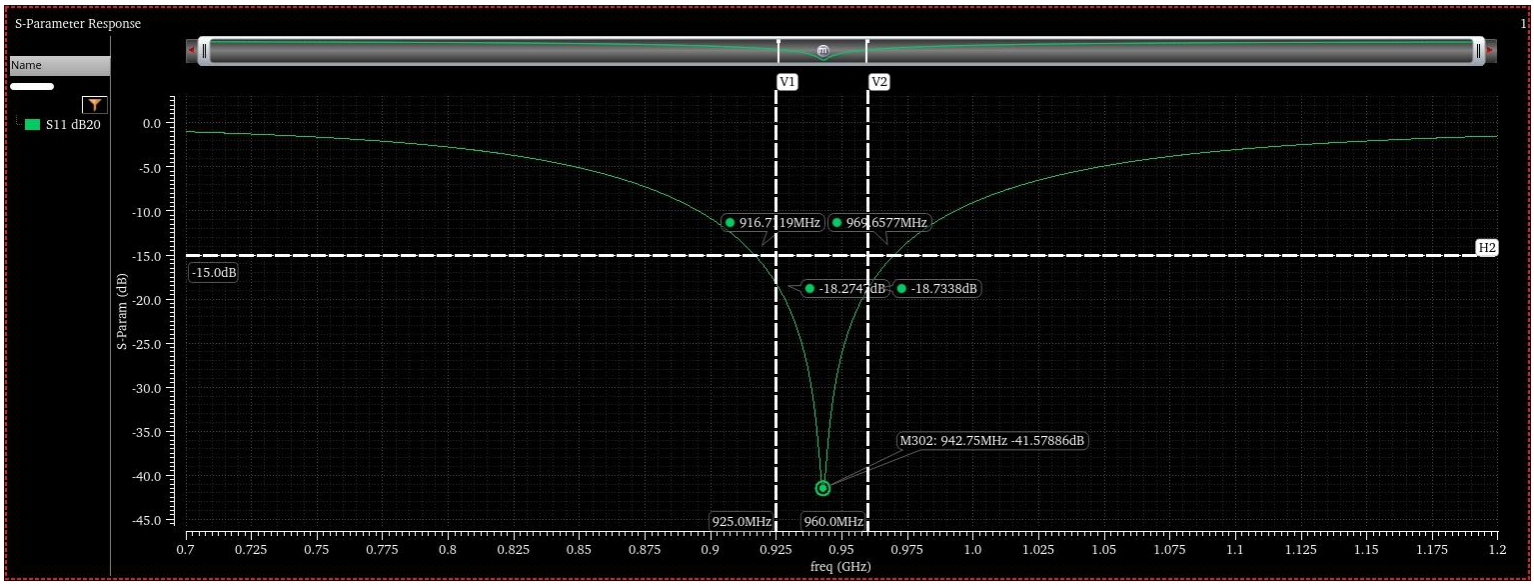
Max Gain through hand calculation: 45.42dB

Max Gain from the simulation: 22.86dB

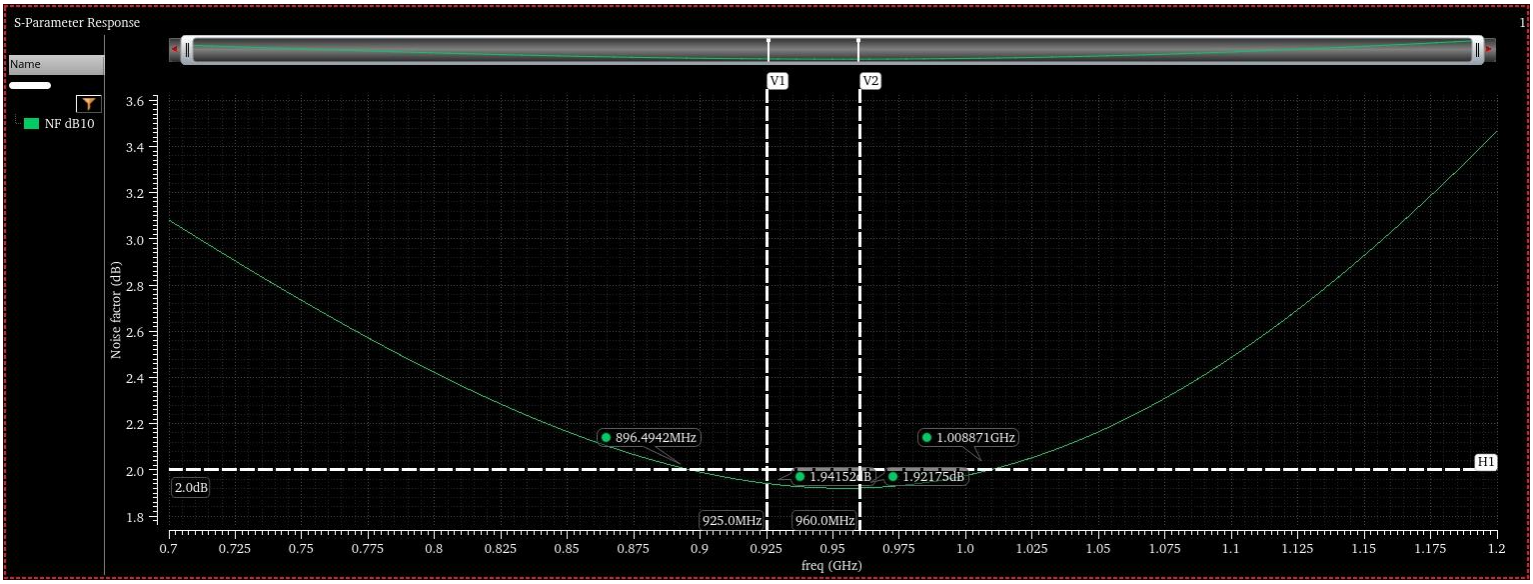
-3dB Gain comes out to be: 19.86dB

From the figure, 3dB bandwidth comes out to be: 295MHz

S11 Plot



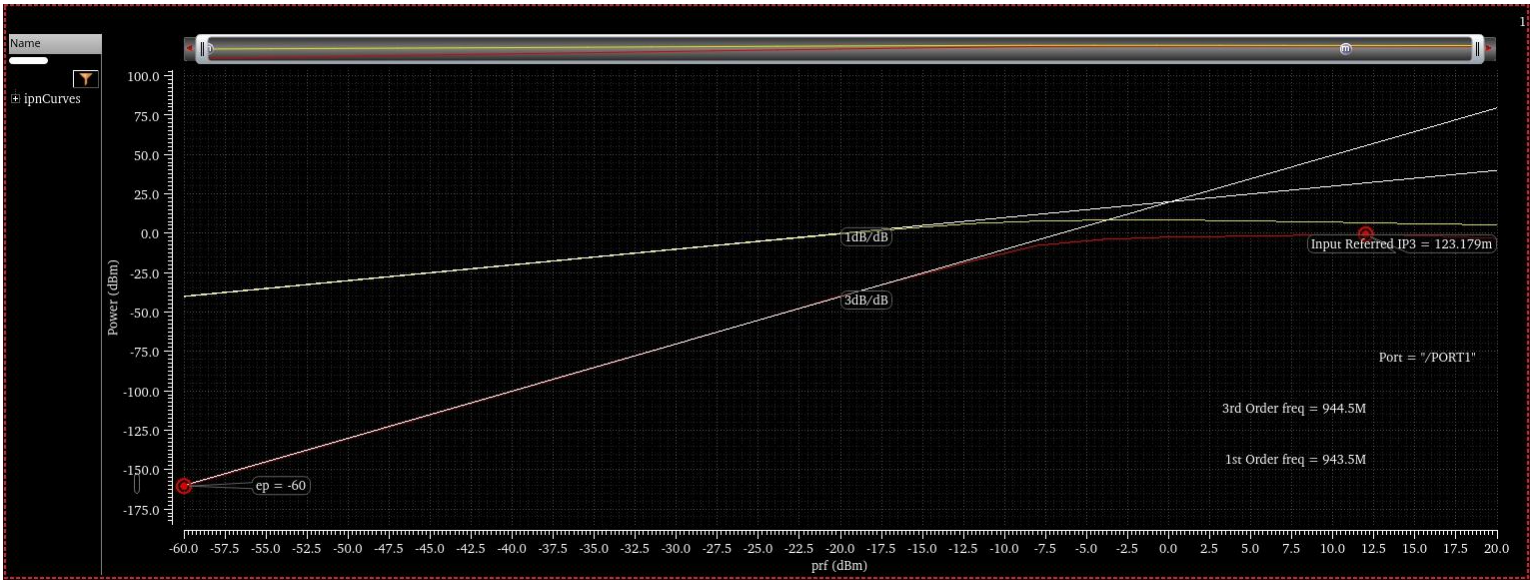
NF Plot



From hand calculations, NF comes out to be: 0.03dB
From the plot, NF comes out to be: 1.92dB

Linearity Plot (IIP3 Computation)

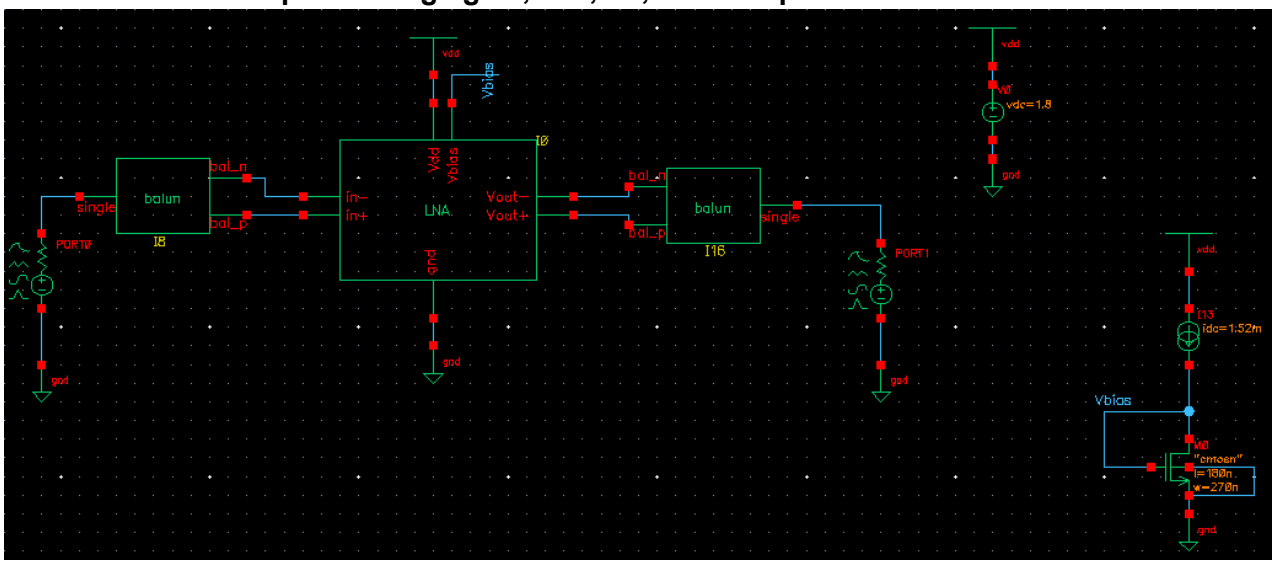
Sweep power from very low powers to very high power and show the extrapolated point



Tones used: 944.5MHz, 943.5MHz
IIP3 point comes out to be: 0.123dBm

LNA Testbench

This testbench is used to compute voltage gain, S11, NF, and IIP3 point.



Comments

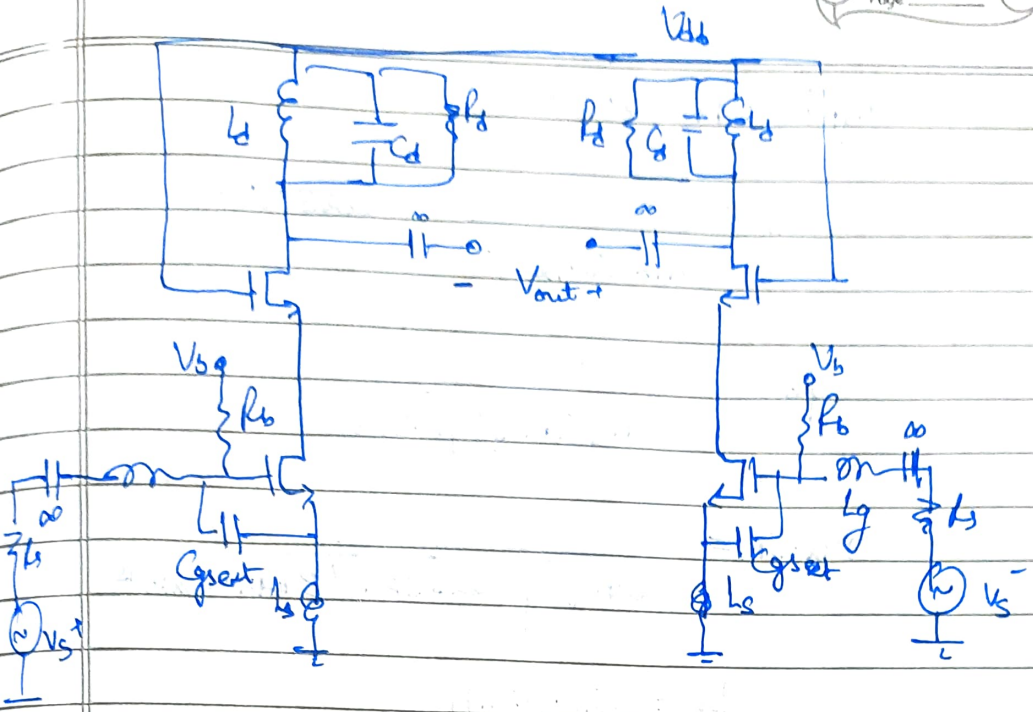
1. First challenge, was to encounter S11 spec, as soon as the input impedance was brought close to 50 Ω, there was a sharp drop in the S11. The S11 dip frequency was adjusted by tweaking the values of Lg and Ls.
2. The Lg happens to behave like a coarse adjustment factor and Ls happens to behave like a fine adjustment factor while trying to obtain Zin = 50 (Im(Zin)=0, Re(Zin)=50) .
3. To obtain the required gain, instead of including Rd in the LNA schematic, the Rd is included as parallel resistance of the Ld. Since value of Ld is pretty high only this gives good Rd at Q=15 and required centre Frequency. So, no external Rd needed to be used to obtain gain.
4. External Cgs capacitor needed to be added in order to reduce the Lg size and therefore meet the NF spec. Since large noise was contributed by the non-ideal inductor Lg due to is ESR.
5. In this event the W was also tweaked of the MOS to get good gm otherwise due to high frequency effects of External Cgs, lower gm was not able to give required gain. Adding a Rd was considered but it added noise and disturbed the NF spec. So, these trade-offs need to be considered while designing.
5. Meeting IIP3 spec was another challenge since the requirement was >0dBm. The biasing current was tweaked to meet that requirement.

Design Procedure

1. First hand calculations were made on a rough scale for the component values. Then a dry run of simulations was done to see the deviation of simulated values from the calculated values.
2. Now one by one approach was taken, first input matching was done tweaking the Lg and Ls values to get the required S11. After achieving that other specs were checked like NF and gain. Since NF was too high an external Cgs was added such that Lg can be brought down so that NF can be reduced and S11 spec can also be met.
3. To meet the Gain spec Ld was tweaked continuously to get the required Rd due to its Q=15.
4. For IIP3 spec the value of bias current has to be continuously tweaked since it controls the gm and its non-linearity as well.

Hand Calculations done for the Project

Hand Calculations



$f_0 = 942.5\ MHz$ $\quad \Delta f_0 = 925 - 960\ MHz$ (Band)

$$Q = \frac{f_0}{\Delta f} = 27$$

$$Q_{in} = \frac{1}{2\omega_0 C_{gs} R_s} = \frac{1}{2\times 2\pi \times 942.5\times 10^6 \times (C_{ext} + C_{gs}) \times 50}$$

Q_{in} must be low for flat band

$Q_{in} \simeq 4$ $\quad (C_{ext} = 540\ fF,\ C_{gs} = 102\ fF)$

$$\text{gain} \Rightarrow \frac{g_m R_D}{2} Q_{in} \Rightarrow \frac{35.1\times 10^{-3} \times 2.66\times 10^5 \times 4}{2}$$

$$= 45.42\ dB$$

$$f_0 = \frac{1}{2\pi\sqrt{L_d C_d}} \Rightarrow 942.5\times 10^6 = \frac{1}{2\pi\sqrt{L_d \times 400\times 10^{-15}}}$$

$$L_d = 71.28\ nH$$

$2\pi f_T L_s = R_s = 50\,\Omega$

$$L_g = \frac{50}{2\pi \times 35.1 \times 10^9} = 225.9\,pH$$

$$f_o = \frac{1}{2\pi\sqrt{(L_g + L_s)(C_{gs} + C_{ext})}}$$

$$342.5M = \frac{1}{2\pi\sqrt{(L_g + 225.9pH)(340f + 102)\times 10^{-15}}}$$

$$L_g = 56.56nH$$

$$F = 1 + \gamma g_m R_s \left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_d}\left(\frac{\omega_o}{\omega_T}\right)^2$$

$$NF = 0.03\,dB$$