External Mode

In the next part of the lab we will be looking at the second technique for debugging a deployed design called External, which was just outlined in the lecture.

If we want to look at several parameters of the design at once, or examine more signals from the IP core, we need more access than the IQ lines alone can provide. External Mode is a mechanism that allows us to define signals in our design that we can control and/or monitor from Simulink while the IP is running on hardware.

Close all the existing models from the previous section and navigate to the External Mode folder:

```
Command Window
>> cd C:\Seminar\Lab3\modem-phy\FixedPoint\external_mode
>>
```

Now open the model "combinedTxRx_ExternalMode.slx":

```
Command Window
>> open combinedTxRx_ExternalMode.slx
```

This model is algorithmically equivalent to the model we have been working with, but the signal mapping in the receiver has been modified to bring out signals of interest. In Figure 9, we have outlined the exterior modifications made to the model which include parameters from the "Configuration Variables" subsystem that we want to tune. For outputs, we are bringing out an IQ signal from the receiver which is connected to a constellation diagram. There is also a "Display" block which provides a running count of received packets.

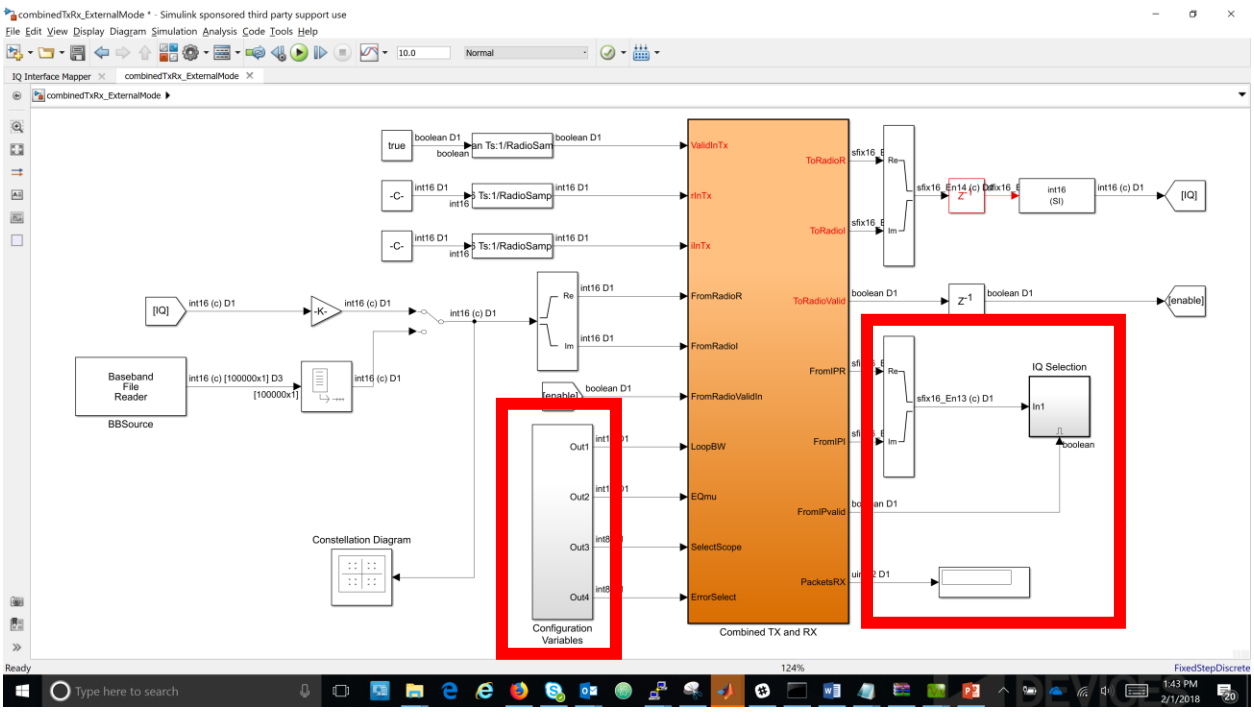


Figure 9

Next, by double-clicking on the "Combined TX and RX" subsystem, we can see the additional control signals mapped into and out of the main receiver block, as shown in Figure 10.

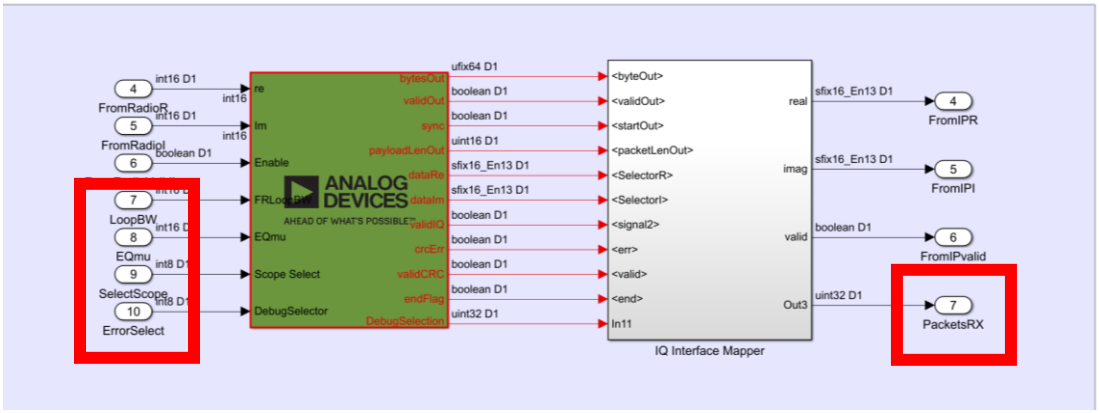
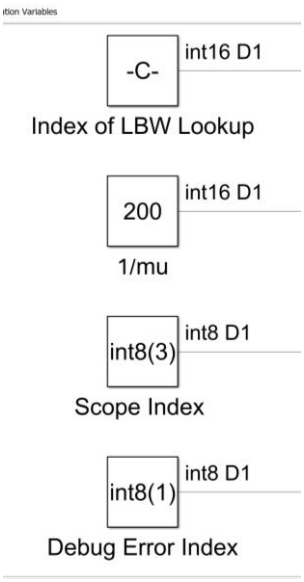


Figure 10

Before we deploy this design, we need to discuss the configuration variables, which are now externally available in Simulink. These are located in the "Configuration Variables" subsystem shown in Figure 9 and shown in more detail below. There are three parameters we want to control from Simulink (the fourth can be ignored for this lab):



- **Index of LBW Lookup**: This parameter controls the Loop Bandwidth of the frequency-recovery loop. Inside the "HDL Receiver" subsystem there is a table of possible values which configures certain gains within that loop. Increasing the index will increase the loop bandwidth.
- **1/mu**: This parameter controls the equalizer step size. The value here is equivalent to 1/stepsize provided. Since registers are provided only as integers this inversion was chosen or simply argument passing.
- **Scope Index**: Within the "HDL Receiver" subsystem there are a series of taps of IQ data from different parts in the receiver chain. These are mux-ed together and that mux is controlled by this index. The different values enable viewing of the IQ data at different stages of the design:
    1. After SRRC
    2. After Timing Recovery
    3. After Frequency Recovery
    4. After Equalizer

Send New Design to Board

As before, we need to update the bitstream on the board. We will load the pre-synthesized bitstream as before:

```
Command Window
>> sendToBoard
## Loading bitstream file
## Rebooting board
## Reboot complete
>>
```

Interface Models

Since these additional interfaces added into the design are not stream based (basically single registers), we connected them to the AXI-Lite bus when we configured the interface in HDL Coder. AXI-Lite is a specifically designed interface for these kinds of lower-speed connections between the ARM and PL. The "hdlworkflow.m" script, which was generated out of "HDL Workflow Advisor", describes this mapping.

To access these new registers from Simulink, the HDL Workflow Advisor produces something called a Software Interface Model – the Zynq processor-system's view of the design. This is essentially a template model for us to fill in with the necessary blocks. The Software Interface Model generated for the "combinedTxRx_ExternalMode.slx" model is shown in Figure 11. It contains IQ data stream blocks for the transceiver (defined as ARM-FPGA Interfaces), and a "Xilinx Zynq AXI Interface" block. This "Xilinx Zynq AXI Interface" is custom and contains the ports we selected as AXI-lite interfaces in the HDL Workflow Advisor. This is what we will use to connect to those new registers. The model itself will appear after the HDL code generation process completes.

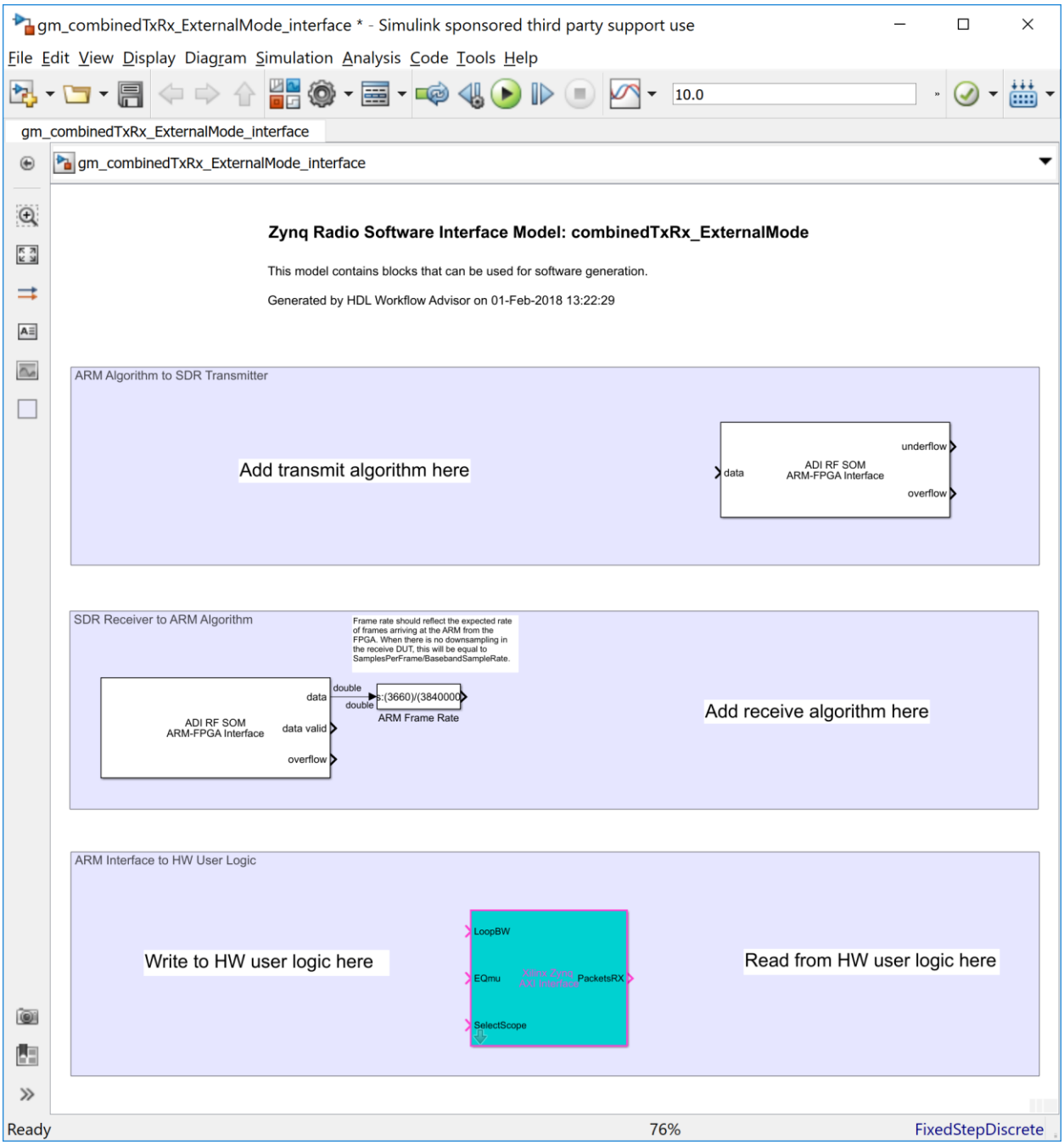


Figure 11

You can examine the software interface model:

Command Window

```
>> open gm_combinedTxRx_ExternalMode_interface.slx
```

Once we have this model we can move our external blocks in “combinedTxRx_ExternalMode.slx” into this template model. The updated model is called “interface_model.slx”. Open this model by running the following:

```
Command Window
>> open interface_model.slx
```

In this model, which is shown in Figure 12, we have also added some dashboard controls for easy tuning of the AXI-lite mapped parameters which are outlined in the figure as well.

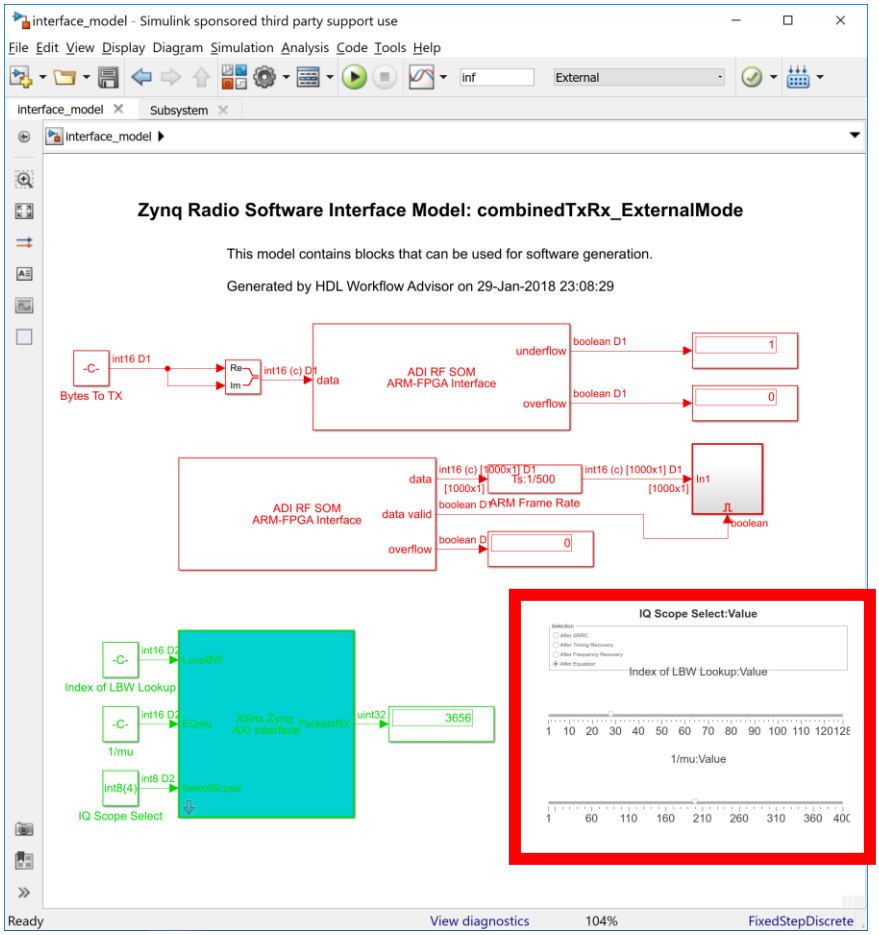


Figure 12

To run this model, select “External” from the pull-down in Simulink, as shown in Figure 13.

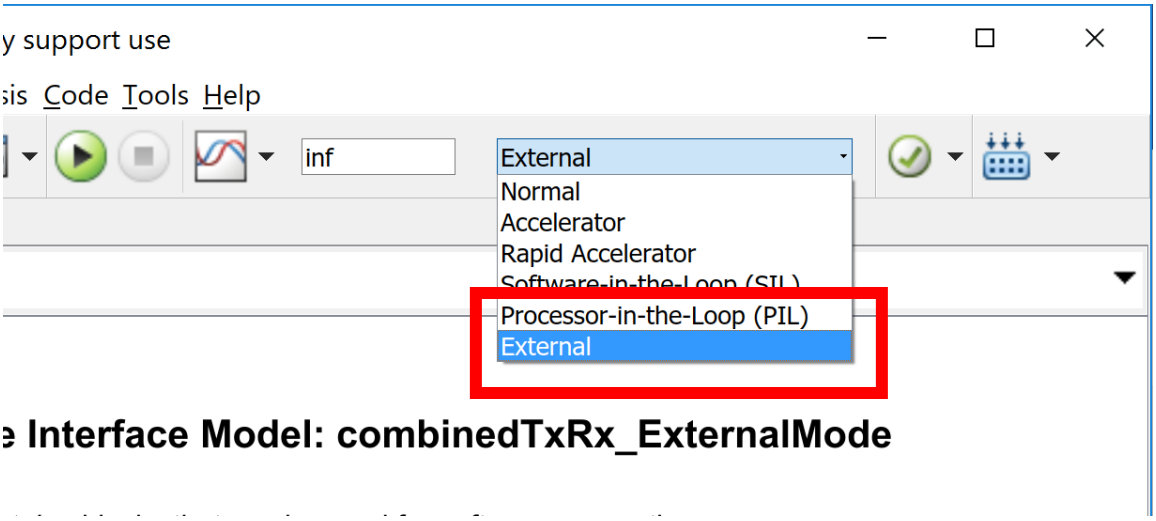


Figure 13

External Mode is a feature of Embedded Coder, and creates a "pipe" between code running on the ARM cores on Zynq and Simulink, enabling read and write access to the Processor System on Zynq. The data visualization and interface console are running in Simulink. Figure 14 highlights the components of our system and shows what elements are running on which platform.

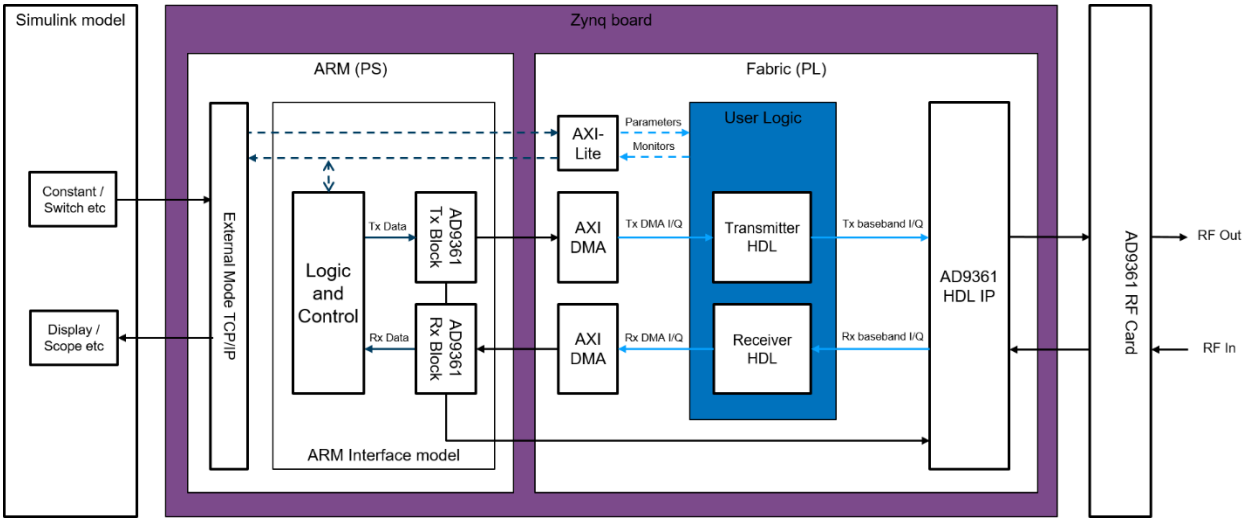
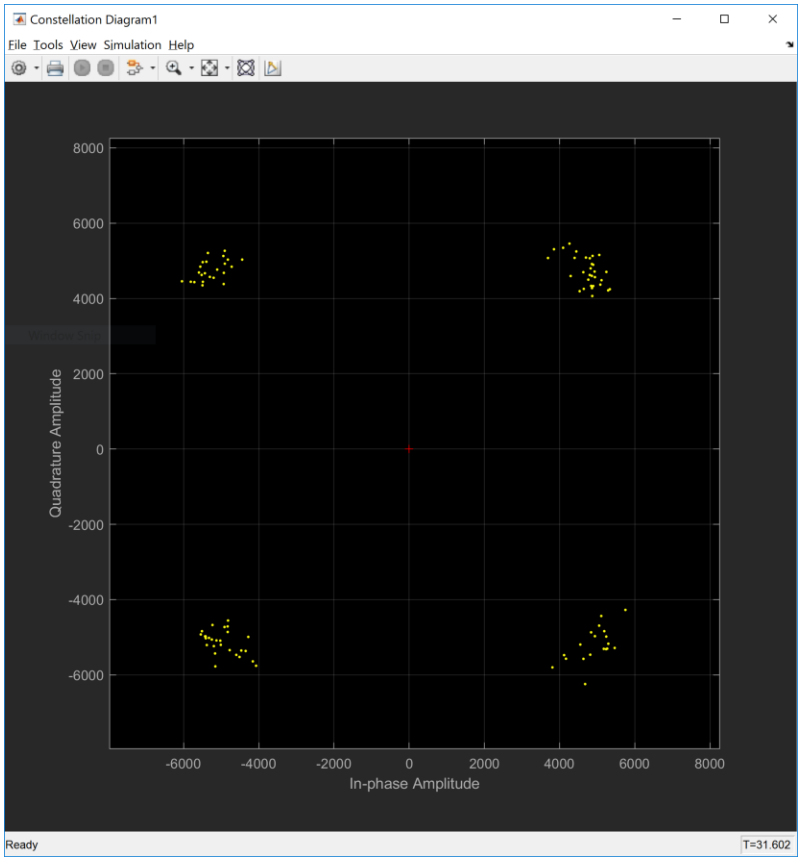


Figure 14

At this point we can run the model. Press the run button  , which will build the ARM code for the model, deploy it to the target, and start execution. It may take a few seconds for it to complete this process. When the model is running you should see data appear on a constellation plot:



Since we now have access to the model's registers we can begin to tune system parameters. To visualize these effects do the following:

1. On the Scope Index select "After Frequency Recovery". You should see a stable constellation. Now change the Loop Bandwidth values. What do you observe?
2. On the Scope Index select "After Equalization". You should see a jumping constellation. Now change the 1/mu values. What do you observe?
3. On the Scope Index select "After Timing recovery". On the "Carrier Offset" slider, make this value non-zero. What happens to the constellation? Now select "After Frequency Recovery" on the scope index. Does this help the constellation? Increase the slider to a large value. What happens to the constellation?