EXP3: HALF ADDER AND HALF SUBTRACTOR

AIM:

To design a half adder and half subtractor circuit and verify its truth table in Quartus using Verilog programming.

Equipments Required:

Hardware – PCs, Cyclone II , USB flasher

Software – Quartus prime

Theory:

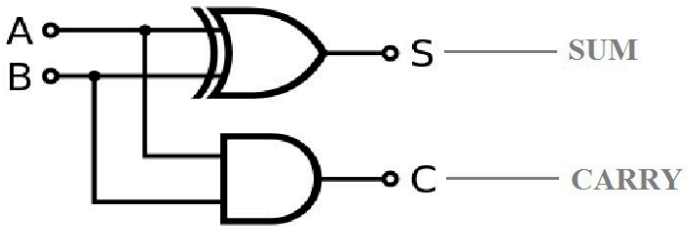
Adders are digital circuits that carry out the addition of numbers.

Half Adder

Half adder is a combinational circuit that performs simple addition of two binary numbers. The input variables designate the augend and addend bits; the output variables produce the sum and carry. It is necessary to specify two output variables because the result may consist of two binary digits.

Sum = A'B+AB' =A ⊕ B Carry = AB

Logic diagram:



Truth table:

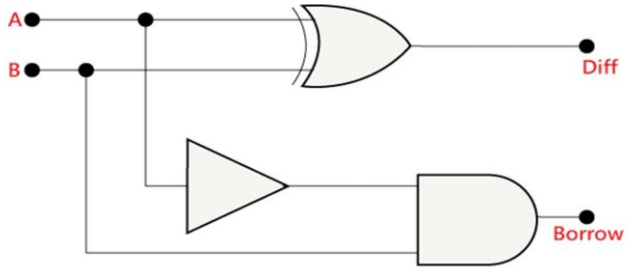
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Subtractor

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). To perform x - y, we have to check the relative magnitudes of x and y. If x ;;, y, we have three possibilities: 0 - 0 = 0, 1 - 0 = 1, and 1 - I = 0. The result is called the difference bit. If x < y, we have 0 - I, and it is necessary to borrow a 1 from the next higher stage. The I borrowed from the next higher stage adds 2 to the minuend bit, just as in the decimal system a borrow adds 10 to a minuend digit. With the minuend equal to 2, the difference becomes 2 - I = 1. The half-subtractor needs two outputs. One output generates the difference and will be designated by the symbol D. The second output, designated B for borrow, generates the binary signal that informs the next stage that a I has been borrowed.

Diff = A'B+AB' =A ⊕ B Borrow = A'B

Logic diagram:



Truth table:

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Procedure

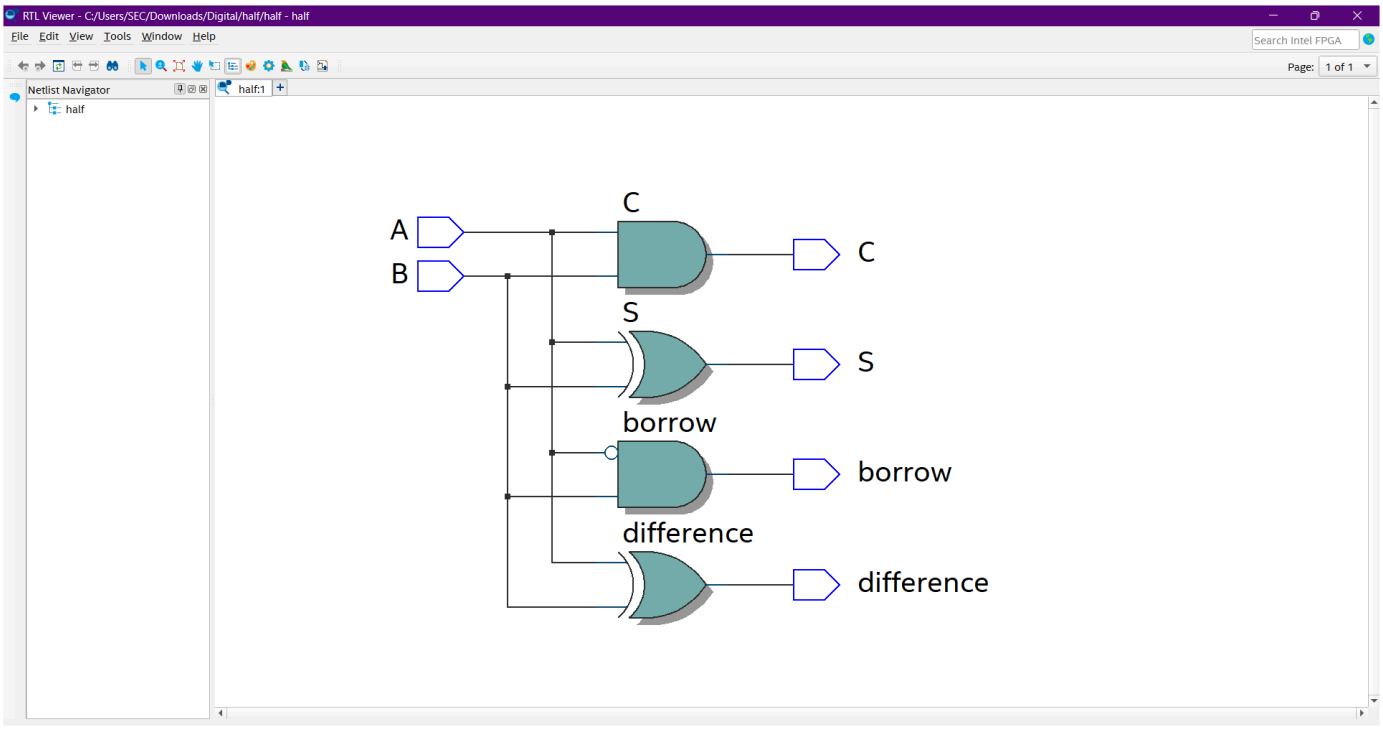
1. Type the program in Quartus software.
2. Compile and run the program.
3. Generate the RTL schematic and save the logic diagram.
4. Create nodes for inputs and outputs to generate the timing diagram.
5. For different input combinations generate the timing diagram.

Program:

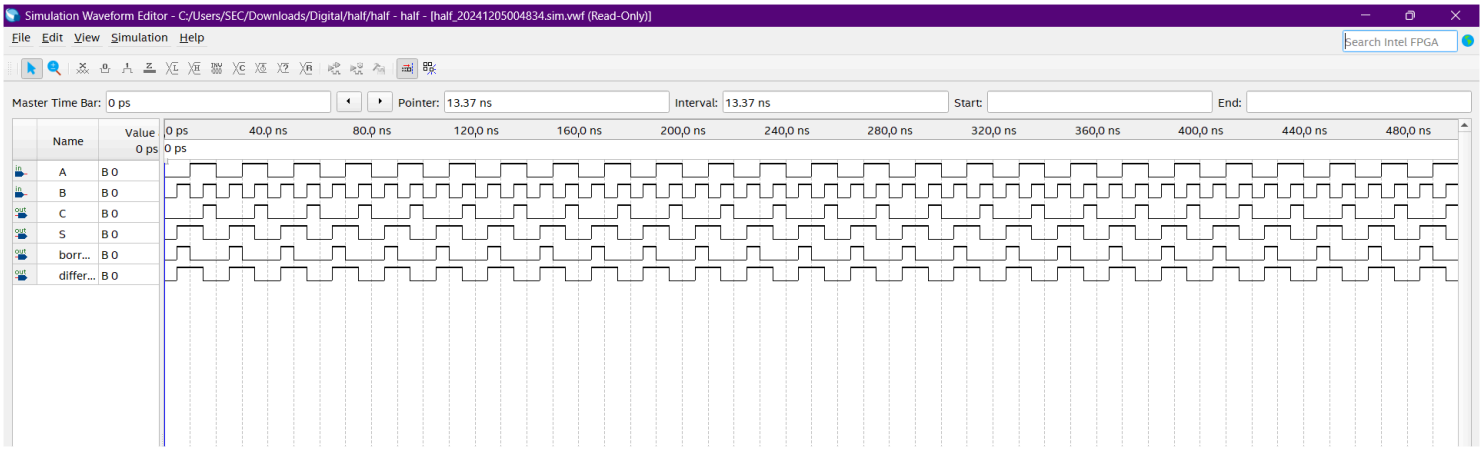
Home | half.v | Compilation Report - half

```
1   module half(A, B, S, C, difference, borrow);
2       input A, B;
3       output S, C, difference, borrow;
4
5       // Half Adder Logic
6       assign S = A ^ B; // Sum
7       assign C = A & B; // Carry
8
9       // Half Subtractor Logic
10      assign difference = A ^ B; // Difference
11      assign borrow = ~A & B;    // Borrow
12  endmodule
```

RTL Schematic:



Output/TIMING Waveform:



Result:

The design of both the half adder and half subtractor circuits in Quartus II using Verilog has been successfully completed. The truth table for both circuits has been verified through simulation, demonstrating accurate functionality and alignment with the expected truth table values for all input combinations.

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