EXP6 :SERIAL IN SERIAL OUT SHIFT REGISTER

AIM: To implement SISO Shift Register using verilog and validating their

functionality
using their functional tables

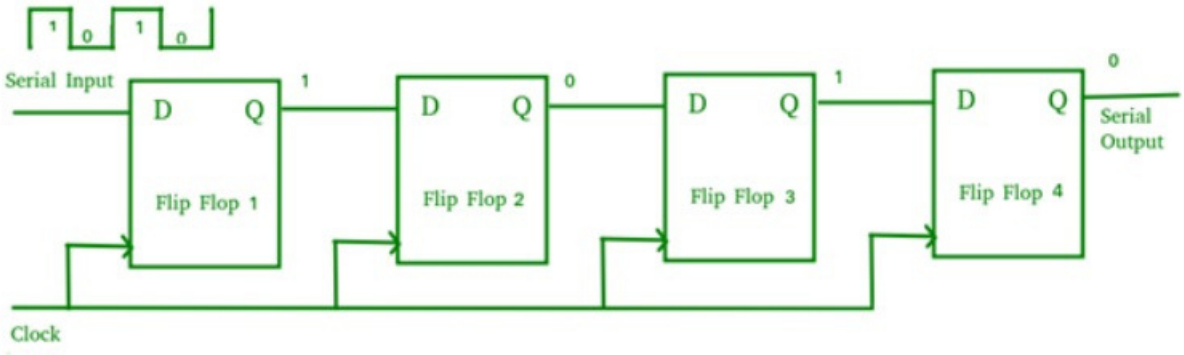
SOFTWARE REQUIRED:
Quartus prime

THEORY:

SISO shift Register

A Serial-In Serial-Out shift register is a sequential logic circuit that allows data to be shifted in and out one bit at a time in a serial manner. It consists of a cascade of flip-flops connected in series, forming a chain. The input data is applied to the first flip-flop in the chain, and as the clock pulses, the data propagates through the flip-flops, ultimately appearing at the output.

The logic circuit provided below demonstrates a serial-in serial-out (SISO) shift register. It comprises four D flip-flops that are interconnected in a sequential manner. These flip-flops operate synchronously with one another, as they all receive the same clock signal.



The synchronous nature of the flip-flops ensures that the shifting of data occurs in a coordinated manner. When the clock signal rises, the input data is sampled and stored in the first flip-flop. On subsequent clock pulses, the stored data propagates through the flip-flops, moving from one flip-flop to the next. Each D flip-flop in the circuit has a Data (D) input, a Clock (CLK) input, and an output (Q). The D input represents the data to be loaded into the flip-flop, while the CLK input is connected to the common clock signal. The output (Q) of each flip-flop is connected to the D input of the next flip-flop, forming a cascade.

Procedure:

1. Type the program in Quartus software.

2. Compile and run the program.

3. Generate the RTL schematic and save the logic diagram.

4. Create nodes for inputs and outputs to generate the timing diagram.

5. For different input combinations generate the timing diagram.

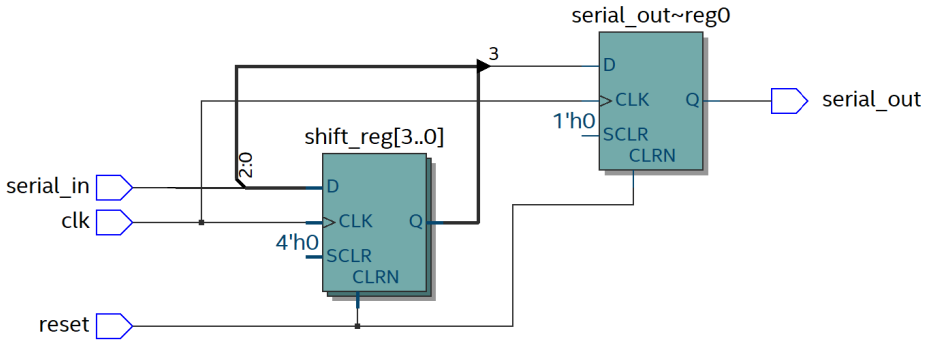
PROGRAM:

```
module siso (
    input wire clk,          // Clock input
    input wire reset,        // Reset input (active high)
    input wire serial_in,    // Serial input
    output reg serial_out    // Serial output
);
    // Internal 4-bit register to hold the data
    reg [3:0] shift_reg;

    always @(posedge clk or posedge reset) begin
        if (reset) begin
            // Reset the shift register to 0
            shift_reg <= 4'b0000;
            serial_out <= 1'b0;
        end else begin
            // Shift data to the left, bringing in serial_in
            shift_reg <= {shift_reg[2:0], serial_in};
            serial_out <= shift_reg[3];  // Output the MSB
        end
    end
endmodule

```

RTL LOGIC FOR SISO Shift Register:



TIMING DIGRAMS FOR SISO Shift Register:

RESULTS:

The SISO (Serial-In, Serial-Out) Shift Register implemented in Verilog has been successfully completed. Its functionality has been validated by comparing its output behavior with the expected values from the functional table. Simulation results confirm that the SISO Shift Register operates correctly, shifting input data serially into the register and shifting out the data sequentially as per the specified shift direction, as indicated by its functional table.

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