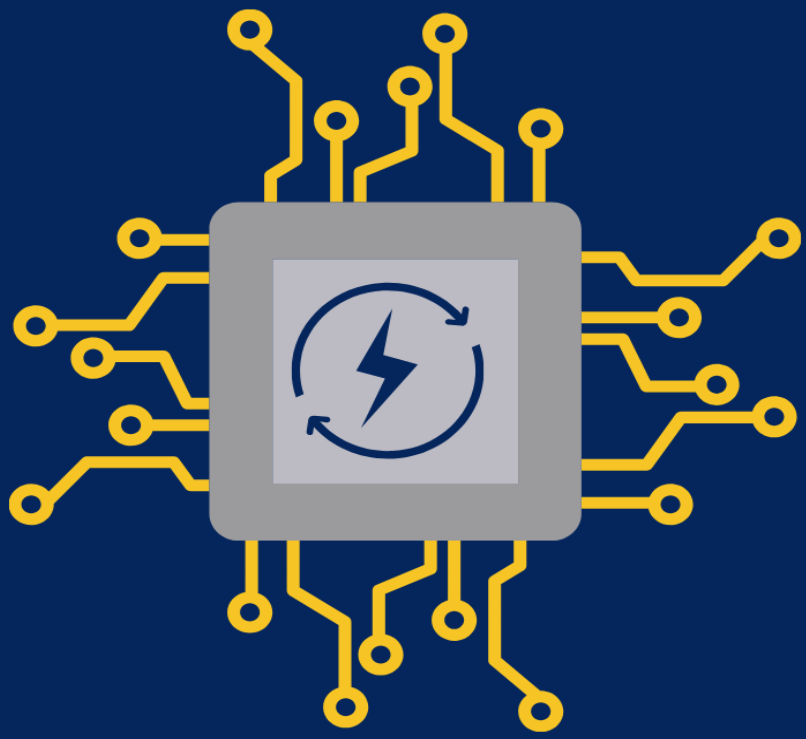
INTER IIT TECH MEET 12.0

19th to 22nd DECEMBER 2023

JLR CHIPLET CHALLENGE



MID EVALUATION REPORT

TEAM - 40

CONTENT

1.1 Motivation of Problem:

Electronic components entered the automotive area in the 1950s and 1960s, since then, electronics have spread into all relevant areas of automotive transportation.
Today, electronics are responsible for nearly 40% of a new car's total cost, and along with software, up to 90% of all innovations in a modern car. (Ref: Chasing the Software-Defined Dream Car | BCG)

With the surge of software-driven applications in the modern automotive sector, there is a noticeable shift in the industry's priorities, transitioning from hardware-centric approaches to software-centric ones. This shift has led to the industry's evolution toward single centralized compute stacks within the electrical and electronic (E/E) architectures of cars, and at the heart of this transformation lies the crucial role of the System-on-Chip (SoC).

SoCs offer various advantages that enable advanced features, enhance vehicle performance, improve safety, and contribute to a more connected and efficient driving experience in the modern automotive industry.

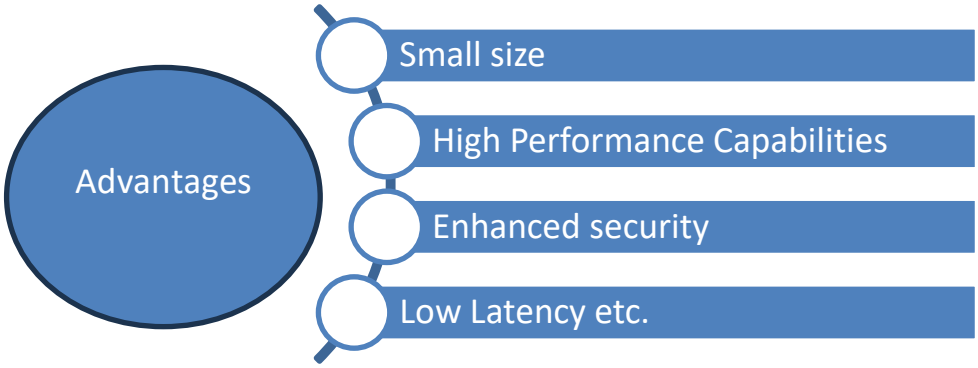


Figure 1: Advantages of System on Chip (SoC)

The semiconductor industry has evolved according to **Moore's law**. Transistors have gotten smaller, allowing more of them to fit on ICs, thus exponentially increasing compute capability. However, Moore's Law has not been a constant trend over time. In the early years, the doubling of transistor count was consistent, with ICs becoming smaller and more powerful a high rate. The physical limitations of silicon have made it increasingly difficult to continue shrinking transistors without compromising their performance and reliability. So, it is unlikely that Moore's Law will continue in its original form. However, the underlying principles of Moore's Law are still driving the advancement of semiconductor technology.
In recent years, the focus has shifted from simply doubling transistor count to optimizing the overall performance of ICs.

The growing demand for advanced features in electronic devices has led to larger and more complex SoCs, but this approach faces several limitations.

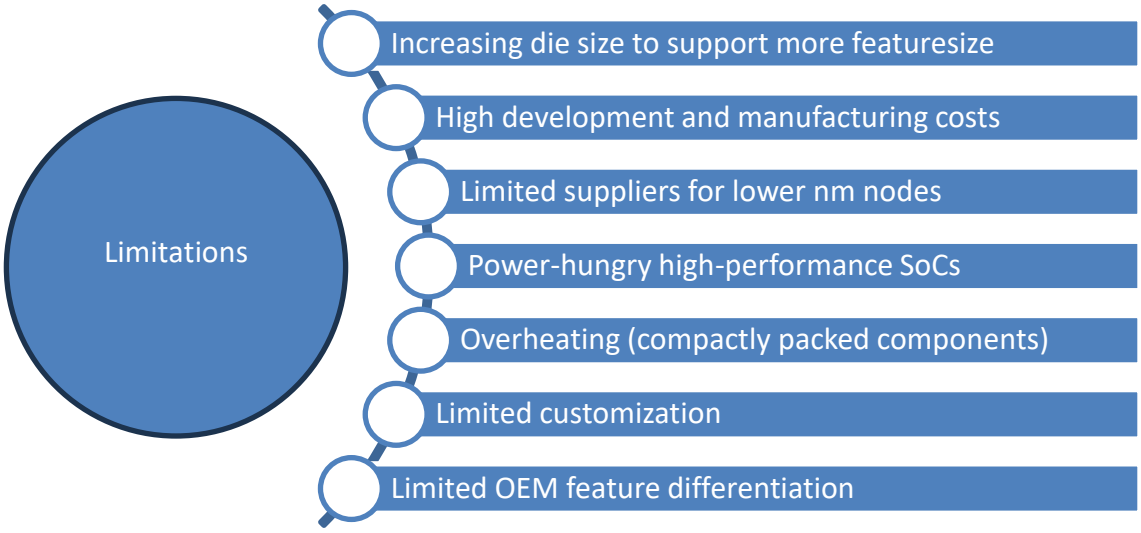


Figure 2: Limitations in System on Chip (SoC)

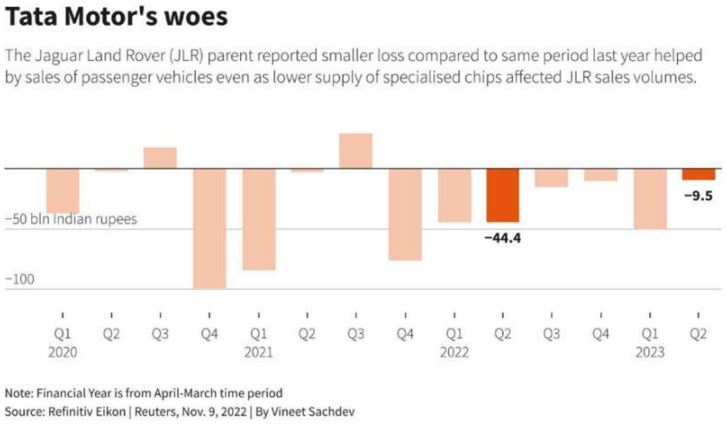
The motivation for exploring chiplet technology stems from the need to address these limitations and open up new possibilities in the automotive industry. Chiplets can offer solutions by breaking down the system-on-a-chip into modular components, enabling customization, cost savings, and enhanced reliability, aligning with the unique requirements and challenges of the automotive sector. This innovation has the potential to revolutionize the automotive industry, leading to more energy-efficient systems, shorter development cycles, and greater flexibility in creating purpose-built vehicles for various applications.

1.2 WHY SHOULD JLR ADOPT CHIPLET TECHNOLOGY?

1.2.1 MARKET ANALYSIS-

1. **To reduce the dependency on a single company for buying the SOCs:** While making chiplets, the company could procure different processors from different companies so as to reduce their dependence on any single company as chiplet based systems allow heterogeneous integration that involves combining chiplets, each manufactured using a different process node, substrate material or size, into a single package.

   Why does this make more sense for JLR- JLR's profit after tax went into loss due to chip shortages in the market and it was only after 2022, that their profit after tax turned positive. Therefore, being dependent on a single chip manufacturer could worsen the situation of a car manufacturer and therefore they should diversify their chip procurement process. JLR delivered on its targets and attained positive free cash flow and profitability in Q4 as chip supply constraints continued to ease.



As it can be seen from the figure, JLR has been continuously in loss for the past few quarters because of chip shortages.

Figure3:Reference:https://www.jaguarlandrover.com/news/2023/05/jlr-delivers-significantly-improved-revenue-profit-and-free-cash-flow-quarter

Here's how the finances of the company got better after the chip supply improved–

a) Revenues in Q-4 FY23 of £7.1 billion, which were up by 49% (y-o-y); Full year revenue for FY23 of £22.8 billion, which were up by 25% vs FY22 as chip supply improved further
b) Sales in Q-4 were 94,649 units, which were up by 24% (y-o-y); Full year wholesales of 321,362 which were up by 9% vs FY22
c) Free cash flow in Q-4 FY23 of £815 million resulting in £1.3 billion in H2 FY23 and £521 million for the full year.

2. **To bring differentiability into their product:** The companies which make SOCs are usually in partnership with various other automotive companies and hence the SOC company sells the same product to various companies. So, it becomes difficult for a company like JLR to bring changes specific to their product if they want to. To explain this through an example, Nvidia Drive Hyperion platform is used by JLR and Mercedes and various other companies which makes it becomes difficult for any of these companies to bring any change into their car when talking in ADAS's perspective.

   To sum it up, it becomes easy for a company to bring distinction between their and their competitor's product by using the chiplet technology.

3. **Reduced Time-to-Market:** Heterogeneous integration can accelerate product development because new chiplets with most advanced technologies can be integrated into the existing design with older nodes without the need to redesign the entire system, thus, JLR can quickly adapt to changing market demands leading to faster development cycles.

   Just to give an example, Nvidia took almost 4 years to develop ORIN SoC which it uses in its Drive Hyperion platform.
   On the other hand, chiplets do not take that much time to be developed as they do not have to be necessarily made from scratch. Just to give a perspective, chiplets can be customizable designed for the customers in a matter of 3 to 4 months.
   In short , the time required for Research and Development can be reduced by using chiplets instead of SoCs.

1.2.2 TECHNICAL ANALYSIS-

2. **Scalability and Customization:** Chiplets are like LEGO building blocks where individual components can be replaced whenever needed, thus, system's performance, capabilities, or size can be flexibly and efficiently

adjusted by adding or removing chiplets. For example, the technology behind GPUs gets frequently updated. So, they can be replaced in a chiplet as per the requirement which is not the case with a SOC.

3. **High Performance Compute (HPC):** Multiple chiplets optimized for specific tasks, such as graphics processing, artificial intelligence (AI) acceleration, or memory management, combined with each-other in a single package, can work in parallel, dividing the overall computational workload to deliver higher performance in their respective domains, leading to more efficient computation required for technologies like ADAS, communication, and entertainment functions of tomorrow's vehicles.

4. **Yield Improvement**: In chiplets, a defect in one chiplet does not necessarily impact the entire system. SoCs are more complex and contain numerous integrated components on a single chip. A defect in any part of an SoC can potentially render the entire chip unusable, leading to lower yield compared to chiplets. Moreover, Chiplets are less complex to manufacture than large monolithic chips and can be tested before assembly.

5. **Energy Efficient:** Using advanced chiplet packaging technologies, such as 3D stacking and chiplet-based architectures that allow use of already optimized chiplets, combined with the sharing of resources such as wiring and cooling infrastructure leads to enhanced thermal and power management.

6. **Cost Efficient:** Mix and match of process nodes, reduced development and verification costs by using already tested and verified chiplets, yield improvement, scalability and customization could increase cost efficiency.

Summary: JLR announced ReImagine Strategy in 2021 which aims to invest £15bn over five years in JLR's electrification and digital transformation and also Jaguar is set to be completely electrified by 2025. This further makes the set of reasons described above become even more important for Jaguar as the number of SOCs in EVs are more than that in a combustion engine car because of power electronics systems, battery management systems etc.

Chiplet Systems involve advanced packaging methods such as 2.5D or 3D, which ensure high-speed low-latency communication between the single Chiplets. Compared with traditional packaging, the manufacturing costs of these are significantly higher. The lower production costs are partly offset by higher packaging costs.

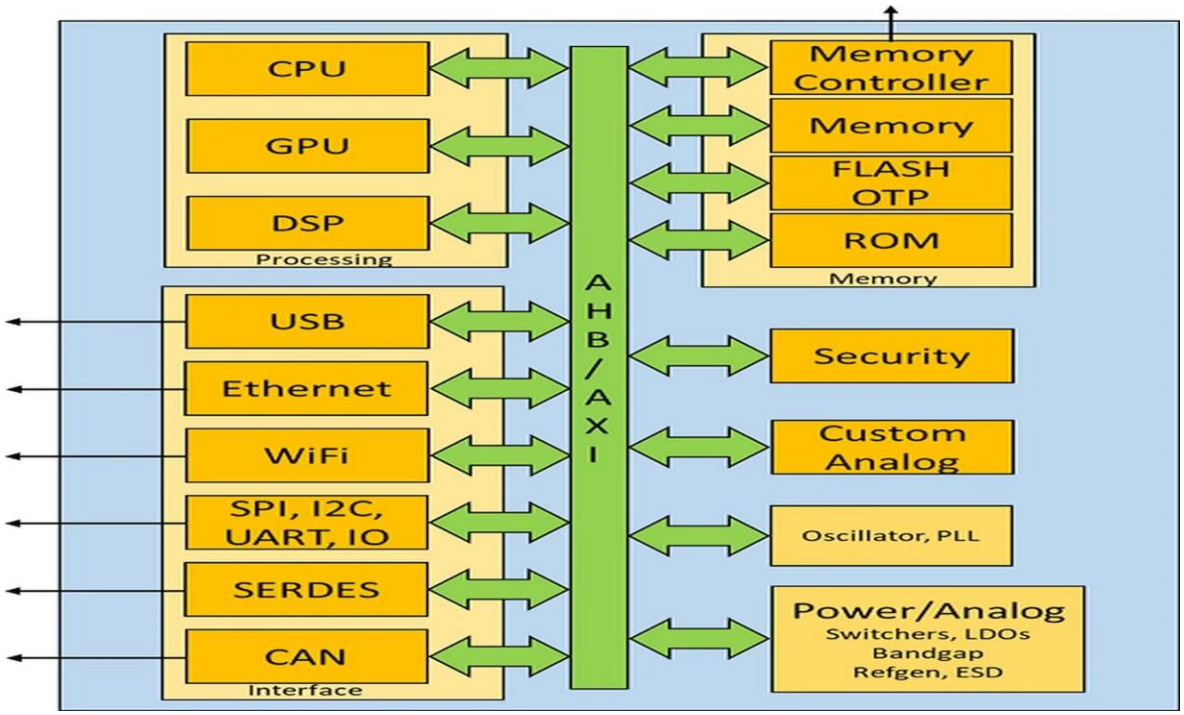


Figure 4: Typical SoC Block Diagram

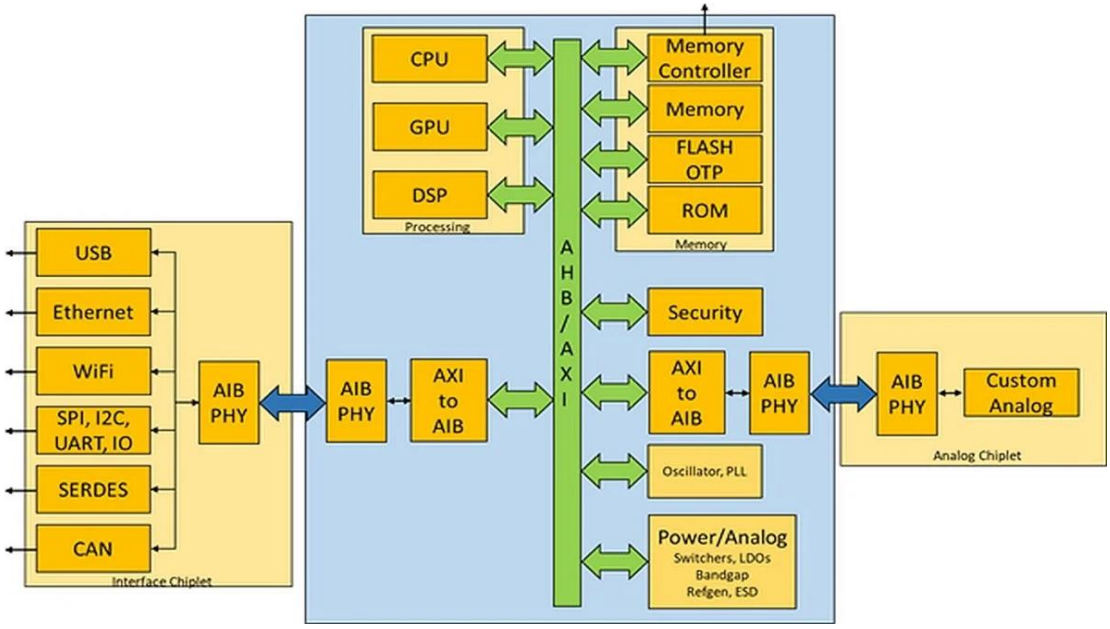


Figure 5: SoC Partitioned into Chiplets

Figure 5 depicts three chiplets interconnected by Advanced Interface Bus (AIB) - Intel's promising standard interface for chiplet based systems.

1.3 Application or components in car where use of chiplet will add value:

Chiplets for Autonomous Vehicles (AVs):

Autonomous vehicles (AVs) use technology to partially or entirely replace the human driver in navigating a vehicle from an origin to a destination while avoiding road hazards and responding to traffic conditions.

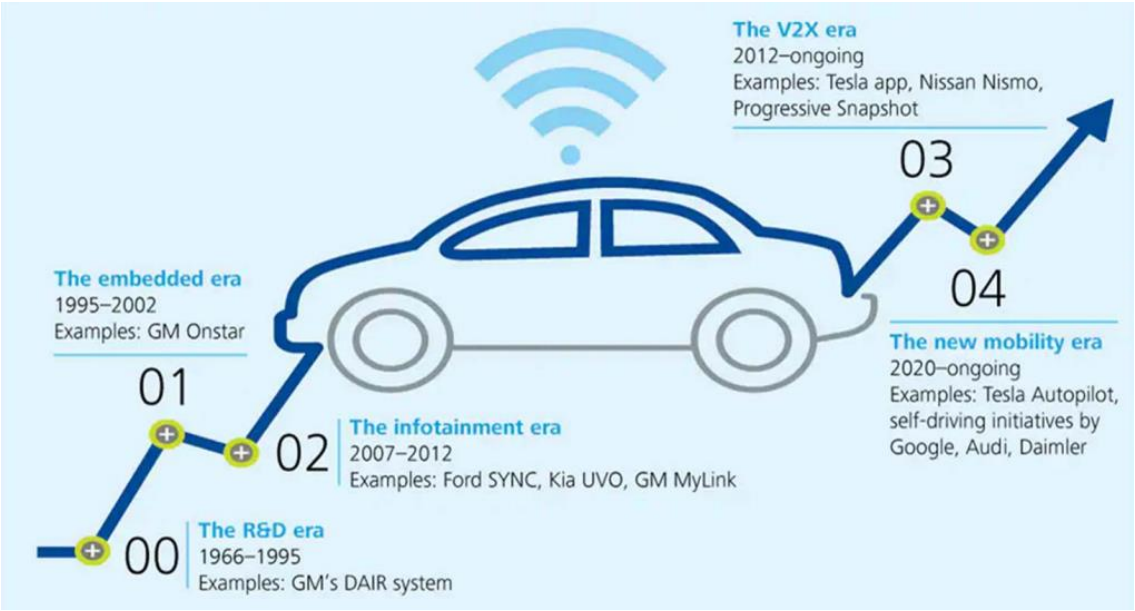


Figure: Evolution of the Connected Car
Source: Deloitte University Press | DUPress.com

1.3.1 Application 1: 3D interconnect based Chiplets for computation in ADAS systems

Chiplet architectures for AI could be of great benefit in automotive. At the moment the premium automotive market volumes are not as significant as the mid-range. Therefore, if AI inference accelerators were carved out as separate logic blocks on silicon, the semiconductor manufacturer could spin multiple variants of mostly the same SoC with a greater level of AI compute.

The architectures could have a significant role to play in advanced driver assistance systems (ADAS) – the fastest growing segment in the automotive market as the industry continues on the road to fully self-driving vehicles.

Essentially, ADAS is a spectrum of autonomy that leads to full driving automation at Level Five.

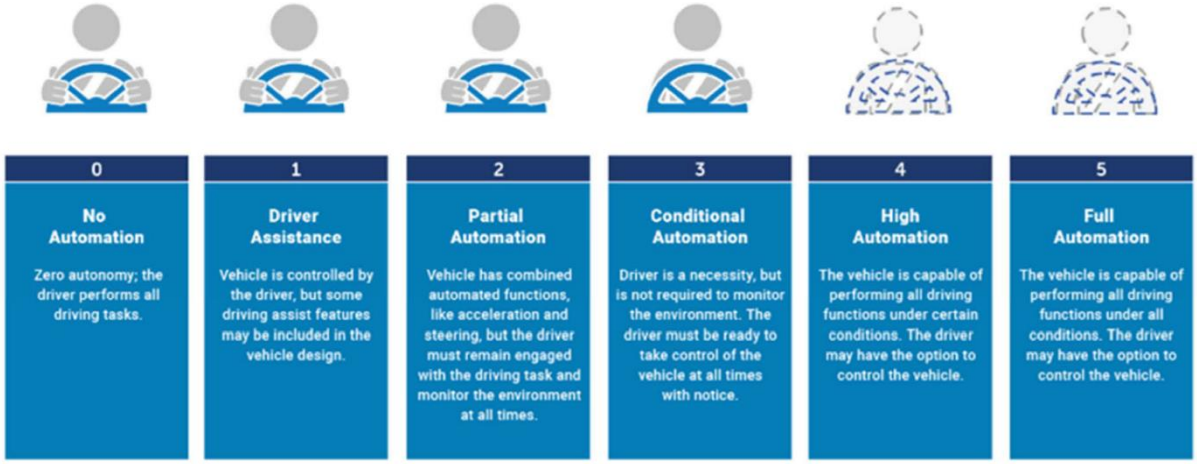
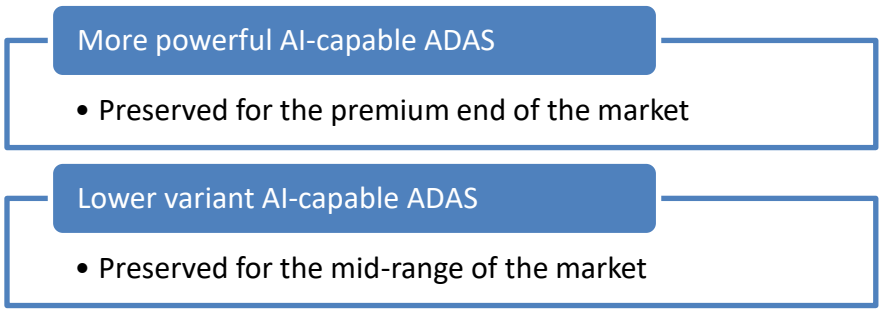


Figure: Autonomous Driving Levels
Source: eps.ieee.org

Currently, the compute that provides auto-pilot functionality sits on silicon of the expensive GPU (General processor unit) or TPU (Tensor processor unit) variety. It's therefore the preserve of the premium end of the market. A partitioning and modular chip strategy, allowing the AI inference accelerator to be split out and variants developed, offers a way for the premium and mid-range OEM to offer more and more AI-based ADAS features incrementally. This means they can create value and improve margins.



The **Nvidia Drive Orin** is an example of chiplet-based AI processor which is being used by multiple automobile manufacturers, including Jaguar Land Rover, Volvo, and Geely, in a number of ADAS and autonomous driving applications. The processor is able to deliver a performance upto 17 TOPS, which is helps meet the demanding ADAS and autonomous driving applications.

It could be a smart idea to go to 3D interconnect-based technology, even if JLR just teamed with Nvidia to strengthen their ADAS system and is aiming to use the NVIDIA Drive Hyperion platform with chiplet based SoCs like the Drive Orin, which is based on 2.5D interconnect technology.

Among all the car manufacturers today who have launched vehicles with level 4 ADAS, none are using **3D chiplet interconnect technology**.

The proposed NVIDIA Drive promises upto 254 TOPs and 200GB/s of memory bandwidth which is better compared to that provided by other chips in the segment like Intel's Mobileye EyeQ chips. Hence, JLR might bring a revolution in Level 4 ADAS systems with new 3D architecture based chiplet technology.

Some advantages of 3D architecture based chiplet technology:

- Greater bandwidth, reduced latency, increased flexibility, and a smaller footprint are just a few of the benefits that 3D interconnect technology offers over 2.5D, and these attributes are particularly appealing for automotive applications.
- We are aware that although 3D interconnect technology costs more than 2.5D, it offers advantages over the latter. But looking ahead, it's clear that more businesses are investigating 3D technology, and that it will only get more advanced and affordable.
- The race for developing 3D chiplet packaging has begun. AMD has already developed next generation packaging similar to 3D using TSMC's copper hybrid bonding technology.

1.3.2 Application 2: Chiplet-based Sensor Fusion for Radar and V2X Communication

RADAR

RADAR stands for RAdio Detection And Ranging. The development of several parallel mega trends like internet ubiquity, sensor fusion, compute power advances, mobility, data analytics drove a multitude of applications in the automobile that utilize Radar technology. It is used in detecting the obstacles that occur in the pathways, Collision Warning Systems, Blind Spot Detection and Proximity Sensing.

In current deployment, radar modules consist of a processor chip, RF radar sensor, analog drivers, and antennas, assembled on a PCB and enclosed in a module for mounting in automobiles. Depending on the requirements, the radar sensor can be a one-chip unit combining transmit and receive functions and include analog functions, or it can be a separate chip for each function.

For now, the adoption of flip-chip or wafer-level packaging is used as the platform of choice, depending on the application, from major electronics suppliers such as NXP, Texas Instruments, ST Microelectronics. mmWave RF technology is now the mainstream for automotive radar.

This system can be upgraded to **3D technology** integrated with the high-density fan-out and flip-chip technologies (FCCSP). Flip-chip structures have an advantage in enabling antenna-stacked-on-chip configuration in a cost-effective manner and hence shrinking the package size/board footprint compared to a conventional side-by-side antenna-in-package (AiP) configuration. Antenna in package (AiP) has the antenna built into the package and radiates the signal coming from the RFIC to/from the environment directly.

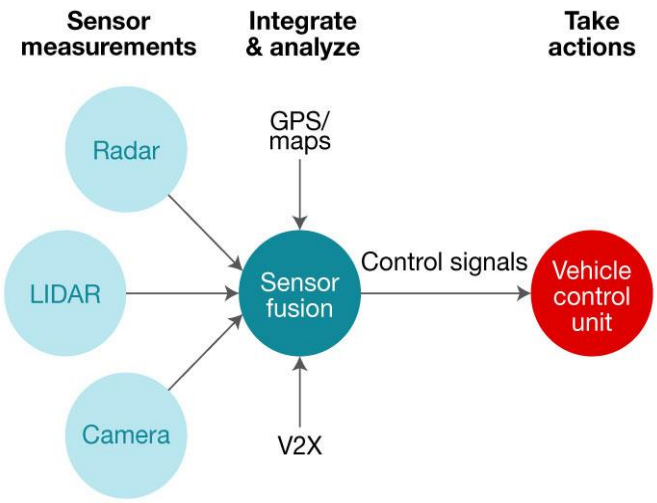


Figure: Sensor fusion box
Source: Texas Instruments (TI)

Vehicle to everything (V2X) Communication

The successful implementation of an autonomous-driving system relies on the ability to make reliable and prompt decisions based on the data collected. Additionally, the reliability and accuracy of the data obtained from these technologies must be continuously monitored and evaluated to ensure the optimal functioning of the autonomous-driving system. So, developing and maintaining the V2X system is a complex task requiring significant technical expertise.

For the V2X system to operate efficiently, it must connect with multiple components through wireless channels that rely on new and untested technologies. To develop a successful V2X system, wireless-communication protocols, ML algorithms and sensors must be combined and prioritized within a single structure. Hence is best suited for using the chiplet technology by deploying advanced packaging and communication protocols.

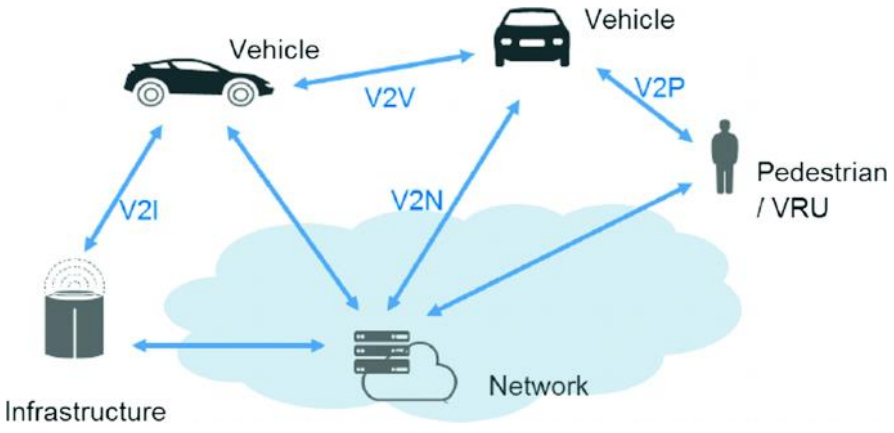


Figure: V2X Communication
Source: link.springer.com

Communication latency, transmission range, transmission throughput, and power consumption are a few important challenges that need to be considered while choosing any of those technologies for V2X.

For now, the following points have been implemented on this V2X –

1. A LoRa architecture is proposed for V2X communication to ensure higher reliability by smooth data handover from one RSU to another.
2. A Device-to-Device (D2D) based approach is considered in the architecture which improves the latency by enabling direct V2V and V2X communication which is missing in the literature of LoRa V2X.
3. RSSI-based algorithms are proposed for V2V and V2I communication that support good link quality at a higher speed of the vehicles which is not addressed yet by the state-of-the-art literature for LoRa V2X.
4. Prototypes of the On-Board Units (OBU) and Road-Side-Units (RSU) are designed with low power microcontrollers to maintain portability and to achieve better energy efficiency.
5. The performance of the architecture is evaluated under practical scenarios with vehicles on the move at different speeds which is not addressed in the relevant literature.
6. Two main components of the proposed architecture are OBU and RSU. As OBUs are integrated into vehicles to collect and send vehicle data to other vehicles and infrastructures, they are equipped with sensors and transceivers.

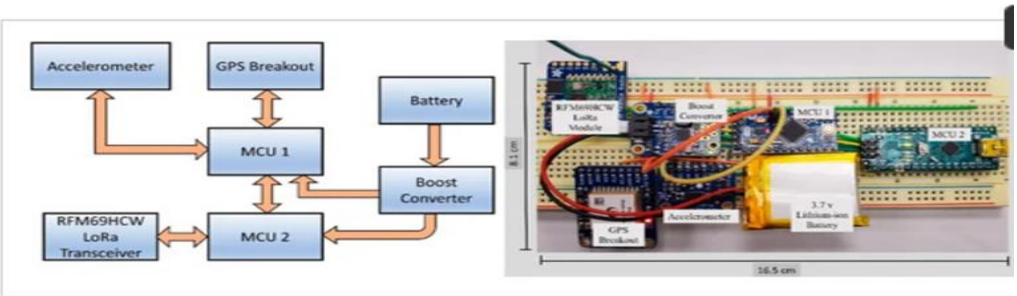


Figure 7: Artitecture and protytpe of OBU
Source: mdpi.com

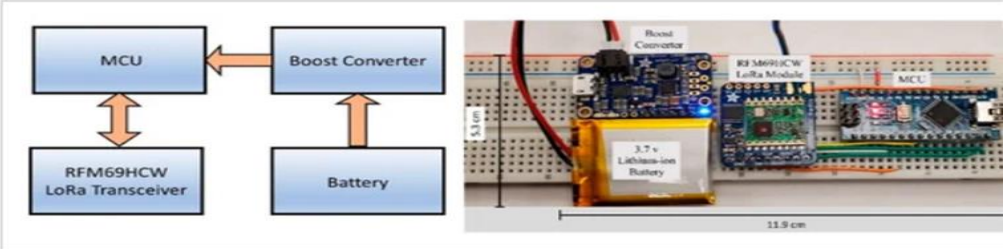


Figure 8: Artitecture and protytpe of RSU
Source: mdpi.com

1.3.3 Existing chiplet based systems applications:

Some specific examples of how chiplet technology is being used in automobiles to increase efficiency are as follows:

Nvidia Drive Orin	Chiplet-based AI processor	▪ ADAS and autonomous driving applications ▪ Used by multiple automobile manufacturers, including Jaguar Land Rover, Volvo, and Geely ▪ Processor is able to deliver a performance upto 17 TOPS, which is helps meet the demanding ADAS and autonomous driving applications.
NXP S32G3 EVB	Chiplet-based automotive microcontroller	▪ Powertrain control and other related applications ▪ Several power-saving capabilities, including dynamic voltage and frequency scaling ▪ Can provide up to 10.7 TOPS of performance
Renesas R-Car V4H	Automotive system-on-a-chip (SoC) based on chiplets	▪ Infotainment and other related application ▪ Performance of the R-Car V4H may reach 10.8 TOPS. ▪ Numerous features for optimization and power conservation are also offered

Chiplet technology is still relatively new in the automotive industry, but it has the potential to completely change how cars are designed and manufactured. Chiplet technology can help to increase efficiency, performance, and reliability by enabling automakers to design unique chips that are suited to the particular requirements of their cars.

2.1 Leading Communication Technologies in Semiconductor Industry:

In the semiconductor industry, communication technologies play a pivotal role in facilitating data exchange and connectivity between various components within electronic systems. In particular, the emergence of chiplets has introduced innovative methods for achieving modularity and enhancing semiconductor communication.

The leading communication technologies in the semiconductor industries include

i)Ethernet:

Ethernet technology is a fundamental element in modern networking and data communication, essential for enabling data exchange within data centers and across the internet. It has evolved to support high-speed data transmission and is of paramount importance in fulfilling the connectivity needs of the semiconductor industry. Ethernet uses packet-based data transfer and a number of different protocols and physical layer technologies to make data transfer as efficient as possible (up to 400 Gbps i.e 400 Gigabit Ethernet), reduce latency, and allow for growth. Semiconductors are pivotal in making Ethernet technology effective in facilitating communication and networking. Below is a breakdown of Ethernet technology

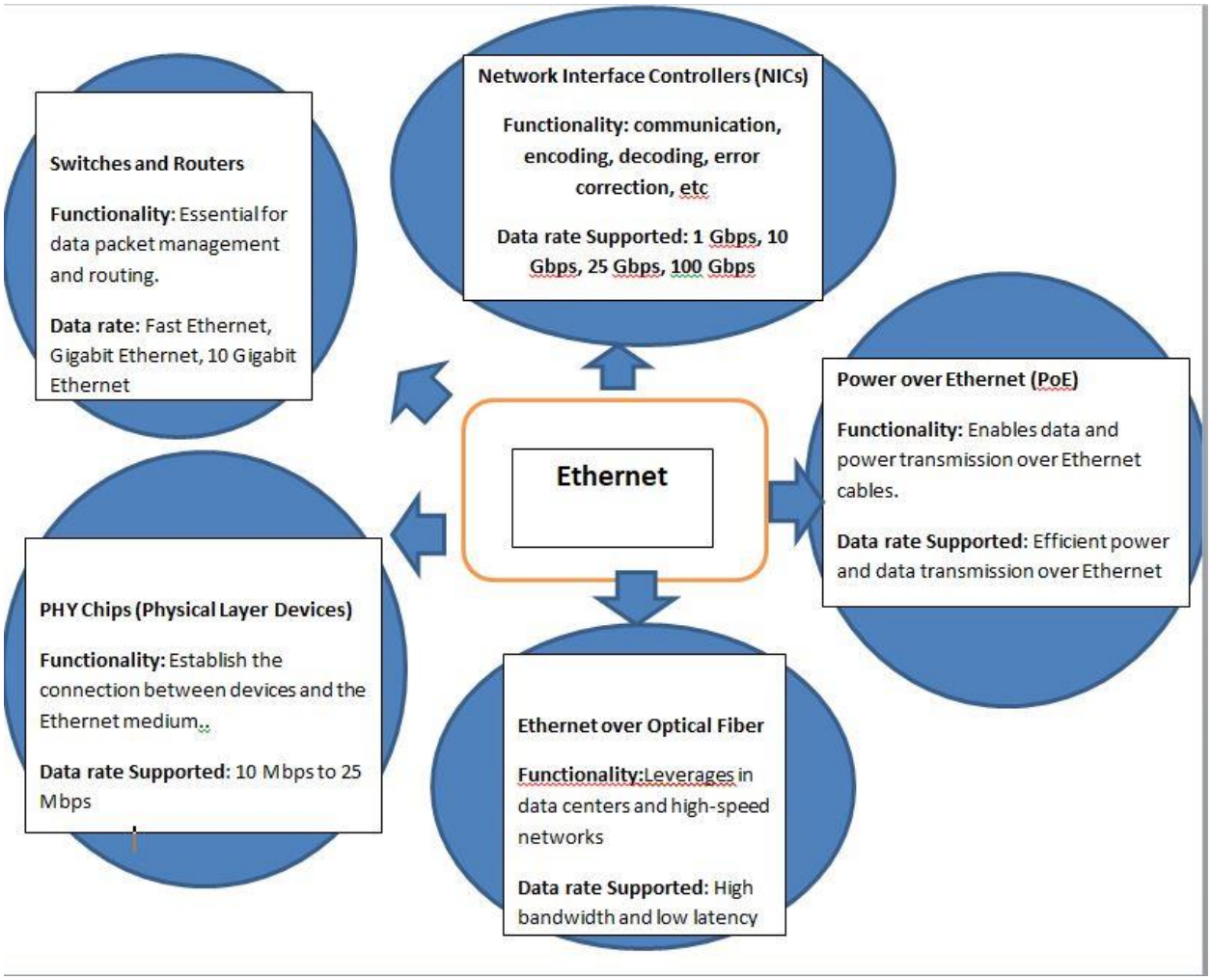


Figure9:Ethernet

ii)USB (Universal Serial Bus) :

USB serves as a widely adopted interface for connecting peripherals and devices to host systems. USB utilizes various data transmission modes, such as

i. Isochronous mode - Rate can range from as low as 1.5 Mbps (USB 1.0) to as high as 20 Gbps (USB 4)
ii. Bulk mode - Can achieve data rates ranging from 12 Mbps (USB 1.0) to 20 Gbps (USB 4).
iii. Interrupt mode - Used for low latency devices such as keyboard/mouse etc. The data rate ranges from 1.5 Mbps (USB 1.0) to 20 Gbps (USB 4)

thus, accommodating a wide range of device types.
Enhanced versions like USB 3.2 and USB 4 offer increased data rates and compatibility.
USB 3.2 consists of different generations with 8b/10b and 128b/132b encoding, with data transfer rates ranging from 5Gbps to 20 Gbps.
For USB 4, the types of encoding include 128b/132b, 66b/68b and PAM-3, along with the data transfer rates ranging from 10Gbps to 120 Gbps (latest). Now-a-days, USB type C to C cables are also booming with data transfer rates as high as 80 Gbps cables. These are very high data rates with high compatibility.

iii)Serial Attached SCSI(Small Computer System Interface) (SAS):

SAS is a high-speed interface for connecting and transferring data between storage devices, including hard disk drives (HDDs) and solid-state drives (SSDs), in data centers and enterprise environments.
SAS employs a point-to-point serial connection for efficient data transfer and supports various protocols and data rates, including 12 Gbps and 24 Gbps. SAS is backward compatible with SATA drives, allowing SAS controllers to use SATA drives, thus making storage configurations flexible and cost-efficient.

iv)SATA (Serial ATA):

SATA is a computer bus interface employed for connecting HDDs and SSDs to a computer's motherboard in consumer and enterprise systems.
Communication Technology: SATA is a point-to-point connection that supports data rates of 6 Gbps (SATA revision 3.0, SATA - 600) and 12 Gbps (SATA 3.2). The SATA Express (SATA revision 3.2) specification defines an interface that combines both SATA and PCI Express buses (which are also used in chiplet technology), making it possible for both types of storage devices to coexist. The PCI express offers a much higher theoretical output of 1969 MB/s. The SATA revision 3.5 released in July 2020, introduces features that promote greater integration of SATA devices , enabling higher performance and compatibility of products with other industry I/O standards.

v)HDMI (High-Definition Multimedia Interface):

HDMI is widely utilized for high-definition mp3 and mp4 connections across various devices, including TVs, monitors, and gaming consoles. HDMI, facilitating a data rate of up to 48 Gbps, utilizes a packet-based data transmission approach to carry both video and audio signals. It continually evolves to support higher resolutions and features such as Ethernet over HDMI. For instance, HDMI supports a wide range of video resolutions, including standard definition (SD), high definition (HD), Full HD (1080p), Ultra HD or 4K (2160p), and even 8K (4320p) resolutions, with refresh rates of up to 144 Hz depending on the resolution.

vi)Thunderbolt:

developed jointly by Intel and Apple, combines PCIe (often used as a chiplet interconnectrotocol) and DisplayPort technologies, commonly used for connecting high-performance peripherals to computers.
Thunderbolt employs a blend of PCIe data transfer and DisplayPort for video transmission over a single cable.

Thunderbolt 5 unidirectional bandwidths up to 120 Gbps (three times that of Thunderbolt 3 and 4), making it suitable for various applications, including external storage and displays. It also support USB 4.0 . Thunderbolt also provides appropriate power to charge laptops and devices through the same cable used for data transfer, along with support for Daisy-Chaining.

vii)InfiniBand:
InfiniBand is a high-speed interconnect technology commonly applied in high-performance computing clusters, data centers, and storage systems. It uses a switched fabric topology optimized for low-latency, high-bandwidth communication between computing nodes. It supports flexible topologies, efficient data routing between devices with direct memory-to-memory transfer. Most importantly, it is easily scalable for large clusters.

viii)Fiber Channel:
Fiber Channel is a high-speed storage networking technology extensively used in data centers to connect storage devices to servers. Fiber Channel relies on optical fibers for data transmission and supports high-speed data rates. It is designed to ensure high reliability and low latency for storage connectivity. It has multiple data transfer rates available ranging from 100 to 12,800 MB/s along with diverse topologies, port connectivity, access for control security, common SCSI transport protocol. Fibre Channel over Ethernet (FCoE) is another type of computer network technology that encapsulates Fibre Channel frames over Ethernet networks. It facilitates convergence due to network simplification, saves cost of infrastructure and enhanced expandability.

ix)SerDes (Serializer/Deserializer):
SerDes technology is a pivotal component within high-speed data communication systems, commonly found in data centers and networking equipment. Its primary role is to facilitate the conversion of data between parallel and serial formats, thereby enhancing the efficiency of data transmission. This technology holds immense significance in modern communication systems. SerDes is used majorly in order to reduce the number of data paths for data transmission, addressing power and interference challenges with parallel data transmission and ensure high speed data transmission over long distances.

Depending on the specific application, SerDes supports a wide variety of data rates, commonly including 10 Gbps, 25 Gbps, 56 Gbps, and 112 Gbps. These speeds are continually evolving, with higher rates becoming available to meet the increasing demand for faster data transfer. The acceptable Bit Error Rate (BER) are typically very low as much as 10^{-12} to 10^{-15}, indicating a high level of data integrity and reliability in the transmission process. SerDes technology is designed to meet specific interface standards like PCIe (Gen 5 and 6 for high speed interconnects) along with USB. It also works with varying data widths as 8,16, 32 or more and also has high jitter tolerance. Apart from these, SerDes is used in mixed-signal circuits, equalization methods to fix signal degradation, CDR (Clock and Data Recovery), error correction and many others.

x)MIPI (Mobile Industry Processor Interface):

MIPI (Mobile Industry Processor Interface) is a suite of communication protocols widely employed in mobile devices, facilitating efficient data exchange between critical components like cameras, displays, and sensors. Its core objectives include enhancing interoperability, reducing design complexity, and fostering innovation in these systems to meet the growing demand for higher performance, reduced power consumption, and smaller component sizes.

MIPI specifications are instrumental in the semiconductor industry, offering standardized, reliable, and efficient means for various components to communicate and collaborate seamlessly. These specification include display interfaces, camera interfaces, sensor interfaces, and power management. A few instances are mentioned below:

MIPI Interfaces	Purpose and functionality	Key Components/ Protocols	Scope of Application
MIPI SLIMbus	Audio transport for mobile device withHigh Speed , low power and EMI	CMOS IOs, used in smartphone	Mobile Devices, automotive, IoT.

MIPI DSI	Connects display panels to processors for image/video	Facilitates vibrant visual displays	Mobile Devices,automotive,AR/VR headset.
MIPI Uni Pro	Unified protocol for Seamless Communication	Used MIPI-PHY for data transfer	Mobile Devices,semiconductor integration.
MIPI I3C	Simplifies sensor-to-processor connections	Enable efficient sensor data relay	Mobile Devices,semiconductor integration ,IoT.
MIPI REF(RF Front-End)	Optimizes RF components for wireless communication	Enhances wireless connectivity	Mobile Devices, automotive, IoT.
MIPI D-PHY and C-PHY	Vital high speed serial communication	Enable efficientdata exchange.	Mobile Devices,automotive, semiconductor integration.

xi)Optical Communication:

Optical communication technologies, including optical transceivers and fiber optics, are gaining increasing importance in high-speed data transfer and long-distance communication, particularly in data centers and high-performance computing.

Optical Component	**Description and Functionality**	**Key Semiconductor Components**	**Data Rates and Specifications**	**Applications**
Lasers and SOAs	Generate coherent light signals and amplify optical signals for transmission.	Laser diodes, SOAs	Lasers: Milliwatts to watts, SOAs: 10-30 dB	Long-distance optical communication
Photodetectors	Convert optical signals into electrical signals for further processing.	Semiconductor materials (e.g., InGaAs)	Responsivity: 0.5 A/W to 1.5 A/W, Bandwidth: 10 GHz to 50 GHz	Optical signal-to-electrical signal conversion
Modulators and Semiconductor Optical Modulators	Encode data onto optical signals using semiconductor technology.	Mach-Zehnder, electro-absorption modulators	High modulation bandwidth, Extinction ratios: 5-10 dB	Data encoding in optical signals
Optical Transceivers	Compact modules with lasers, photodetectors, and electronic driver circuitry.	Various semiconductor components	Data rates: 10 Gbps, 25 Gbps, 100 Gbps, 400 Gbps	Networking equipment
Optical Signal Processing ICs	Semiconductor-based ICs for signal processing, error correction, and conditioning.	Semiconductor ICs	Multiple gigabits per second, SNR, BER	Enhancing optical signal quality
Wavelength Division Multiplexing (WDM) Chips	Combine and separate multiple optical signals for simultaneous data transmission.	Semiconductor chips	Wavelength spacing: 0.4 nm to 0.8 nm	Multiplexing and demultiplexing of optical signals

Semiconductor Optical Switches	Efficiently route optical signals within a network.	Semiconductor technology	Switching times: nanoseconds to microseconds	Signal routing in optical networks
Semiconductor Optical Amplification (SOA)	Enhance the strength of optical signals for long-distance transmission.	Semiconductor optical amplifiers	Gain levels: 10 dB to 30 dB, C and L bands	Amplification for extended-range communication
Optical Transponders and Regenerators	Receive, regenerate, and transmit optical signals in high-speed optical networks.	Various semiconductor components	Data rates: 10 Gbps to 100 Gbps or more	Signal reception, regeneration, and transmission
Silicon Photonics	Integrates optical and electronic components on a silicon substrate for compact devices.	Semiconductor fabrication processes	Data rates: 100 Gbps, 400 Gbps, or higher	Compact and high-performance optical devices
Coherent Detection and Digital Signal Processing (DSP)	Utilizes semiconductor-based DSP for complex optical signal processing.	Semiconductor-based DSP	Bit rates: 100 Gbps to 800 Gbps, advanced modulation formats	Enhanced optical signal quality and error correction
Semiconductor Materials for Light Emission and Detection	Various semiconductor materials for light emission and detection.	Gallium arsenide, InGaAs, etc.	Laser diode outputs: milliwatts to watts, Photodetector response wavelengths: near-infrared	Light emission and detection in optical communication

All the important leading communication technologies in the communication field are summarized below:

Semiconductor-based technology	**Type/ Specific use case (If any)**	**Purpose and functionality**	**Key components / Protocols**	**Metrics**	**Scope of Application**
Ethernet	NIC, Switches and Routers, PHY Chips, IoT and Embedded Systems, Ethernet over Optical Fiber	- Enables data exchange in data centers and internet. - Supports high-speed data transmission.	- NICs, Switches, Routers, PHY Chips, Optical Transceivers. - Diverse protocols and	- Speeds ranging from 10 Mbps to 800 Gbps. - Various encoding types for	- Data centers, internet, LAN, IoT, high-speed networks. - High-speed data exchange, low-power

		- Orchestrates data flow and connectivity. - Facilitates network integration. - Ensures high bandwidth, low latency communicatio n.	encoding schemes.	efficient data transfer.	IoT, large-scale deployment.
USB	USB 2.0, 3.2, 4.0 ,Type C to C	- Supports isochronous, bulk, and interrupt data transfer modes. - Accommodate s various data rates.	- USB-A, USB-B, EHCI, USB-C, xHCI, PCIe. - Protocols for isochronous, bulk, and interrupt modes.	- Data rates from 1.5 Mbps to 80 Gbps. - Suitable for a wide range of applications, including real-time tasks, high-speed data transfer, and low-latency devices. - Uses various USB connectors and protocols for high data rates.	- Versatile data connectivity in modern devices and peripherals. - Supports high-speed connections and data transfer.
HDMI (High-Definition Multimedia Interface)	-	- Used for high-definition mp3 and mp4 connections in devices like TVs, monitors, and gaming consoles. - Utilizes packet-based data transmission	- HDMI connectors and cables. - Protocols for video and audio transmission.	- Data rate of up to 48 Gbps. - Supports multiple video resolutions and refresh rates. - Supports various video	- Used for high-definition connections in devices like TVs, monitors, and gaming consoles. - Suitable for a wide range of video

		for video and audio signals to support higher resolutions and features		resolutions, including SD, HD, Full HD (1080p), 4K (2160p), and 8K (4320p) with refresh rates up to 144 Hz.	resolutions, from standard to 8K. - Evolving to meet advanced audio and video needs.
Fiber Channel	Fiber Channel, Fiber Channel over Ethernet (FCoE)	- High-speed storage networking, ensuring reliability and low-latency connectivity. - Supports data rates from 100 to 12,800 MB/s with diverse topologies and access control. - Encapsulates Fiber Channel frames over Ethernet for network simplification and cost reduction	- Fiber Channel switches, adapters, and optical fibers. - SCSI transport protocol. - FCoE adapters and Ethernet networks. - Encapsulation protocols for Fiber Channel frames.	- Data rates from 100 to 12,800 MB/s.	- Data centers, ensuring fast, reliable, and low-latency storage connectivity with security. - Facilitates network simplification, cost reduction, and expandability.
SerDes	-	- Converts data between parallel and serial formats, optimizing efficiency and data integrity. - Supports high-speed data transmission (10 Gbps to 112 Gbps)	- SerDes components and data transmission protocols.	- Data rates from 10 Gbps to 112 Gbps with low BER levels.	- Crucial in high-speed data communication systems, ensuring data integrity in various applications.

		with low Bit Error Rates.			
MIPI Interfaces	MIPI SLIMbus, MIPI DSI, MIPI Uni Pro, MIPI I3C, MIPI RF (RF Front-End), MIPI D-PHY, MIPI C-PHY	- Facilitates audio transport, display panel connections, seamless communication, sensor-to-processor connections, RF optimization, high-speed data exchange. - Enhances wireless connectivity, visual displays, and efficient sensor data relay.	- CMOS IOs, MIPI-PHY, MIPI RF Front-End. - MIPI SLIMbus Protocol, MIPI D-PHY, C-PHY, M-PHY, UniPro, I3C Protocol.	- Data rates vary by type, up to 24 Gbps per lane.	- Mobile Devices, automotive, IoT, semiconductor integration. - Supports high-speed data transmission, audio, imaging, and efficient sensor connections.
Optical Components	Lasers and SOAs, Photodetectors, Semiconductor Optical Modulators,Optical Transceivers, Optical Signal Processing ICs, WDM chips, Semiconductor Optical Switches, SOA, Optical Transponders and Regenerators, Silicon Photonics, Coherent Detection and DSP, Semiconductor Materials for	-Generate, amplify, convert, encode, route, amplify, receive, regenerate, and process optical signals. - Enhance optical signal quality and perform wavelength division multiplexing. - Integrate optical and electronic components	- Various semiconductor components, semiconductor materials. - Mach-Zehnder, electro-absorption modulators. - Compact modules with lasers, photodetectors, electronic driver circuitry. - Multiple gigabits per second, SNR,	- Lasers: Milliwatts to watts, SOAs: 10-30 dB. - Responsivity: 0.5 A/W to 1.5 A/W, Bandwidth: 10 to 50 GHz. - Data rates: 10, 25, 100,400 Gbps. - Data rates: 10 to 100 Gbps or more. - Data rates: 100, 400	Light emission and detection in optical communication

	Light Emission and Detection	for compact devices. - Utilize semiconductor -based DSP for complex optical signal processing.	BER. - Wavelength spacing: 0.4 nm to 0.8 nm. - Switching times: nanoseconds to ms - Gain levels: 10 dB to 30 dB, C and L bands. - Bit rates: 100 Gbps to 800 Gbps, advanced modulation formats. - Gallium arsenide, InGaAs, etc.	Gbps, or higher.	

2.2 Leading Communication Technologies in Chiplet:

1)UCIe: Universal Chiplet Interconnect Express

Universal Chiplet Interconnect Express (UCIe) is a high-bandwidth, low-latency interconnect standard that integrates chiplets from multiple suppliers into a package. While still in development, UCIe might revolutionize the semiconductor industry by enabling more powerful and efficient processors.

The latest UCIe version is 1.1, published in August 2023. Support for simultaneous multiprotocol, runtime health monitoring and repair, and bump maps for lower-cost packaging are added to UCIe 1.1. UCIe is utilized in HPC, AI, mobile, and automotive systems. AMD's late 2023 Ryzen 7000 series CPUs use UCIe.

Specific instances of UCIe use today:

i. **HPC:** The Frontier supercomputer at Oak Ridge National Laboratory uses UCIe to link chiplets. Frontier, the fastest supercomputer, connects AMD GPUs and CPUs with UCIe.

ii. **AI:** AI accelerators like Habana Gaudi employ UCIe to link chiplets. The Gaudi processor connects its many cores using UCIe to train and deploy massive language models.

iii. **Mobile:** UCIe connects chiplets in mobile devices such as the Qualcomm Snapdragon 8 Gen 2 SoC. The Snapdragon 8 Gen 2 will be the first mobile SoC to link its CPU, GPU, and other components using UCIe.

iv. **Automotive:** UCIe connects autonomous driving chiplets. The Nvidia Drive Hyperion platform connects its sensors and CPUs with UCIe.

Feature	UCIe 1.1	UCIe 1.0
Maximum bandwidth	32 GT/s	16 GT/s
Maximum latency	1 ns	1.5 ns
Power consumption	1 pJ/bit	1.2 pJ/bit
Form factor	Package-on-package (PoP)	Package-on-package (PoP)
Supported chiplet types	CPUs, GPUs, FPGAs, custom ASICs	CPUs, GPUs, FPGAs, custom ASICs
New features	Simultaneous multiprotocol support, runtime health monitoring and repair, bump maps for lower-cost packaging	None

UCIe, a novel technology, might change the semiconductor industry. Data centers, wearables, and IoT devices will utilize UCIe more as it spreads.

2)AMBA Chiplet Interconnect

A flexible and efficient connecting standard, AMBA Chiplet connecting (AXI-CI), allows chiplets to be integrated into low-power mobile devices like smartphones and tablets. AXI-CI uses the Arm AMBA interconnect standard, a popular semiconductor connection protocol.

The latest version of AXI-CI, AXI-CI 5.0 adds a number of new features, including support for multiple chiplet types, dynamic power management, and enhanced security features.

AXI-CI 5.0 is a significant upgrade over AXI-CI 4.0 offering flexible chiplet connections, dynamic power management, enhanced security, higher bandwidth for performance, and lower latency for real-time applications as compared to AXI-CI 4.0

3)Intel Chiplet Interconnect Bridge (EMIB):

Intel Chiplet Interconnect Bridge (EMIB) connects chiplets from several suppliers into a single package with great performance and low latency. EMIB uses a thin silicon interposer to connect chiplets. The March 2023 release of EMIB is EMIB 3.
Over prior generations, EMIB 3 has better bandwidth, lower latency, and lower power consumption. EMIB is utilised in Intel Xeon Scalable CPUs and Stratix 10 FPGAs. EMIB connects two Intel Xeon Platinum 8476 processors in the 8476P processor.

Specific examples of EMIB use today:

Intel Stratix 10 FPGAs employ EMIB to connect chiplets. Intel can now make more complicated and powerful FPGAs for AI and machine learning.

Other Intel products: The Agilex FPGAs and Ponte Vecchio GPU employ EMIB.
EMIB, a revolutionary technology, could transform the semiconductor industry. As EMIB gains popularity, mobile devices and data center servers may use it.

Feature	**Value**
Maximum bandwidth	10 TB/s
Maximum latency	1 ns
Power consumption	1 pJ/bit
Form factor	1 pJ/bit
Supported chiplet types	CPUs, GPUs, FPGAs, custom ASICs

Feature	Improvement over EMIB 2
Bandwidth	+25%
Latency	-20%
Power consumption	-15%

4)PCI Express (PCIe)

The high-speed serial computer expansion bus PCI Express (PCIe) replaces PCI, PCI-X, and AGP. Personal computers' graphics cards, sound cards, HDD host adapters, SSDs, Wi-Fi, and Ethernet hardware connectors use this motherboard interface. The current PCIe version is 5.0, released in 2019. PCIe 5.0 doubles PCIe 4.0's bandwidth to 16 GT/s per lane.

Many devices employ PCIe, including:

- Personal computers: PCIe is the standard interface for graphics, sound, network, and expansion cards.
- Servers: PCIe connects storage, network, and accelerator cards in servers.
- PCIe is used in routers, switches, and other industrial devices.
- PCIe is a flexible and scalable connectivity technology utilised in many products. It will likely remain the dominant connection standard for years.

Specific examples of PCIe use today:

- Graphics cards: PCIe connects motherboards to graphics cards. This lets users upgrade their graphics cards to boost PC performance in games and other graphics-intensive apps.
- SSDs: PCIe connects SSDs to motherboards. This lets users use SSDs' high performance.
- PCIe connects motherboards and network cards. This connects PCs to fast networks.
- GPUs and FPGAs are connected to motherboards via PCIe. This accelerates machine learning and AI tasks.
- PCIe is a key connection standard for high-performance devices. It is predicted to continue to influence technology development.

Raw data rate	64 GT/s
Maximum bandwidth (x16 configuration)	256 GB/s
Signaling	PAM4
Error correction	Lightweight FEC and CRC
Encoding	Flit-based
Packet layout	Updated to provide additional functionality and simplify processing
Backwards compatibility	Yes

2.3 IPs for communication between chiplets:

1)NuLink:

Eliyan's Interconnect technology built with standard organic chip packaging delivers the same performance as advanced packaging technology, and enables The Ultimate Chiplet Systems at a fraction of total cost of ownership. The exclusive trade secrets and patent-protected technologies deliver a UCIe compliant interconnect at twice the bandwidth and half the power.

The NuLink architecture leveraged cross-technology innovations to deliver the highest bandwidth and lowest latency, at best-in-class area and power efficiency.

NuLink is the physical layer, which means you can run any protocol layer you want on top of it. To put this another way, NuLink is a superset of the UCIe protocol layer and the BoW physical layer.

i. NuLink provides high bandwidth at low power.
ii. Enables large and complex systems in package (10-12 reticles).
iii. Low packaging cost and short production cycle.
iv. High test coverage and high yield.
v. Long D2D reach and low thermal crosstalk.
vi. Good signal and power integrity.
vii. Widely available supply chain.
viii. Operational speed: 40 Gbps per bump
ix. Beachfront bandwidth: 2.2 Tbps per millimeter(for packaging with a 130-µm bump pitch)
x. Increased throughput: With finer bump pitches, up to 3 Tbps per millimeter can be achieved.

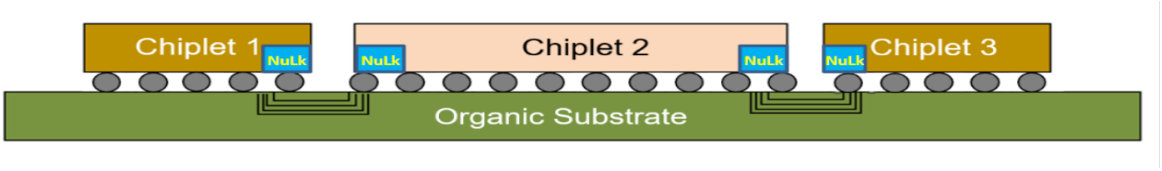


Figure10:NuLink

Source : eejournal.com

Data rate	20Gbps, 32Gbps, and 40Gbps
Latency	Less than 2ns
Power consumption	Less than 1mW/Gbps
Link width	128 bits, 256 bits, and 512 bits
Scalability	Scalable
Flexibility	Flexible
Features	Supports multiple chiplet types, supports different packaging technologies
Applications	High-performance computing, data centers, artificial intelligence, machine learning, networking, storage

2)CXL:

Compute Express Link (CXL) - An industry-supported Cache-Coherent Interconnect for Processors, Memory Expansion and Accelerators.CXL is an open standard industry-supported cache-coherent interconnect for processors, memory expansion, and accelerators. Essentially, CXL technology maintains memory coherency between the CPU memory space and memory on attached devices. This enables resource sharing (or pooling) for higher performance, reduces software stack complexity, and lowers overall system cost. The CXL Consortium has identified three primary classes of devices that will employ the new interconnect:

Type 1 Devices: Accelerators such as smart NICs typically lack local memory. Via CXL, these devices can communicate with the host processor's DDR memory.

Type 2 Devices: GPUs, ASICs, and FPGAs are all equipped with DDR or HBM memory and can use CXL to make the host processor's memory locally available to the accelerator—and the accelerator's memory locally available to the CPU. They are also co-located in the same cache coherent domain and help boost heterogeneous workloads.

Type 3 Devices: Memory devices can be attached via CXL to provide additional bandwidth and capacity to host processors. The type of memory is independent of the host's main memory.**CXL 2.0 and 3.0:**

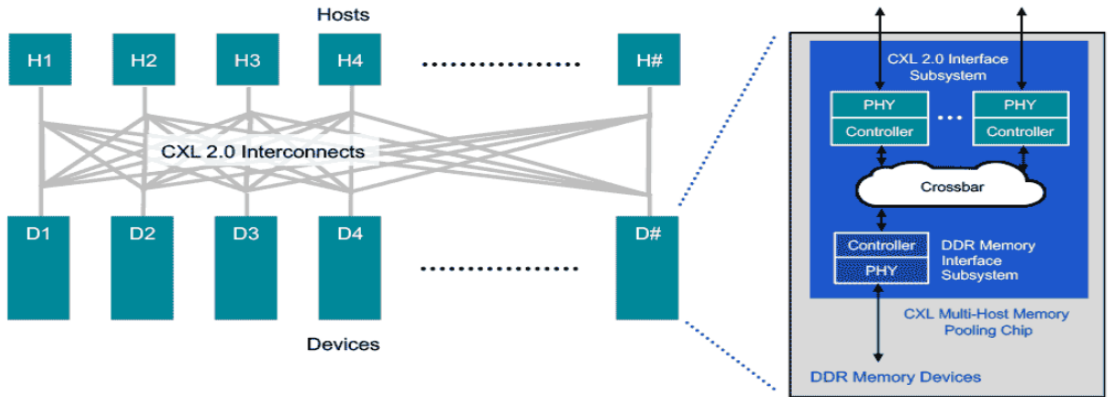


Figure10 :CXL Memory Pooling Through Direct Connect

Source: rambus.com

Memory Pooling is a technology supported by CXL 2.0, allowing hosts to access memory devices from a shared pool. CXL 2.0-enabled hosts can utilize a mix of CXL 1.0, 1.1, and 2.0 memory devices. While CXL 1.0/1.1 devices act as single devices for one host at a time, CXL 2.0 devices can be divided into multiple logical sections, permitting up to 16 hosts to access different parts simultaneously. For instance, Host 1 can use a portion of Device 1 and Device 2 to match its workload's memory needs. CXL 3.0 enhances memory pooling, allowing multiple hosts to coherently share memory space on a CXL 3.0 device, introducing more flexibility in data center setups.Switching in CXL 2.0 involves transitioning to a direct-connect architecture, enabling data centers to expand their main memory effectively and reduce costs. All hosts and devices need to be CXL 2.0-enabled. The "switching" process is handled within memory devices using a crossbar in the CXL memory pooling chip. This keeps data transfer times short but necessitates a more powerful chip to manage switching. It allows memory devices to extend host main memory using DDR DRAM in a flexible way, with hosts accessing the required capacity for specific workloads. CXL 3.0 introduces multi-tiered switching, enabling switch fabrics and significantly expanding scalability beyond the single-layer switching capability of CXL 2.0.

CXL 1.0:

Bit Lanes: CXL 1.0 uses 16 lanes with each lane having a data rate of 32 Gbps.Maximum Aggregate Bandwidth: 64 GB/s (gigabytes per second) for a x16 connection.

CXL 2.0:

Bit Lanes: CXL 2.0 uses 16 lanes with each lane having a data rate of 32 Gbps.Maximum Aggregate Bandwidth: 128 GB/s for a x16 connection.

CXL 3.0 specifications:

Data rate	Up to 64 GT/s (8GB/s per lane)
Latency	Less than 2ns
Power consumption	Up to 25 watts
Link width	x1, x4, x8, x16, x24, x32
Scalability	Highly scalable
Flexibility	Flexible
Features	Supports multiple device types, supports multiple protocols, supports hot-plug and unplug, supports error correction and detection (ECC), supports security features
Applications	High-performance computing, data centers, artificial intelligence, machine learning, networking, storage

Features	CXL 1.0 / 1.1	CXL 2.0	CXL 3.0
Release date	2019	2020	1H 2022
Max link rate	32GTs	32GTs	64GTs
Flit 68 byte (up to 32 GTs)	✓	✓	✓
Flit 256 byte (up to 64 GTs)			✓
Type 1, Type 2 and Type 3 Devices	✓	✓	✓
Memory Pooling w/ MLDs		✓	✓
Global Persistent Flush		✓	✓
CXL IDE		✓	✓
Switching (Single-level)		✓	✓
Switching (Multi-level)			✓
Direct memory access for peer-to-peer			✓
Enhanced coherency (256 byte flit)			✓
Memory sharing (256 byte flit)			✓
Multiple Type 1/Type 2 devices per root port			✓
Fabric capabilities (256 byte flit)			✓

Figure11:CXL Features

Source design_reuse.com

3)Low Voltage In Package Interconnection (LIPINCON):

LIPINCON stands for "low-voltage, in-package interconnect." .TSMC's LIPINCON is a proposed interface for connecting different components (like processors, memory, or I/O controllers) within a computer chip or package. It's designed to provide high data bandwidth while minimizing power usage and signal interference. Here are the key points about LIPINCON:

ADVANTAGES:

1. **Low Voltage Operation**: LIPINCON is designed to operate at low voltages, which helps reduce power consumption and heat generation. This is crucial for modern electronics, especially in applications where power efficiency is critical, such as mobile devices and data centers.
2. **Interconnection Technology**: LIPINCON focuses on the interconnections between chiplets within the same package. These interconnections need to be designed to handle the low voltage operation while providing high-speed data transfer and low-latency communication between the chiplets.
3. **Heterogeneous Integration**: Chiplets often come from different manufacturers or process technologies, and LIPINCON allows for their integration into a single package. This is known as heterogeneous integration, where chiplets with different functionalities and manufacturing processes are combined to create a more powerful and feature-rich system.
4. **System-in-Package (SiP):** LIPINCON is often associated with the concept of System-in-Package (SiP), where multiple chiplets and other components are integrated into a single package. The low-voltage interconnections are crucial for the efficient and reliable operation of these SiP solutions.

5. **Reduced latency:** LVPI has lower latency than traditional interconnects, which can improve the responsiveness of processors. This is important for applications that require real-time communication, such as gaming and video conferencing.

6. **Smaller size:** LVPI interconnects are smaller than traditional interconnects, which can reduce the size of processors. This is important for a number of reasons, including making processors more compact and easier to cool.

APPLICATION:

- **High-performance computing (HPC):** LVPI is a key enabler of HPC applications, as it can provide the high bandwidth and low latency required for these demanding workloads.

- **Artificial intelligence (AI):** LVPI is also well-suited for AI applications, as it can handle the high data rates and low latencies required for deep learning and other AI algorithms.

Data rate	Up to 64 GT/s (8GB/s per lane)
Latency	Less than 2ns
Power consumption	Less than 1mW/Gbps
Link width	x1, x4, x8, x16, x24, x32
Scalability	Scalable
Flexibility	Flexible
Bandwidth density	1.6Tb/s/mm2
Energy efficiency	0.56pJ/bit
Applications	Networking

5)AXI (Advanced Extensible interface)::

AXI is often used as the interface standard for connecting these chiplets together, facilitating communication and data transfer between the various chiplets in a system. This usage of AXI in chiplet-based designs offers several advantages:

1. **Scalability:** AXI is a scalable interconnect standard, which makes it well-suited for connecting chiplets of various functionalities and sizes. It allows chiplets to be added or removed from a system with relative ease.

2. **Compatibility:** Many semiconductor design tools, IP cores, and hardware components support AXI as a standard interface. This compatibility simplifies the integration of chiplets from different sources into a cohesive system.

3. **Performance:** AXI supports high-bandwidth data transfer and efficient communication between chiplets, enabling high-performance systems.

4. **Reusability:** Designers can create AXI-based IP cores and interfaces for chiplets, making it possible to reuse these components in different chiplet-based systems.

5. **Interoperability:** AXI-based chiplets can often be integrated with other chiplets that use AXI interfaces, facilitating interoperability in complex systems.

In chiplet-based systems, AXI can be used for a wide range of applications, such as connecting CPU chiplets, GPU chiplets, memory chiplets, I/O chiplets, and more.

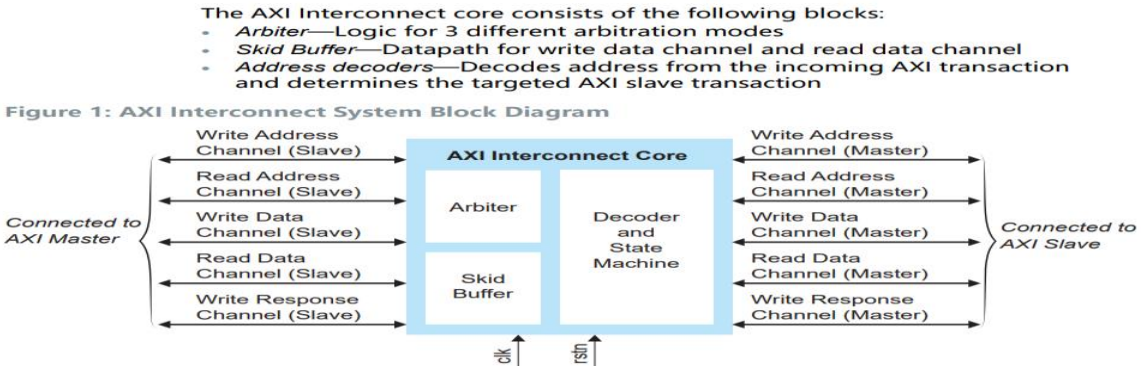


Figure12:AXI

Source: elitestek.com

Data rate	Up to 320 GB/s
Latency	Less than 3ns
Power consumption	Less than 1mW/Gbps
Link width	x1 to x6
Scalability	Highly scalable
Flexibility	High
Applications	HPC, AI, embedded systems, networking, storage

6)AIB(Advanced Interface Bus):

AIB uses a wide parallel interface and operates at relatively low speeds, simplifying transmitter and receiver circuitry. It enables high-density packaging with microbumps, supporting clock speeds up to 1 GHz and a data rate of 2 Gbps per wire.

AIB is a physical-layer specification that connects to Media Access Controllers (MACs) and adjacent chiplets. It features various capabilities, including clock forwarding, receive-domain clock, duty-cycle correction, and retiming.

Two configurations of AIB are available: AIB Base, suitable for lightweight implementations, and AIB Plus, designed for higher speeds and reliable operation. AIB Plus supports double-data-rate (DDR) signaling, while AIB Base uses single-data-rate (SDR) signaling.

The physical arrangement of AIB minimizes signal skew, and signals are collocated for efficient bump placement. Redundancy mechanisms are in place to address faulty connections, improving module yields. Compared to SERDES, AIB offers lower latency

AIB Metrics

METRIC	AIB GEN1 (INTEL® STRATIX® 10 DEVICES)
Bandwidth/wire	2 Gbps
Wires/channel • As used by Intel FPGA • Specification and technology capability	 40 160
Bump density • As used by Intel FPGA (defined by interposer/bridge technology)	55 micron
Bandwidth/mm of die edge shoreline • As used by Intel FPGA • Specification and technology capability	 256 1,024
I/O voltage	0.9-0.7 V
Energy/bit	0.85 picojoule

Figure13 :AIB

Source:intel.com

Latency	Less than 1ns
Power consumption	Less than 1mW/Gbps
Link width	x1 to x64
Scalability	Highly scalable
Flexibility	Highly flexible
Applications	AI/ML accelerators

7)AMD Infinity Fabric

AMD Infinity Fabric) is a high-performance, low-power interconnect that integrates chiplets from several vendors into a package. A coherent connection protocol lets chiplets interact with high bandwidth and low latency in IF3 .Latest IF version is 4.0, announced in May 2023. The new IF4 has better bandwidth, lower latency, and lower power consumption. AMD devices like Ryzen Threadripper processors and Radeon Instinct MI200 accelerators require IF3. The Ryzen Threadripper PRO 5995WX processor connects four Zen 3 chiplets via IF3.

Here are some current uses of IF3: IF3 connects chiplets in Ryzen Threadripper CPUs like the PRO 5995WX. Combining chiplets with diverse capabilities lets AMD make more powerful and efficient processors.

Maximum bandwidth	64 GT/s
Maximum latency	1 ns
Power consumption	1 pJ/bit
Form factor	Package-on-package (PoP)
Supported chiplet types	CPUs, GPUs, FPGAs, custom ASICs

COMPARISON BETWEEN IPs :

Feature	NuLink	CXL 3.0	Infinity Fabric	LVPI	AXI	AIB
Target	General purpose	General purpose	High-performance computing	Networking	Networking	AI/ML Accelerator
Data rate	Up to 25 GB/s	Up to 50 GB/s	Up to 100 GB/s	Up to 32 GT/s	Up to 16 GT/s	Up to 400 GB/s
Latency	Low	Low	Very low	Low	Low	Very low
Power consumption	Low	Low	Moderate	Low	Low	Moderate
Cost	Low	Moderate	High	Moderate	Low	High
Applications	High-performance computing, data centers, artificial intelligence, machine learning, networking, storage	High-performance computing, data centers, artificial intelligence, machine learning, networking, storage	High-performance computing, data centers	Networking	Networking, storage	AI/ML accelerators

Figure 14 Comparison Between IPs

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