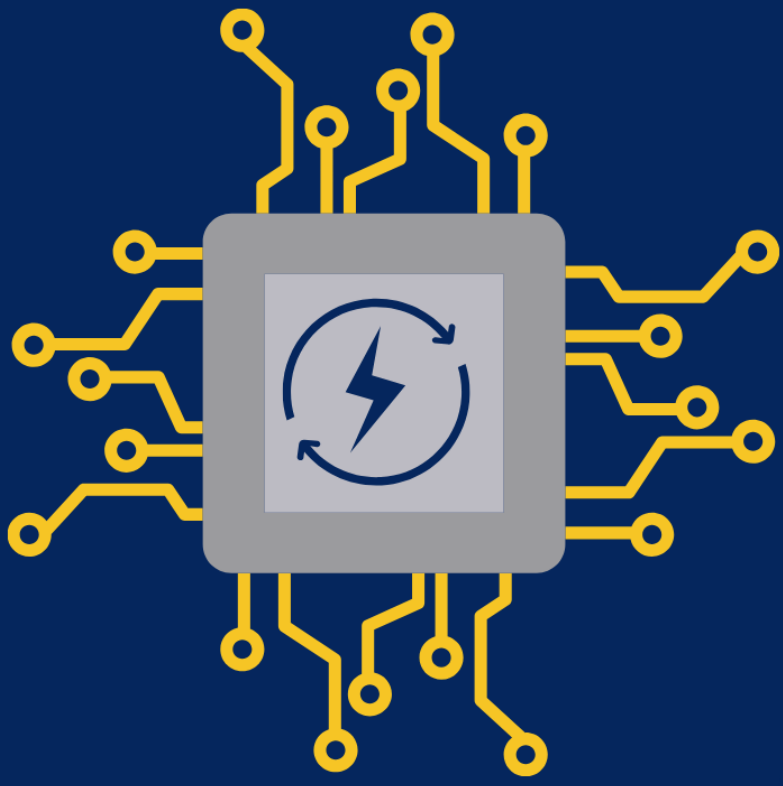
INTER IIT TECH MEET 12.0

19th to 22nd DECEMBER 2023

JLR CHIPLET CHALLENGE

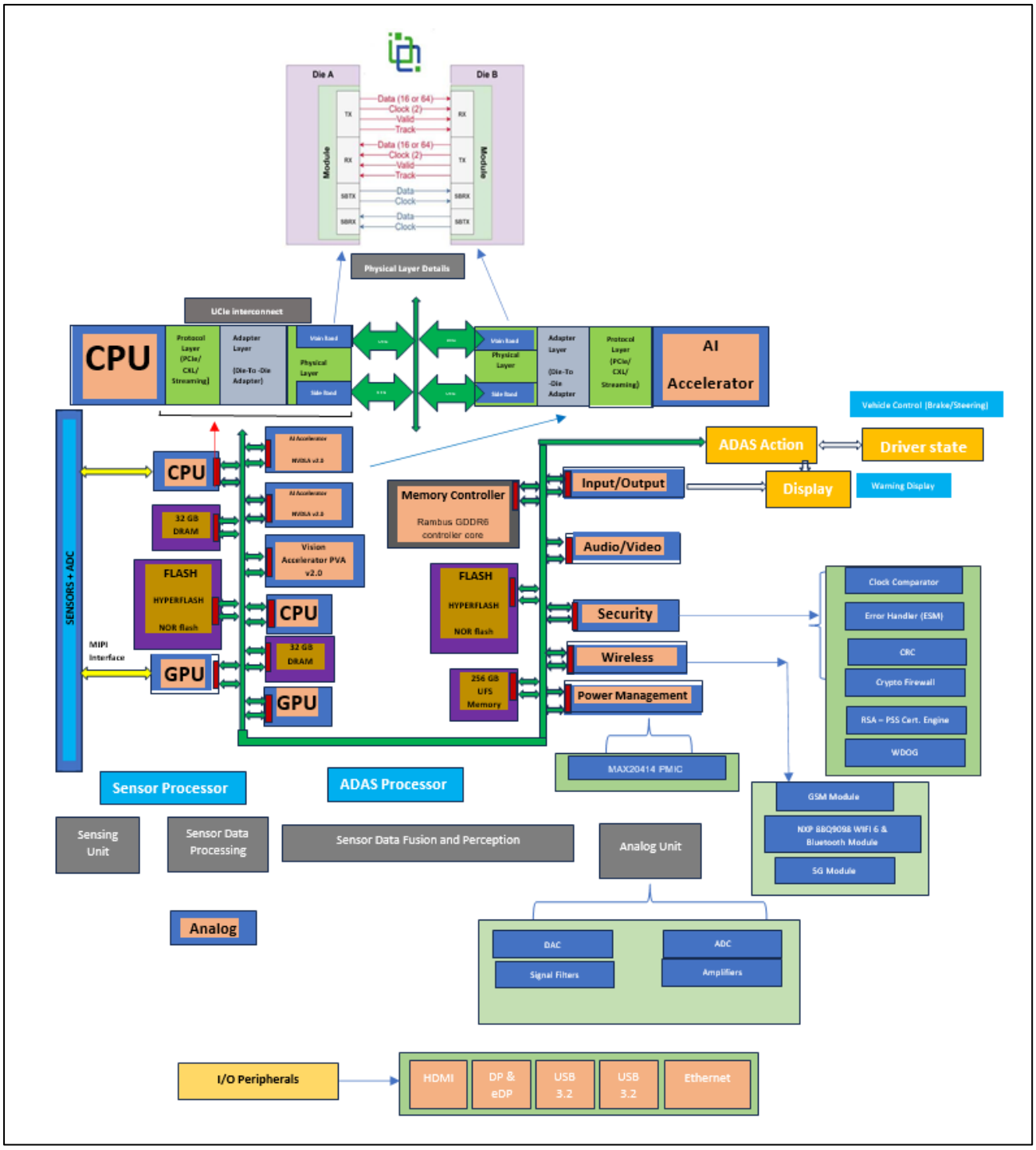


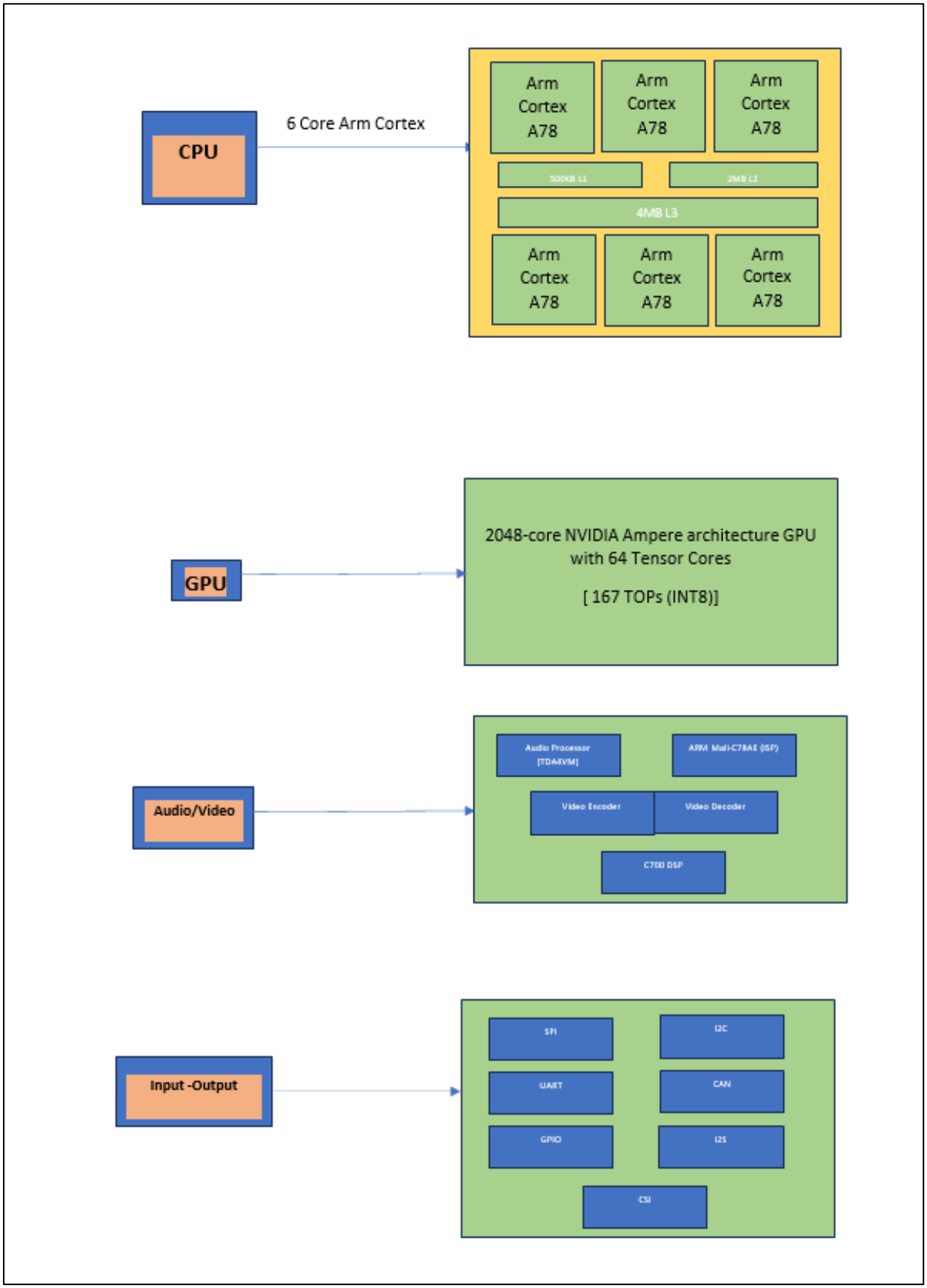
FINAL SUBMISSION

TEAM - 40

CONTENT

1. PROPOSED MICRO-ARCHITECTURE BLOCK DIAGRAM:




CPU
6 Core Arm Cortex
Arm Cortex A78
Arm Cortex A78
Arm Cortex A78
500KB L1
2MB L2
4MB L3
Arm Cortex A78
Arm Cortex A78
Arm Cortex A78
GPU
2048-core NVIDIA Ampere architecture GPU with 64 Tensor Cores
[167 TOPs (INT8)]
Audio/Video
Audio Processor (TDA4VM)
ARM Mali-C78AE (ISP)
Video Encoder
Video Decoder
C7x DSP
Input -Output
SPI
I2C
UART
CAN
GPIO
I2S
CSI

An Advanced Driver Assistance System (ADAS) typically comprises four major components:

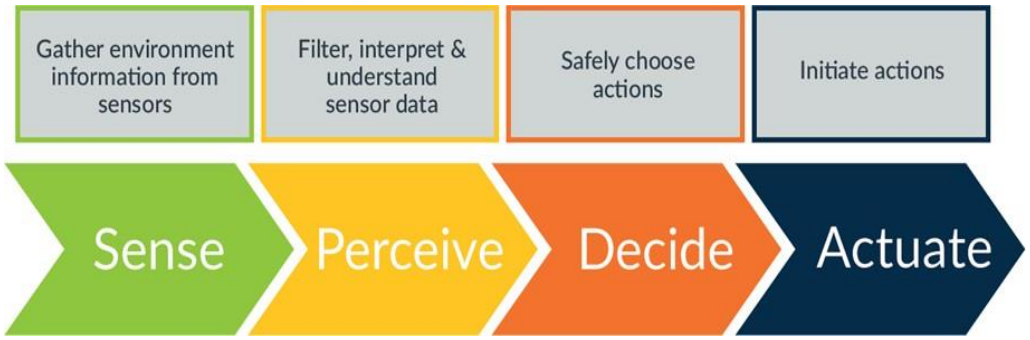


Figure 1: Components of ADAS

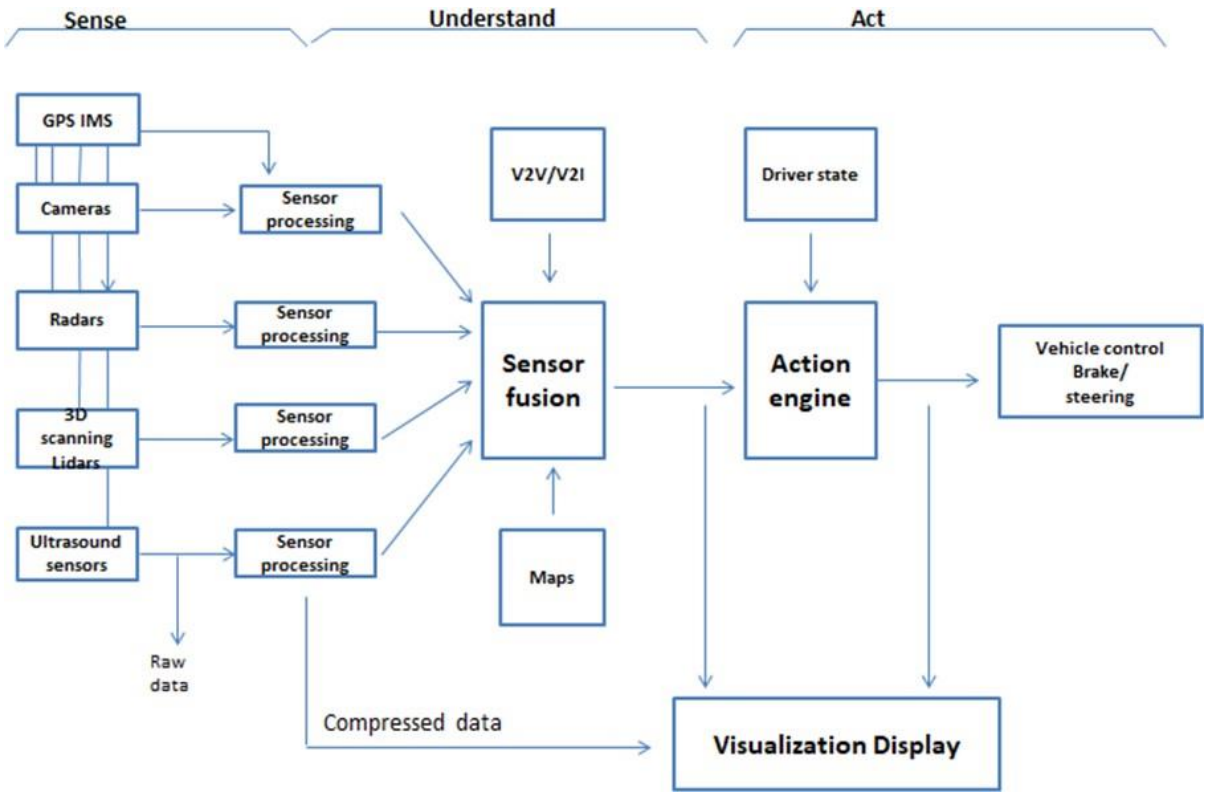


Figure 2: Flow diagram

1.1 CPU (Central Processing Unit) Chiplets:

In ADAS system, the CPU chiplet does the processing of data, runs various algorithms and manages other components of the whole ADAS system. It is also responsible for the various computations

happening around. The functions of the CPU are –

- Sensor data processing: ADAS relies on data from a variety of sensors such as cameras,
  radars, lidars and ultrasonic sensors. The CPU processes data input from these sensors to
  understand the vehicle's environment, detect objects, and make decisions based on the data provided by the sensors.
- System Management: The CPU is responsible for managing the functioning of the system, including memory allocation, power management, and system diagnostics for other chiplets.
- Decision making: Based on the understanding gained by analysing the data given by the sensor data processing data unit, the CPU makes decisions and tells the vehicle to take
  appropriate actions, such as adjusting the steering of the vehicle, braking, or accelerating.
- Communication: The CPU manages communication between different elements of the ADAS system. This involves communicating with other ECUs (electronic control units), other
  chiplets and external servers to receive updates or transfer data to the cloud.

The CPU chiplet which we've used consists of 6 Arm Cortex A78 CPU and we've used 2 such chiplets to maintain the trade-off between area vs thermal efficiency.

1.2 GPUs (Graphic Processing Units) chiplets:

In ADAS system, GPUs (Graphics Processing Units) play an important role in executing graphics and parallel processing tasks. Although the primary role of the GPU is generally related to image

processing for display purposes, in an ADAS system the GPU can be used for a variety of

computational tasks related to images and clusters. Here are some key features of GPU chiplet in ADAS systems-

- Computer vision: ADAS systems rely on computer vision algorithms to interpret data from a variety of sensors such as cameras, radar, and lidar. GPUs accelerate computer vision tasks including object detection, line tracing, and spatial perception. The parallel processing capabilities of GPUs are particularly important for processing large amounts of image and sensor data in real time.
- Image and video processing: GPUs are good at rendering and processing image and video files as compared to CPUs. In ADAS, the GPU is involved in tasks such as image enhancement, noise reduction, and colour correction. It helps improve the quality and clarity of the data the camera sees.
- Neural network inference: ADAS system uses machine learning and deep learning models to perform tasks such as object recognition, pedestrian detection, and gesture recognition. GPUs are ideal for running these neural networks and complex algorithms so that the decisions can be executed faster and more efficiently.

- Real-Time Processing: ADAS applications require real-time processing to quick decisions in response to changing road conditions as the conditions on road are quite unpredictable. The parallel processing capabilities of GPUs help ensure timely execution of computations, contributing to the system's responsiveness.

1.3 Deep Learning Accelerators (DLA) Chiplets:

Deep learning accelerators in ADAS play a crucial role in enhancing the performance and efficiency of machine learning algorithms, particularly deep neural networks (DNNs). They offer specific advantages over general-purpose GPUs (Graphics Processing Units) when it comes to handling machine learning workloads, plus they are much more power efficient as compared to GPUs and help in offloading the work from CPU and GPU. Here are few important uses of deep learning accelerators in ADAS systems:

- Specialized Architecture for Neural Networks-Deep learning, such as custom ASICs (application-specific integrated circuits) or NPUs (neural processing units), are designed to focus on the performance of specific tasks

involved in neural networks. Their architectures are optimized for tasks such as matrix multiplication and convolution, which are common in deep learning models.

- Real-Time Processing: Deep learning accelerators are generally designed so as to minimise the latency and maximise high-throughput inference, helping to improve performance. This is important in ADAS applications where timely decision making is important to ensure vehicle's safety.
- Power Efficiency: DLA's generally use less power than CPUs and GPUs; This reduces power consumption, extends battery life, and reduces cooling requirements for ADAS systems.
- Scalability: As the complexity of Deep Learning algorithms continues to increase, DLA's can be scaled to handle larger models, making them more flexible, allowing ADAS systems to meet new advances in artificial intelligence and becoming more advance.

1.4 Vision Accelerator Chiplets:

Vision accelerators in ADAS plays an important role in improving the visual information. These accelerators are special devices designed for improving computer vision, image processing and

object recognition related tasks. Here are some key points about how vision accelerators work in ADAS systems:

- Accelerate computer vision related Tasks: Vision accelerators are optimized for computer vision, which is the foundation of ADAS capabilities. These tasks include object detection, lane keeping, traffic awareness and other visual functions necessary to understand the vehicle's surroundings.
- Optimization: Vision accelerators are optimized for vision processing, allowing them to provide better performance and performance compared to general-purpose GPUs or CPUs. While deep learning is still optimized for specific tasks, it may not be as specific to CV work as vision accelerators.

Difference between GPU, DLA and Vision accelerators are –

GPU (Graphics Processing Unit):

- Focus: General-purpose parallel computing
- Optimization: Numerous for various tasks, including image processing etc.
- Compatibility: Wide range of applications and frameworks

DLA (Deep Learning Accelerator):

- Focus: Accelerating deep learning algorithms and deep learning tasks
- Optimization: Specialized for specific deep learning tasks and models
- Compatibility: Compatible with popular machine learning frameworks and libraries used for deep learning tasks

Vision Accelerator:

- Focus: Accelerating vision-related tasks and machine learning for computer vision
- Optimization: Specialized for vision-related tasks and optimized for efficiency
- Compatibility: Designed to work with popular machine learning frameworks for computer vision like Open CV and various other CV related modules.

1.5 Flash Memory Chiplet:

NOR Flash and HYPERFLASH memory are the two types of memory that we've included in our Memory Specific Chiplet.

1. NOR Flash Memory:

- Boot Code Storage: NOR Flash Memory is mainly used to store the boot key and firmware required for startup and initialization of the ADAS system. It provides persistent storage, allowing the system to retain this code even when power is removed.

- Firmware Storage: ADAS systems often contain firmware that controls various components, sensors, and subsystems. NOR flash memory can be used to store firmware, making it accessible even when power is turned off or when the system is reset.
- Code Execution: Some microcontrollers or processors in ADAS systems can execute code directly from NOR flash memory. This helps speed up startup time and improve code efficiency.
- Reliability and Durability: NOR flash memory is known for its reliability and durability. NOR flash memory will be a suitable choice in ADAS applications where access to stored codes and important data is easy and consistent.
- Random Access Capability: NOR flash memory allows random access to any storage location, making it suitable for applications that require quickly accessing numbers or files without needing to read the entire memory.

2. HyperFlash memory:

- High speed data storage: HyperFlash is a type of NOR flash memory designed for high-speed data storage. It is especially suitable for applications that need to read a lot of data quickly.
- Major Services: In ADAS systems where large files, maps or other data need to be stored, HyperFlash can be used to provide rapid understanding of this information and thus improve the overall performance of the system.
- Parallel Interface: HyperFlash memory usually has a parallel interface that allows high bandwidth data transfer. This is useful in ADAS applications where rapid data access is required, such as imaging or real-time decision making.
- Code Execution and Data Storage: HyperFlash can be used to store code execution and data storage. This flexibility makes it suitable for applications requiring high-speed processing and efficient data access.
- Multi-Chip Package (MCP): HyperFlash memory is sometimes combined with other memory types or devices into a Multi-Chip Package (MCP). This integration can provide a solution to the limited ADAS space.

3.Memory Chiplet (UFS Memory) (256 GB):

- Data storage: UFS memory is used to store the general data in ADAS systems. It stores firmware, software, maps and other information necessary for operation. UFS provides immutable data storage that protects data even across power lines.
- High-speed data transfer: UFS supports high-speed data transfer, making it suitable for applications that require high-speed data access. This is important for timely processing of sensor data and decision making in ADAS.
- Reliability and Durability: UFS memory is known for its reliability and durability, which is important for automotive storage. The system must be able to withstand extreme conditions.
- Low latency: UFS memory helps improve the response of ADAS systems by providing low-latency access to stored data. Low latency is important for applications that require instant decision making.
- Secure Storage: UFS memory can include security features to protect sensitive data, thus highlighting the importance of data security in ADAS applications.
- Application Data Storage: UFS memory can store specific application data used by various ADAS functions. This includes information about navigation, driver assistance algorithms and physical settings.

Differences between NOR Flash, HYPERFLASH and UFS Memory –

- Speed: NOR flash memory and HyperFlash memory generally provide faster read and write speeds compared to UFS memory.
- Capacity: NOR flash memory and HyperFlash memory generally have more capacity than UFS memory, providing more storage space for data and code.
- Power consumption: NOR flash memory and HyperFlash memory use less power than UFS memory when idle, which can reduce ADAS power consumption and reduce power output.
- Cost: NO flash memory and HyperFlash memory are generally more expensive than UFS memory due to their larger capacity and faster speed.

- Applications: NOR flash memory is mainly used to boot and store important data, while HyperFlash memory is used to store large amounts of data and machine learning models. UFS memory is used for many purposes, including data storage, code execution, and firmware updates.

In conclusion, NOR flash memory, HyperFlash and UFS memory all have their own advantages and are used for different purposes in ADAS systems depending on the specific requirements of the system.

1.6 Memory Controller chiplet:

The memory controller which we've used is Rambus GDDR6 controller core which is a high-speed memory controller that enables efficient data transfer between GPU and memory in ADAS systems. Some of its key features include:

- Memory Interface: Rambus GDDR6 controller core interfaces with the GPU and memory system to facilitate high-speed data transfer.
- Data buffering: The controller core buffers data between the GPU and memory. System memory for smoother data transfer and reduced latency.
- Power efficiency: GDDR6 memory interface uses less power than previous memory interfaces; This can reduce power consumption and reduce power consumption in ADAS systems.
- Compatibility: The Rambus GDDR6 controller core is designed for use with GDDR6 memory modules, which provide increased bandwidth and lower power compared to previous memory technologies.

To summarize, the Rambus GDDR6 controller is crucial for the ADAS system that we've proposed, providing efficient data transfer between GPU and memory, improving overall performance and

reducing power consumption.

1.7 Wireless connectivity chiplet:

In the architecture that we've proposed, we have used 5G, GSM, NXP 88Q9098 Wi-Fi 6 and Bluetooth modules which play an important role in ADAS systems, allowing the system to

communicate with the outside world and other equipment. Some of its key features include:

- Connectivity: These communications enable ADAS systems to connect to the internet, other vehicles, and infrastructure, allowing them to access information, receive updates, and communicate with other systems.
- Data transmission: Communication modules transmit data between the ADAS system and other devices (such as cameras, sensors and control systems) for the proper operation of the system.
- Voice communication: Some communication modules (such as GSM modules) provide voice communication between the driver and other vehicles or in case of emergency services.
- Remote access: The communication module allows remote access and control of the ADAS system, allowing the driver to monitor and control the system.
- Security: Some communication modules, such as 5G modules, support optimal security to ensure data privacy and secure communication between the ADAS system and other devices.

In short, communication modules such as 5G, GSM, NXP 88Q9098 Wi-Fi 6 and Bluetooth are important components for the ADAS system and ensure that the system is well connected with the world, other vehicles and other devices, thus increasing its functionality, safety and security.

1.8 Power management chiplet:

In our Power Management Chiplet, we have used MAX20414 PMIC (Power Management Integrated Circuit) which is a key component of the ADAS system and is responsible for managing power distribution and optimization in the system. Some of its key features include:

- Voltage Regulation: The MAX20414 PMIC controls the voltage levels of various components in ADAS systems to ensure efficient and effective operation.
- Power Management: The PMIC optimizes power distribution between different components of the system, enabling the ADAS system to run efficiently without using much power
- Battery Management: MAX20414 PMIC monitors battery health and performance to ensure efficient power consumption and long battery life that is being used in the car.

- Safety Features: PMIC includes safety features such as overcurrent protection and short circuit detection to protect the ADAS system and its components from getting damaged.
- Communication: The MAX20414 PMIC also communicates with other chiplets in the ADAS system, allowing it to monitor and control its overall operation effectively.

In short, MAX20414 PMIC which is the main element of the power management chiplet in our ADAS system is responsible for: managing energy distribution and optimization, ensuring efficient operation and protecting the body from damage.

1.9 Audio-Video Chiplet:

In our audio - video chiplet we have added modules to process audio and digital signals for the other chiplets to process upon.

The components include—Audio Processor [TDA4VM], ARM Mali-C78AE (ISP), Video Encoder, Video Decoder, and C700 DSP—These play a crucial role in processing audio and video data in an Advanced Driver Assistance System (ADAS). Let's break down the use of each component:

Audio Processor [TDA4VM]:

Use:

The Audio Processor [TDA4VM] is designed to handle audio processing tasks within the ADAS system.

Key Functions:

- Audio Input Processing: The processor can handle inputs from various audio sources, such as microphones which are placed outside the car for adas system or even for in-car audio systems.
- Audio Output Processing: It processes and optimizes audio signals for Driver Assistance Information, collision avoidance alerts, navigation guidance and other audio output devices.
- Audio Signal Processing: The TDA4VM may include algorithms for noise cancellation, echo reduction, and other signal processing tasks to enhance audio quality for Audio Input processing.

- Voice Recognition: It could even support voice recognition capabilities, allowing the ADAS system to respond to voice commands.

ARM Mali-C78AE (ISP):

Use:

The ARM Mali-C78AE is an Image Signal Processor (ISP), which is primarily used for processing image and video data from cameras and other sensors.

Key Functions:

- Camera Image Processing: The ISP handles image processing tasks, such as color correction, exposure control, and white balance to the input obtained from various camera sensors, to ensure high-quality input from cameras to other processor chiplets.
- Computer Vision: It assists other chiplets in computer vision tasks for (GPUs, Vision Accelerator), including object detection, lane departure warning, and other vision-based ADAS features.
- Sensor Fusion: The ISP can integrate data from multiple sensors, such as cameras and radar and lidar, to provide a more comprehensive understanding of the vehicle's environment to create a 3D map of surroundings followed by which, all the tasks related to CV are performed.

Video Encoder:

Use:

The Video Encoder is responsible for compressing video data before transmission or storage.

Key Functions:

- Compression: The encoder compresses raw video data into a more efficient format, reducing the amount of data that needs to be transmitted to other chiplets. The Video Encoder is responsible for compressing video data into a smaller format i.e H.264 for our system, enabling efficient storage and transmission of video data.
- Transmission: Compressed video data can be transmitted over communication networks that are being used in our ADAS system or stored in memory for later use.

- Bandwidth Optimization: Video compression is crucial for optimizing bandwidth usage in applications such as video transmitting video data in real-time.

Video Decoder:

Use:

The Video Decoder is responsible for decompressing video data for playback or further processing.

Key Functions:

- Decompression: The decoder reverses the compression process, restoring the compressed video data to its original format. The Video Decoder is responsible for decompressing video data from a compressed format like H.264, and converting it back into its original format for display or for further processing by other chiplets.
- Playback: Decoded video data can be displayed on in-car infotainment or other display screens or used for computer vision tasks within the ADAS system.
- Real-Time Processing: The ability to decode video data in real-time is essential for applications such as ADAS cameras or object detection using video feeds.

C700 DSP:

Use:

The C700 DSP (Digital Signal Processor) is a specialized processor designed for digital signal processing tasks.

Key Functions:

- Signal Processing: The DSP can handle complex signal processing tasks, such as filtering, modulation, and demodulation, which are essential for audio and video processing.
- Accelerated Processing: The DSP can offload specific tasks from the main processor (CPU), providing accelerated processing for tasks like audio and video processing in real-time.

To summarise, these components work together to enable comprehensive audio and video processing capabilities in ADAS systems. The Audio Processor, ISP, Video Encoder, Video Decoder, and DSP contribute to tasks ranging from handling audio input/output, image signal processing, video compression and decompression, to accelerated signal processing tasks critical for ADAS

functionalities. Their integration enhances the system's ability to perceive and respond to the vehicle's environment.

1.10 Input-Output chiplet:

In the context of ADAS,input-output (I/O) chiplets are used for various communication and interface protocols are used to control the input and output functions of different components. Let's examine the role and features of I2C, SPI, UART, CAN, GPIO and I2S in the context of ADAS:

1. I2C (Inter-Integrated Circuit):

Use in ADAS:

I2C is commonly used for communication between different components within the ADAS system, such as for sensors, cameras, or other peripherals.

Characteristics:

- Bus Structure: Two-wire bus (SCL for clock and SDA for data).
- Master-Slave Configuration: Supports a master-slave architecture.
- Addressing: Devices on the bus have unique addresses.
- Data Transmission: Supports multiple data rates (Standard, Fast, High-Speed).
- Applications: Connecting sensors like cameras ,lidar, EEPROMs, real-time clocks (RTCs), and other peripherals.

2. SPI (Serial Peripheral Interface):

Use in ADAS:

SPI is employed for high-speed communication with peripherals that require fast data transfer rates, such as displays, cameras, or memory devices.

Characteristics:

- Bus Structure: Four-wire bus (MOSI, MISO, SCK, SS for Slave Select).
- Master-Slave Configuration: Typically operates in a master-slave configuration.
- Full-Duplex Communication: Supports simultaneous data transmission and reception.
- Data Transmission: Variable data formats, configurable clock polarity and phase.
- Applications: Connecting wireless modules, and peripherals requiring high-speed communication.

3. UART (Universal Asynchronous Receiver-Transmitter):

Use in ADAS:

UART is used for serial communication with devices that require asynchronous data transfer, such as GPS modules or certain sensors.

Characteristics:

- Point-to-Point Communication: Typically used for point-to-point communication.
- Asynchronous Communication: No shared clock; uses start and stop bits.
- Baud Rate: Configurable baud rates for communication speed.
- Applications: Connecting to GPS modules, certain sensors, and other devices requiring serial communication.

4. CAN (Controller Area Network):

Use in ADAS:

CAN is widely used in automotive applications for communication between ECUs (Electronic Control Units) and other components.

Characteristics:

- Differential Bus: Uses a differential bus for robustness in noisy environments (noisy as in having noisy signals).
- Multi-Master Communication: Supports a multi-master architecture like ours.

- Priority-Based Communication: Messages have priority levels for efficient data transmission.
- Applications: In-vehicle communication between ECUs or in between chiplets, including ADAS components.

5. GPIO (General-Purpose Input/Output):

Use in ADAS:

GPIO pins are used for general-purpose digital input or output, such as controlling LEDs, buttons, or interfacing with other digital devices.

Characteristics:

- Digital I/O: Supports digital input and output operations.
- Configurability: Configurable as input or output based on system requirements.
- Applications: Controlling LEDs, buttons, interfacing with digital sensors, and general-purpose digital I/O.

6. I2S (Inter-IC Sound):

Use in ADAS:

I2S is used for transmitting digital audio data between components, such as microphones, audio processors, or speakers .

Characteristics:

- Serial Audio Interface: Designed for serial communication of audio data.
- Synchronous Communication: Uses a synchronous clock for precise audio data transfer.
- Separate Data and Clock Lines: Typically includes separate lines for data and a bit clock.
- Applications: Connecting microphones, audio processors, speakers, and other audio-related components.

7. MIPI CSI-2:

MIPI CSI-2 (Mobile Industry Processor Interface Camera Serial Interface 2) is a popular protocol used to transmit video and image data in a variety of applications, including ADAS. MIPI CSI-2 is designed to transfer data from image sensors to application processors or other image processing devices.

The main points of the MIPI CSI-2 protocol are:

- Purpose: MIPI CSI-2 is specifically designed for camera interface implemented in mobile devices, automotive systems including ADAS and other applications.
- Serial Interface: MIPI CSI-2 is a high-speed serial interface that transmits image and video data between the camera sensor and the operating processors chiplets. It uses differential signaling to transmit data, reducing the number of wires compared to parallel interfaces.
- Data transmission: MIPI CSI-2 uses data transmission in packets. Image and video data is divided into packets, each packet contains synchronization information, payload information and control information. This packaging ensures efficient data transmission and helps synchronization between the camera and receiver.

In an ADAS system, these communication and interface protocols work together to enable seamless connectivity and data exchange between various components. Each protocol has its strengths and is chosen based on factors such as data transfer speed, distance, and the specific requirements of connected devices within the ADAS architecture.

Analog Unit:

The analog unit which we've made consists of DAC (Digital to Analog Convertors) , ADC (Analog to Digital Convertors), Signal filters,Amplifiers which are mainly focused on performing basic operations on the input signals obtained from sensors.

ADCs: ADCs are used to convert analog signals, such as those generated by sensors, into digital data that can be processed by the other chiplets used for ADAS.

DACs: DACs are used to convert digital data back into analog signals for output to other chiplets which process these signals .

Filters: Filters are used to remove unwanted noise and frequencies from the sensor signals before they are processed by the chiplets in ADAS .This helps improve the accuracy and reliability of the sensor data. Common types of filters used in ADAS include low-pass filters, high-pass filters, and band-pass filters.

Amplifiers: Amplifiers are used to increase the signal strength of the sensor signals before they are converted into digital data by the ADC. This ensures that the chiplets involved in our ADAS system can accurately measure the signals even in the presence of noise or weak signals.

In proposed micro-architectural diagram, we can achieve optimal throughput in following ways:

1. Chiplets specialized in specific tasks, allow parallel processing of different functions simultaneously. This parallelism boosts overall throughput as multiple chiplets work on tasks concurrently. In an ADAS system, a CPU chiplet can handle general-purpose computing tasks, while a GPU chiplet can excel in parallel processing for graphics-related computations. AI accelerators can focus on machine learning algorithms for object detection and recognition, and making real-time decisions.

2. Use of efficient and high-bandwidth interconnects like UCIe between chiplets enhances the overall throughput. The UCIe stack itself has three layers. The top Protocol Layer ensures maximum efficiency and reduced latency through flow-control-unit-based (FLIT-based) protocol implementation, supporting the most popular protocols, including PCIe, Compute Express Link (CXL), and/or user- defined streaming protocols. The second layer is where the protocols are arbitrated and negotiated and where the link management occurs through a die-to-die adapter. Based on cyclic redundancy check (CRC) and a retry mechanism, this layer also includes optional error correction functionality. The third layer, the PHY, specifies the electrical interface with the package media.
   This is where the electrical analog front end (AFE), transmitter and receiver, and sideband channel allow parameter exchange and negotiation between two dies. Logic PHY implements the link initialization, training and calibration algorithms, and test-and-repair functionality.
3. With advanced packaging techniques (such as 2.5D/3D packaging), which reduces interconnect lengths, improving signal integrity and enabling faster communication between chiplets, throughput is enhanced.

4. Placing memory closer to processing units reduces access latency. Memory chiplets positioned strategically within the system architecture enable faster data retrieval, hence, high throughput.
5. Mix and match of chiplets to create customized configurations tailored to specific performance or application requirements, ultimately optimizing throughput for different workloads [Sensors – 28nm, CPU & GPU – 7 to 14 nm, AI accelerator – 7 to 5 nm or even smaller]

1.11 Redundant Chiplets:

A redundant chiplet refers to a duplicate or backup chiplet within a chiplet-based system that serves as a fail-safe mechanism.

Multiple identical chiplets like CPUs, GPUs, AI accelerators enhance compute power at the same time act as redundant chiplets in case of any failure in any of identical chiplets. If one of them fails or experiences an issue, the workload can be redistributed or managed by the remaining functional chiplets.

2. SPECIFICATION OF PROCUREMENT OF COMPONENTS:

The above-mentioned architecture comprises distinct chiplets dedicated to various components. An inherent benefit of chiplet technology is its independence from the need for a single company to create all the components. By utilizing a standardized interconnect technology such as UCIe, the potential to combine and interchange various components is enabled.

The objective, as stated in the problem statement, is to enhance the efficiency of the procurement process for various components. From a resource management perspective, it is more efficient to procure pre-designed components from manufacturers who specialize in their production. To prioritize certain components, which are reliant on the unique application or offer potential for customisation, JLR could consider creating their own designs in collaboration with their partners.

According to our research and analysis, the plan to implement the proposed design is as follows:

2.1 Components JLR should outsource:

1. CPUs:

A CPU, or central processing unit, serves as the brain of a computer system, handling a wide range of general computing tasks. Its versatility lies in its ability to execute a diverse array of instructions and perform computations across various applications. Unlike specialized processors designed for specific tasks, a CPU is a general-purpose processor that can adapt to different workloads and applications. Although it is undeniably a crucial element of the system, it does not necessarily have to be highly tailored to a certain application.

Designing a CPU involves a complex and intricate process that requires a high level of skill, expertise, and resources. The significant costs associated with CPU design are attributed to various factors involved in the research, development, and production phases. These include:

- Research and Development
- Intellectual Property(IP) costs
- Advanced Manufacturing Processes
- Skilled Workforce
- Prototyping and testing
- Development time and iteration

The CPU need not be application specific. CPUs with good enough specifications exist in the market which can be implemented in ADAS systems.

Therefore, it is advisable for JLR to subcontract the central processing units (CPUs) that fulfil the specified requirements outlined in the architecture. We have suggested using a 6-Core Arm Cortex A-78 processor. Its specifications are as follows:

ISA support	A64 A32 and T32 (at EL0 only)
Max number of CPUs in cluster	4
Physical Addressing(PA)	40 bit
L1 Cache	32Kb to 64Kb
L2 Cache	256Kb to 512Kb
L3 Cache	4 MB
ECC Support	Yes
LPAE Support	Yes
Bus Interfaces	AMBA ACE or CHI

2. GPUs:

GPUs are a crucial element of the system that performs the intensive computational tasks involved in handling image and graphic data.

Enhancing the GPU for ADAS (Advanced Driver Assistance Systems) applications could potentially enhance the performance. However, it is crucial to consider the resources involved in GPU design. The research and development process required for designing GPUs is quite costly, which would consequently lead to a higher price for the automobile. This would be unfavourable from a customer's perspective.

Given the GPUs' ability to handle a wide range of machine learning and deep learning models for different applications such as image processing, sensor fusion, and object recognition, it does not seem worthwhile to invest in customizing the GPUs for a minimal improvement in performance.

Therefore, it is advisable to go for pre-existing GPU chiplets available in the market.

Some standard GPU configurations being used currently in the automotive industry such as the GPUs used in the Nvidia Orin Series bundle will be suitable.

No. of Graphics Processing Clusters	2
No. of Texture Processing Clusters	8
No. of Nvidia CUDA cores	2048
No. of Tensor cores	64
Clock frequency	1185.75 MHz
Interconnect Bus	PCIe 4.0 x4

3. Memory (Controller,DRAM, Flash, ROM):

Memory is a ubiquitous component found in practically every chip or system-on-a-chip (SoC). It serves a wide range of purposes and is not specialized for any specific task.

Outsourcing with the appropriate configuration is necessary, as it will not serve as a distinguishing factor in the performance and functioning of the system.

The investment-to-outcome ratio would be exceedingly low in this particular scenario.

The Rambus GDDR6 would be a good choice for the memory controller. It supports a speed data rate of up to 24Gb/s, maximizes memory bandwidth and minimizes latency with the help of Look-Ahead command processing. It is full run-time configurable for timing parameters and memory settings and supports automatic and controller-initiated training. Supports AXI connect technology.

4. AI Accelerators:

Similar to GPUs, AI accelerators necessitate extensive research and development for their design and creation.

Companies like Nvidia, Intel, AMD, Qualcomm, and others possess specialized knowledge in creating accelerators capable of supporting a diverse array of applications, including ADAS.

Therefore, it is advisable for JLR to get the accelerator chiplet from the market.

Since we have suggested Nvidia GPU used in the Orin package, using the bundled set of accelerators i.e. Nvidia DLA v2.0 would be good for easier integration. It has a max frequency of 1408 MHz.

5. Analog chiplet:

In a chiplet architecture, analog chiplet performs functions like:

- Boost weak signals for digital processing.
- Convert and regulate power for stable operation.
- Bridge the gap between analog sensors and digital systems.
- Control and interface with sensors and actuators.
- Perform specialized tasks like signal processing and MEMS control.
- Increasingly integrated for efficient and compact designs.

Most of the tasks performed by the chiplet are generic and there is not a great need for customization, on an application level.

JLR should focus more on other chiplets like Security, Audio/Video, etc mentioned below, rather than expending resources and investing in R&D of analog chiplet. Hence, JLR should consider outsourcing this chiplet.

2.2 Components JLR should design and customize:

1. I/O chiplet:

An I/O chiplet in an architecture serves the crucial role of managing communication with external components like memory, storage, and other devices. It acts as the bridge between the internal processing cores and the outside world, facilitating data transfer and enabling the system to interact with its environment.

Some key features of I/O chiplet are:

- High-speed data transfer: PCIe, DDR, Ethernet, and even optical I/O for ultra-high bandwidth.
- Peripheral communication: Sensors, actuators, displays, specialized protocols, and dedicated resources.
- Modular design and flexibility: Add or remove I/O functionalities, customize systems, and upgrade easily.
- Improved performance and efficiency: Offload tasks, optimize power, and reduce main processor complexity.

Specific to JLR applications, I/O plays an important role in luxury cars like the ones manufactured by JLR. Some key I/O requirements needed from automotive point of view include:

1. High-speed data transfer:

- High-bandwidth networking: JLR automobiles are equipped with sophisticated infotainment systems, driving assistance technologies, and telematics that necessitate high-speed connection capabilities. This involves the provision of assistance for various protocols such as Ethernet, Wi-Fi, and cellular networks, which possess advanced capabilities in terms of 5G/6G connectivity.

2. Human-machine interface (HMI) I/O:

- Luxury cars are equipped with spacious, high-resolution touchscreen displays that serve for infotainment, navigation, and vehicle settings.
- Enhanced by advanced voice control, the car's systems can be interacted with hands-free, providing both convenience and safety benefits.
- Haptic feedback refers to the use of tactile sensations, such as vibrations or pressure, transmitted through steering wheels, chairs, and other surfaces. This type of feedback serves to convey intuitive information to the user and improves their overall experience.

3. Customized I/O:

- Luxurious automobile manufacturers frequently provide customisation choices, enabling customers to personalise the interior lighting, audio system, and other characteristics of the vehicle. This necessitates adaptable input/output capabilities to support various combinations.
- To fully integrate all these functionalities, we suggest that JLR invest in the development of a tailored I/O chiplet design.

In addition to these core requirements, luxury cars may also incorporate other advanced I/O features, such as:

- Biometric authentication: Fingerprint scanners or facial recognition systems can be used for secure access and car personalization.

- Augmented reality (AR) displays: These can provide information and warnings directly in the driver's field of vision, enhancing safety and awareness.
- Wireless charging: This allows for convenient charging of smartphones and other devices without the need for cables.

Therefore, it is necessary for JLR and its partners to develop a specialized I/O chiplet that is built upon the aforementioned architecture. This could help enhance the end user experience and differentiate in the high-cost market compared to other luxury car manufacturers.

2. Security chiplet:

- As stated in the issue statement, security is a critical aspect in automotive applications where human lives are at stake.
- Ensuring robust security measures is crucial for the chiplets in order to protect against cyber threats.
- According to the suggested security protocol, it is more advantageous for JLR to develop this chiplet exclusively in order to have greater control over the security of the system. We have later elaborated on the security strategy used and included specifications on the type of chiplet to use. More details can be found there.(Part 2.2.b of the Problem statement).

3. Audio/Video chiplet:

The audio/video chiplet is a crucial component in high-end autos. It has the potential to significantly distinguish JLR from its competitors.

Some important functions that the A/V chiplet performs are:

- Processing audio and video signals
- Interfacing with audio and video peripherals
- Offloading tasks from the main processor
- Enhancing audio and video quality

- Enabling advanced multimedia features such as AR, VR, hardware acceleration for video editing and transcoding, multi-display setups, etc.

It directly facilitates multimedia services such as In-Car Entertainment, driver-monitoring, surround-view camera displays, augmented reality displays, parking assistance, and gesture recognition.

This chiplet is one of the components that will directly influence the user experience.

Therefore, tailoring and enhancing this chiplet in accordance with JLR's UI software can contribute to delivering a more immersive user experience, which is a key requirement for luxury automobile purchasers.

4. Power Management chiplet:

Efficient power management is a crucial function that can have a significant impact on the overall system performance.

Functions carried out by the power management chiplet include:

1.Power Delivery

- The power management chiplet efficiently delivers power to the various ADAS components, including sensors, cameras, radars, and LiDAR units.
- It ensures the stable and uninterrupted supply of power, even under demanding environmental conditions.
- This is crucial for the continuous operation of ADAS features like lane departure warning, adaptive cruise control, and automated emergency braking.

2.Power Optimization:

- The chiplet optimizes power consumption by dynamically adjusting power supply based on the real-time needs of the ADAS system.
- This reduces energy waste and improves overall battery efficiency, especially important for electric and hybrid luxury cars.

- Additionally, power optimization helps maintain optimal temperature levels for the ADAS components, preventing overheating and ensuring reliable performance.

3.Fault Tolerance:

- The power management chiplet continuously monitors power parameters and detects any anomalies or potential failures.
- It can implement fault tolerance mechanisms like automatic power isolation or redundancy switching to maintain ADAS functionality in case of a problem.
- This ensures the system's safety and reliability, preventing accidents caused by ADAS malfunction.

Designing power management for a system requires less effort compared to designing a CPU/GPU.

Therefore, it is imperative for JLR to develop an efficient power management chiplet that takes into account all the power needs of the proposed architecture.

3. LATENCY AND COMMUNICATION EFFICIENCY

The Universal Chiplet Interconnect Express (UCIe) used for the heterogeneous integration of chiplets with different functionality, process nodes, and different material. UCIe is the only standard with a compatible stack for die-to-die interface.The UCIe interconnect is designed to accommodate a wide range of designs, supporting data transfer speeds from 8 Gbps to 16 Gbps per pin.

It offers two package variants such as Advanced and Standard packages.

1. UCIe Advanced package: It is suitable for applications utilizing silicon interposer, Silicon Bridge, and Redistribution Layer (RDL) fan-out. It is suitable for higher bandwidths, utilizes smaller bump pitches ranging from 25 to 45 micrometers, offering 64 lanes for data transfer and very short channel reaches of under 2mm. Leveraging the 45 µm bump pitch technology, UCIe achieves an impressive linear bandwidth of up to 1.3 TB/s/mm

2. UCIe Standard package: It is geared towards applications using organic substrate and laminate. It is suitable for lower bandwidths and provides up to 16 lanes for data transfer, 100 micrometers+ bump pitches, and extended channel lengths.

Characteristics / KPIs	Standard Package	Advanced Package	Comments
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	
Target for Key Metrics			
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u for AP; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ CXi Flit Mode

Figure 3: UCIe standard package

Our architectural design for ADAS Application consists of the following :

1)High-Performance Processing cores :

- These form the brain of the architecture comprising the CPU and GPU cores, which carry out all the high-compute and graphic processing workloads of the system.
- Chiplet contains a Hexa-core ARM Cortex A78 core configuration with private L1(500KB),a shared L2(2MB) and L3(4MB) cache.
- It also contains a GPU (2048- core NVIDIA Amphere artitecture GPU with 64 tensor flow).

2)Non Volatile memory Chiplets:

- It consists of 32GB DRAM via the UCIe Interconnect.
- The prefetch buffer and load-store buffer send memory access requests via the UCIe interconnect.

3) Volatile Memory:

- The volatile chiplets consist of hyperflash, 256 GB ROM via the UCIe Interconnect.

4)The Memory Controller :

- This chiplet consists of Rmabus GDDR6 controller core with bandwidth of 96GB/sec, speed of 24 GB/sec, power consumption 10mW/Gb/sec, throughput 96Gb/sec.

5)Power Management chiplet :

- It is based on MAX20414 PMIC operating at 2.2 MHz frequency thus providing power regulation, voltage monitoring, battery charging, and other features.
- Ensures efficient power management to maintain high throughput and energy efficiency.

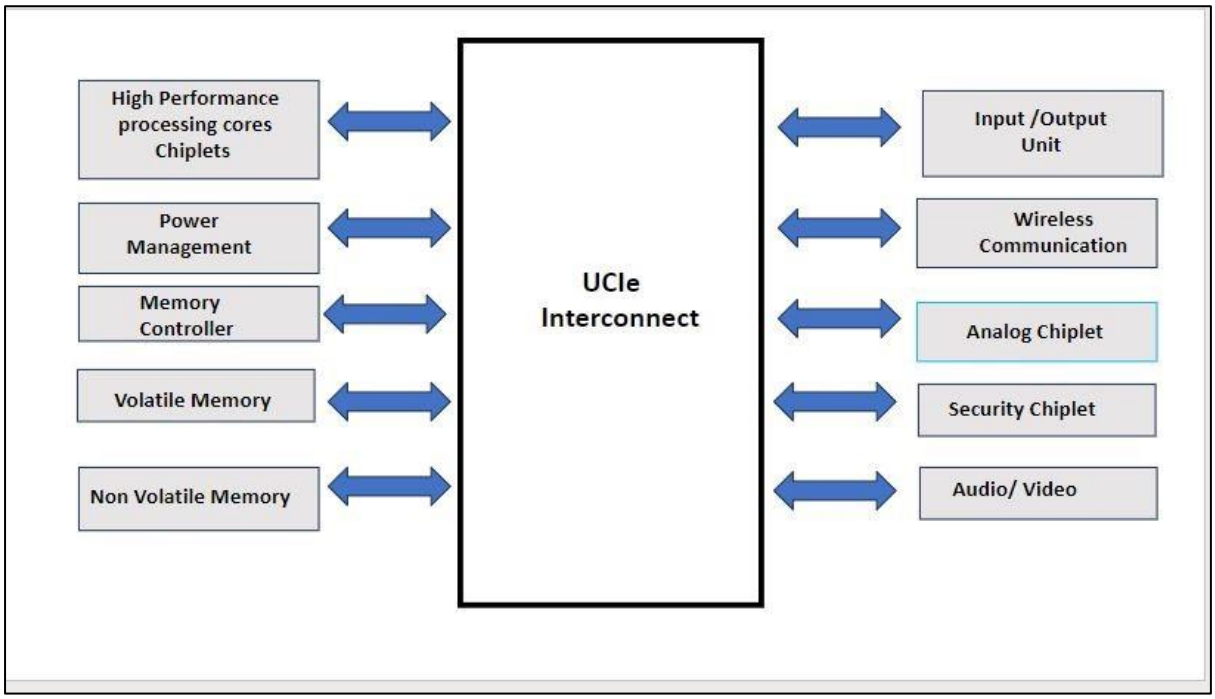


Figure 4: UCIe Interconnect for ADAS Application

6)Audio /Video:

- Audio module consists of TDA4VM Audio processor design to handle audio processing tasks of ADAS system.
- ARM Mali-C78AE(ISP),Video Encoder,Video Decoder and C700 DSP.

7)Input/Output Unit:

- It is used in various communication and interface protocols used to control the input and output function of different components.such as I2C,SPI,UART,CAN,GPIO and I2S in ADAS system.

8)Wireless Communication Chiplet:

- It controls all the wireless communication channels like Bluetooth and Wifi.
- It consists of NXP 88Q9098 Wifi-6 with 2x2 configuration that is providing a speed of 1201 Mbps and throughput of 2.4Gbps and Bluetooth 6 with speed of 2Mits/second.
- QUECTEL 5G & C-V2X AG55xQ Automotive Module series with specifications such as Automotive grade 5G NR sub-6GHz module,Max. downlink 2.4Gbps / uplink rates of 550Mbps under 5G NR,Max. downlink

1.6Gbps / uplink rates of 200Mbps under LTE-A,Extended temperature range of -40°C to +85°C and eCall temperature range of -40°C to +95°C.

9) Analog Chiplet :

- It uses PCIe Gen6 interface, consisting of Digital to analog control unit, signal filter, amplifiers and ADC.
- Hence, to interface it with the UCIe interconnect, corresponding ports were configured with the streaming protocol.

Device	Product description	Key specifications
DAC		
DAC5311-Q1	8-bit, low-power, single-channel DAC	8-bit, single-channel DAC, MicroPower operation, 1.8-V to 5.5-V supply range, serial SPI interface, 6-µs settling time, ±0.25 LSB INL, 80 µA at 1.8 V, –40°C to +85°C
DAC7551-Q1	12-bit, ultra-low glitch, single-channel voltage-output DAC	2.7-V to 5.5-V operation, ±0.3 5LSB INL, 0.1-nV-s glitch, 100 µA at 2.7 V, –40°C to +105°C, SPI digital interface, small form factor and low power operation, 5-µs settling time
DAC8562/63-Q1	16-bit, ultra-low glitch, dual-channel DAC with internal reference	2.7-V to 5.5-V operation, ±0.4 LSB INL, 0.1-nV-s glitch, 4 ppm/°C internal reference, –40°C to +125°C
DAC8162/63-Q1	16-/14-/12-bit, ultra-low glitch, dual-channel DAC with internal reference	16-/14-/12-bit, dual-channel DAC, 4ppm/°C internal reference, 2.7 V to 5.5 V operation, serial SPI interface, 7 µs settling time, ±4 LSB INL (16-bit), 0.1 nV-s glitch, 0.73 mA at 2.7 V, -40°C to +125°C
DAC7562/63-Q1	16-/14-/12-bit, ultra-low glitch, dual-channel DAC with internal reference	16-/14-/12-bit, dual-channel DAC, 4ppm/°C internal reference, 2.7 V to 5.5 V operation, serial SPI interface, 7 µs settling time, ±4 LSB INL (16-bit), 0.1 nV-s glitch, 0.73 mA at 2.7 V, –40°C to +125°C
ADC		
ADS5204-Q1	Dual 10-bit 40-MSPS low-power ADC with PGA	10-bit dual-channel pipeline ADC with on-chip programmable gain amp, up to 40-MSPS sampling, 3.3-V single-supply operation, low power
ADS7955-Q1	10-bit, 1-MSPS, 8-channel, single-ended, MicroPower, sr i/f, SAR ADC	10-bit, 8-channel SAR ADC, 2.7-V to 5.25-V supply range, 1-MSPS sampling with serial SPI interface, 0.5-LSB INL
ADC3422	Quad-channel, 12-bit, 25-MSPS to 125-MSPS, analog-to-digital converter	Quad-channel, 12-bit, 25-MSPS to 125-MSPS, flexible input clock buffer with divide-by 1, 2, 4; SNR = 70.2 dBFS, SFDR = 87 dBc; ultra-low power consumption: – 98 mW/ch at 125 MSPS; channel Isolation: 105 dB

Figure 5: Ports table from reference 22

The overall data transfer rate is given as:

Overall Data Transfer Rate

= Memory Controller Bandwidth + Wifi-6 Speed + 5G NR Max. Downlink Speed + LTE-A Max. Downlink Speed

= 96GB/sec+2.4Gbps+2.4Gbps+1.6Gbps

= 102.4 GB/s

In conclusion, the architecture of the ADAS chiplet system is meticulously designed to prioritize low latency and achieve high communication efficiency with a high overall data transfer rate of 102.4 GB/s. The implementation of the Universal Chiplet Interconnect Express (UCIe) standard plays a pivotal role in enabling heterogeneous integration, accommodating chiplets with varied functionalities, process nodes, and materials.

The UCIe Advanced package, with its utilization of silicon interposer, Silicon Bridge, and Redistribution Layer (RDL) fan-out, stands out for applications demanding higher bandwidths. The impressive linear bandwidth of up to 1.3 TB/s/mm, facilitated by a smaller bump pitch ranging from 25 to 45 micrometers, demonstrates a commitment to high-speed data transfer. The 64 lanes for data transfer and very short channel reaches of under 2mm further contribute to the architecture's low latency attributes. Conversely, the UCIe Standard package is tailored for applications utilizing organic substrate and laminate, providing flexibility for lower bandwidth requirements. This package, offering up to 16 lanes for data transfer, accommodates extended channel lengths and larger bump pitches of 100 micrometers+, showcasing adaptability to diverse communication needs.

The core components of your ADAS architecture, such as the high-performance processing cores, non-volatile and volatile memory chiplets, memory controller, power management chiplet, audio/video module, input/output unit, wireless communication chiplet, and analog chiplet, are seamlessly integrated using UCIe. The inclusion of a Hexa-core ARM Cortex A78 configuration, a powerful NVIDIA Amphere GPU, and efficient memory access through UCIe contribute to the system's overall low latency and high communication efficiency. Furthermore, the Wireless Communication Chiplet's incorporation of advanced technologies like Wifi-6 and 5G, along with the extensive range of communication and interface protocols in the Input/Output Unit, reflects a forward-looking approach to connectivity and communication efficiency.

In essence, the architecture is made with a holistic approach in achieving low latency and high communication efficiency. The careful selection of UCIe packages and the integration of diverse chiplets, each with specialized functions, collectively contribute to a robust system capable of meeting the demanding requirements of Advanced Driver Assistance Systems.

4. CYBERSECURITY ASPECT -

Currently in the market there are some companies providing various security chiplets to ensure hardware root of trust to complete hardware and software solutions reducing integration complexity and efforts. One of them includes CEVA, through its wholly-owned subsidiary, Intrinsix, offers the Fortrix SecureD2D IP, a comprehensive hardware-based solution that uniquely enables secured communication between chiplets in an HSoC. The IP was selected and deployed as part of the Department of Defense State-of-the-Art Heterogeneous Integrated Packaging (SHIP) program and has already been adopted by various companies including Lockheed Martin and a world-leading semiconductor company

Fortrix SecureD2D IP:

Key Features: Secure Boot, Root of Trust, Encryption/Decryption, Secure Communications, Authentication, NSA Suite-B and CNSA level of performance with low power and low latency,

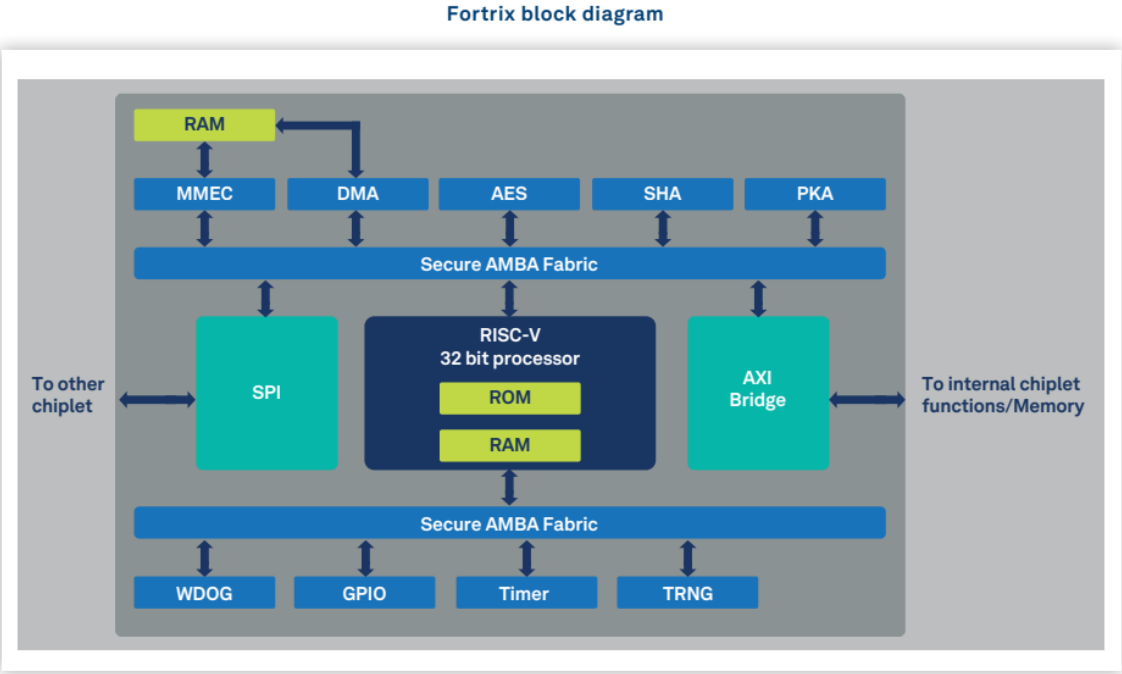


Figure 6: Fortrix Block Diagram

Developing own security chiplets will allow for complete control over the design and implementation, enabling JLR to tailor the solution to its specific needs and requirements.By having its own in-house design, JLR can avoid dependence on a single vendor and maintain greater flexibility in the future. Developing own security chiplets is more efficient as it provides full Control and Flexibility and customisation according to need and reduces the risk of vendor lock-in. If JLR wants to approach in a more time and cost efficient way, it can partner with leading dedicated security chiplet manufacturers. Purchasing pre-built security chiplets allows for faster implementation and deployment, saving JLR's valuable time and resources in design and development.

Based on our thinking the approach for JLR for developing security chiplets should include the features which are currently most efficient in providing secure and reliable communication within chiplets should as follow:

Shielding against physical attack: Anti Tempering desin and Tamper Detection and Response Mechanisms for prevention against Invasive attacks like data scrambling and shuffling, Against Semi invasive attacks like Metal shielding and non invasive attacks like built in secure repair and Access control. In the SoC we have seen various ways of tempering reported by black hat and white hat hackers. The major reason behind it is to leak confidential information like, secret key or any asset. Making the Chiplets Tamper proof protects them from a number of attacks including reverse engineering and Side channel attacks. Protecting the Chiplets in a Tamper proof case can provide a shield to the Chiplets from those attacks. If tampering at the case level is detected, then the system inside the case must take defensive measures.For devices with built-in anti-tampering circuits, it may be possible to configure the tamper responses. The case must provide adequate security against tampering attempts for the enclosed chiplets containing sensitive information. Some countermeasures are physical, while others involve active sensors. Providing evidence of tampering can be helpful during investigations and legal procedure.

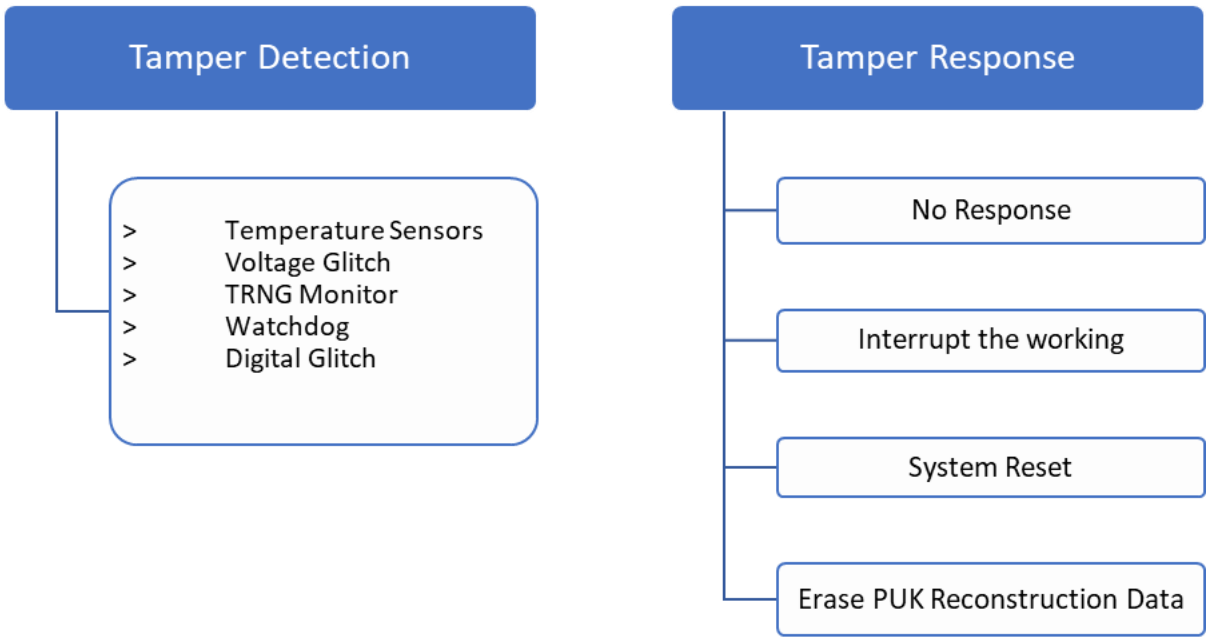


Figure 7: Tampering

Authentication of Chiplets: Secure and reliable communication in the chiplets with others is very essential in the Automobile Sector. As the chiplets are popularizing in the market and a number of companies are starting manufacturing chiplets with various different purposes or functionality, assembling them as one SiP poses some concern about security making authenticating them necessary. Authenticating chiplets if a single company manufactures it is not a big problem But 3rd Party Chiplets there is much possibility for a malicious chiplet getting into. It calls for the authentication of various chiplets on the SiP and allows only genuine authenticated chiplets to perform their actions.To Enhance security and trust in chiplet-based systems and prevent unauthorized access and manipulation of data Physical Unclonable Functions (PUFs) can be a good idea. These leverage unique, inherent physical variations within each chiplet to create a "fingerprint" that cannot be copied. This fingerprint serves as a secure identifier for authentication.

Physically unclonable functions (PUFs) Chip Fingerprinting

Physically unclonable functions (PUFs) are used in hardware security primarily for chip identification and authentication. They are circuits that exploit the inherent

process variations in chip fabrication to generate unique and unpredictable identifiers. These identifiers, also known as chip fingerprints, remain consistent throughout the chip's lifetime and are virtually impossible to replicate.

PUF evaluation metrics:

- Randomness: Difficulty of predicting PUF value
- Uniqueness: Chance of collision between PUFs
- Robustness: Stability of PUF response
- Non-traceability: Resistance to physical attacks

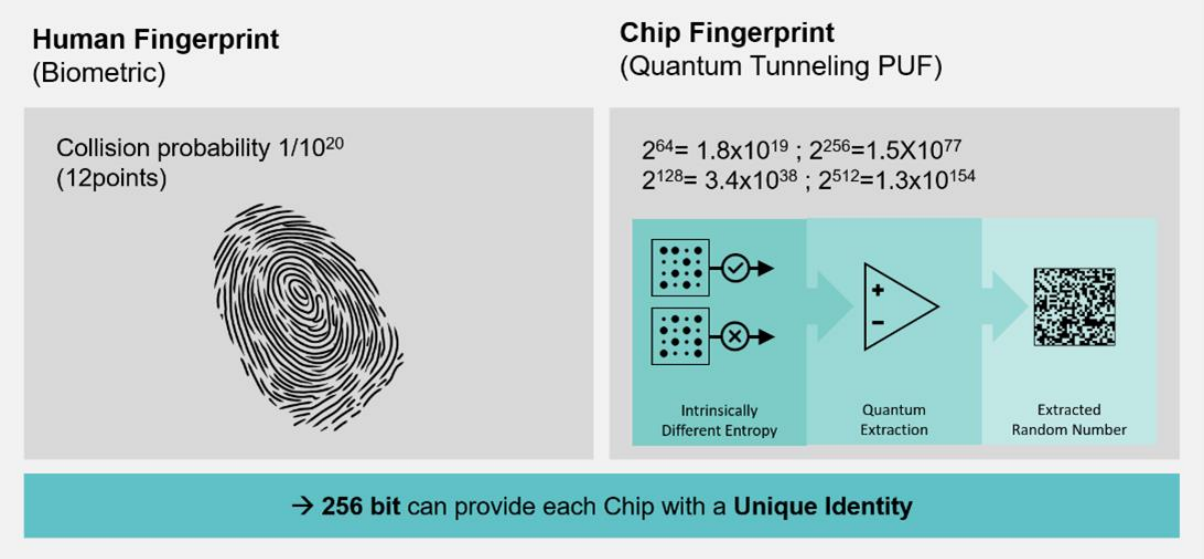


Figure 8: PUFs

Source:https://www.pufsecurity.com/document/securing-system-on-chips-hardware-protection-in-the-age-of-chiplets/

PUFrt - Hardware Root of Trust
100% compatible with any crypto coprocessor to be the root of trust

Four 256-bit hardware PUF fingerprints with self-health check

APB Interface: It is a low-cost, low-power, and simple to use interface designed for communication between a processor and peripheral devices. APB is designed for low-power and low-bandwidth: Security chiplets prioritize low power consumption and security, making APB a more suitable choice. Replacing APB with UCI, which is designed for high-power and high-bandwidth applications,

would increase power consumption significantly and could compromise security.

Hardware Root of Trust:

Hardware-based Root of Trust is a specialized module that acts as a secure enclave, isolated from the main processor and operating system, dedicated to safeguarding the system against unauthorized access and manipulation. This serves as the foundation for critical security functionalities, including Secure Boot ensuring the system boots only from authorized firmware, preventing the execution of malicious code and Key Management. Sensitive cryptographic keys used for encryption, authentication, and digital signatures are securely stored and managed within the RoT.

The value and effectiveness of Hardware-based RoT are not merely theoretical. Several leading companies have embraced this technology and integrated it into their cutting-edge products:

- Infineon AURIX microcontrollers: These microcontrollers, commonly used in automotive applications, leverage a dedicated RoT for secure boot, key management, and communication encryption, ensuring the safety and integrity of critical systems.
- NXP i.MX RT1170 microcontroller: This microcontroller utilizes PUF (Physically Unclonable Functions), a unique identifier generation technology, within its RoT for secure authentication and key generation, bolstering security in diverse applications.
- Renesas R-Car V3H chip: This chip integrates a Secure Processing Unit (SPU) as its RoT, enabling the secure execution of critical functions required for advanced automotive technologies.
- Bosch Sensortec BMI085 inertial measurement unit: This unit utilizes PUFs within its RoT for unique identification and tamper detection, fostering trust in sensor data used in various applications.
- Apple T2 chip: This chip acts as the RoT for Apple Mac computers, providing secure boot, encryption, and Touch ID functionality, enhancing user security and privacy.

Clock Comparators:

In Advanced Driver-Assistance Systems (ADAS), ensuring accurate timing and synchronization between various chiplets within the system is crucial for safe and reliable operation. This is where clock comparators play a critical role.

1. Silicon Labs Si5341:

- Description: This high-performance clock comparator boasts Ultra-low jitter of 90 fs rms and sub-picosecond accuracy, making it ideal for demanding ADAS systems.
- Key Features: Integrated PLL, multiple clock inputs and outputs, phase interpolation, spread spectrum capability. Pb-free, RoHS-6 compliant
- Applications: Clocking for FPGAs, processors, memory; Clock tree generation replacing XOs, buffers, signal format translators

Input frequency range:	
External crystal:	25 to 54 MHz
Differential clock:	10 to 750 MHz
LVCMOS clock:	10 to 250 MHz
Output frequency range:	
Differential:	100 Hz to 1028 MHz
LVCMOS:	100 Hz to 250 MHz
Core voltage:	
VDD:	1.8 V ±5%
VDDA:	3.3 V ±5%
Independent output clock supply pins:	
3.3 V, 2.5 V, or 1.8 V	
Serial interface:	
I2C or SPI	
Temperature range:	
–40 to +85 °C	

Reference Link: https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/data-sheets/si5341-40-d-datasheet.pdf

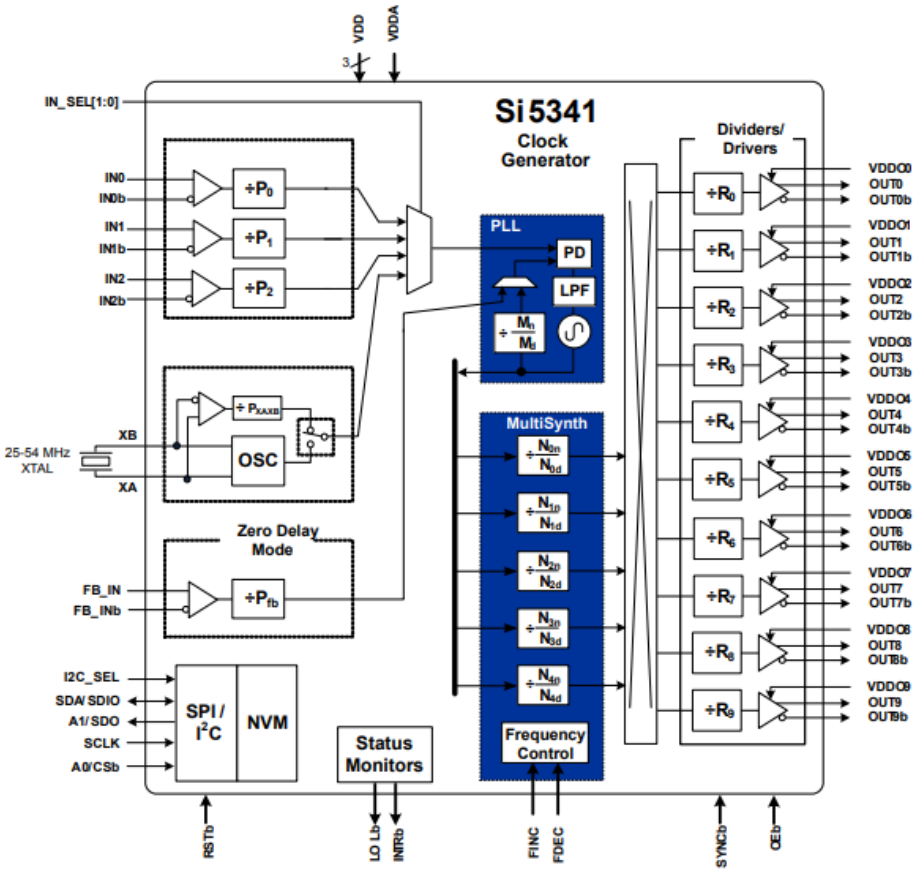


Figure 9: Si5341 Block Diagram

Source:https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/data-sheets/si5341-40-d-datasheet.pdf

ESM:

Advanced Driver-Assistance Systems (ADAS) rely heavily on security chiplets to handle sensitive data and ensure safe operation. These chiplets require robust Error Handlers (ESMs) to maintain system stability and prevent critical errors from compromising the safety of the vehicle. ADAS systems operate in highly dynamic environments, requiring the ESM to react to errors instantaneously to prevent accidents. The ESM itself must be secure to prevent malicious attacks and unauthorized access.

Benefits:

1. ESMs help to prevent critical errors that could lead to accidents.
2. ESMs can protect ADAS systems from data manipulation and other attacks
3. ESMs can help to quickly recover from errors and minimize system downtime.
4. SM logs can provide valuable information for diagnosing and resolving errors.

1. NXP S32G Vehicle Network Processors:

- Description: These processors integrate Hardware Security Modules (HSMs) with dedicated ESMs specifically designed for ADAS applications.
- Key Features: Real-time error detection and response, secure boot, secure communication protocols, tamper detection, redundancy mechanisms.
- Applications: Sensor data integrity checks, secure communication between ADAS components, secure boot of ADAS software.

Input frequency range:	
Differential clock:	10 MHz to 160 MHz
Output frequency range:	
Differential:	10 MHz to 800 MHz
Core voltage:	
VDD:	1.00V to 1.35V (nominal 1.2V)
VDDA:	3.0V to 3.6V (nominal 3.3V)
Ambient Temperature Range:	
–40 to +105 °C	

Reference Link: https://www.nxp.com/docs/en/data-sheet/S32G2.pdf

Cyclic Redundancy Check (CRC):

CRC is used to verify the integrity of sensor data received from LiDAR, cameras, and radar. This ensures that the data has not been corrupted in transit and can be used for accurate decision-making. It is also used to detect attempts to tamper with the ADAS hardware or software. This allows the system to take appropriate action, such as shutting down or alerting the driver.
We mentioned the NXP S32G Series Processors before in the ESM part. The NXP S32G274A Processor integrates a hardware CRC engine for data integrity protection. The CRC engine supports a wide range of CRC algorithms, including CRC-32, Commonly used for general data integrity verification and CRC-16, offers a more compact implementation for certain applications.
The hardware CRC engine can calculate CRC values with high performance, achieving data rates of up to 64 Gbps.

TEE security enhancement:

Trusted Execution Environments (TEEs) offer a valuable layer of security for sensitive data and operations on mobile and embedded devices. Partitioning the TEE into smaller, isolated environments can limit the attack surface and prevent vulnerabilities in one partition from impacting others. Utilizing secure enclaves within the TEE can offer additional isolation and protection for highly sensitive tasks and data.

Crypto Coprocessor

A crypto coprocessor is a dedicated hardware chip designed to accelerate cryptographic operations. It offloads the burden of encryption and decryption from the main processor, enhancing security and performance.The performance of the coprocessor should be sufficient to handle the workload of your application without introducing bottleneck. For example: NXP's S32G vehicle network processors integrate secure enclaves with dedicated crypto coprocessors for secure boot, key management, and communication authentication in ADAS systems.

WDOG

Watchdog Timer is a crucial component that plays a vital role in maintaining system stability and reliability. It is essentially a hardware timer that triggers a predefined action if it doesn't receive a regular "heartbeat" signal from the system it's monitoring. This heartbeat signal is typically sent by the main processor or another critical component within the ADAS system. If the monitored system crashes or freezes, the WDOG will not receive its expected heartbeat signal. This

triggers a reset or other recovery action, preventing the system from hanging indefinitely and potentially causing safety hazards and preventing system hang. For example we mentioned NXP's S32G vehicle network processors before. The main processor of the S32G continuously sends a "heartbeat" signal to the WDOG within the SPE.The WDOG is configured with a specific timeout period. If the WDOG does not receive the heartbeat signal within the specified timeout period, it triggers a predefined action.

UID

Unique identity (UID) is the identifier typically stored on each chip and an essential part of a Hardware Root of Trust.UIDs can be implemented in various formats, depending on the specific application and security requirements. Common formats include:

- Globally Unique Identifiers (GUIDs): 128-bit values providing a high level of uniqueness and collision resistance.
- Serial Numbers: Unique sequences of numbers assigned sequentially to components during manufacturing.
- Cryptographic Hash Values: Generated from component-specific data using a cryptographic algorithm, offering tamper-resistance and verification capabilities.

Bosch Utilizes UIDs in its ADAS platform to manage component configurations and ensure compatibility between different hardware and software versions. NVIDIA Integrates UIDs within its DRIVE platform to track and manage sensor data for accurate object detection and autonomous driving functions.

Key Derivation Function (KDF)

It is a cryptographic algorithm that derives one or more secret keys from a secret value, such as a master key, a password, or a passphrase. This process involves applying a cryptographic hash function or a block cipher to the secret value, often with additional inputs like a salt and an iteration count, to generate a secure and unpredictable key. KDF when used with UID provides a powerful combination for security in ADAS. UIDs act as unique identifiers for each ADAS component. KDF uses the component's UID as an input to derive a unique and secure key.

This key verifies the authenticity of firmware and software updates before allowing them to be loaded onto the component. This approach prevents unauthorized

modifications and ensures only legitimate software is installed, safeguarding the integrity of the ADAS system.

AES: The Advanced Encryption Standard

The Advanced Encryption Standard (AES) is a symmetric cryptographic encryption algorithm playing a vital role in securing Advanced Driver Assistance Systems (ADAS). Its strong encryption capabilities ensure the confidentiality and integrity of sensitive data within ADAS, contributing to the safety and reliability of autonomous driving technologies. AES uses the same key to encrypt and decrypt data.This means the key used in the encryption of a piece of data is also the only key that can be chosen to decrypt that data.

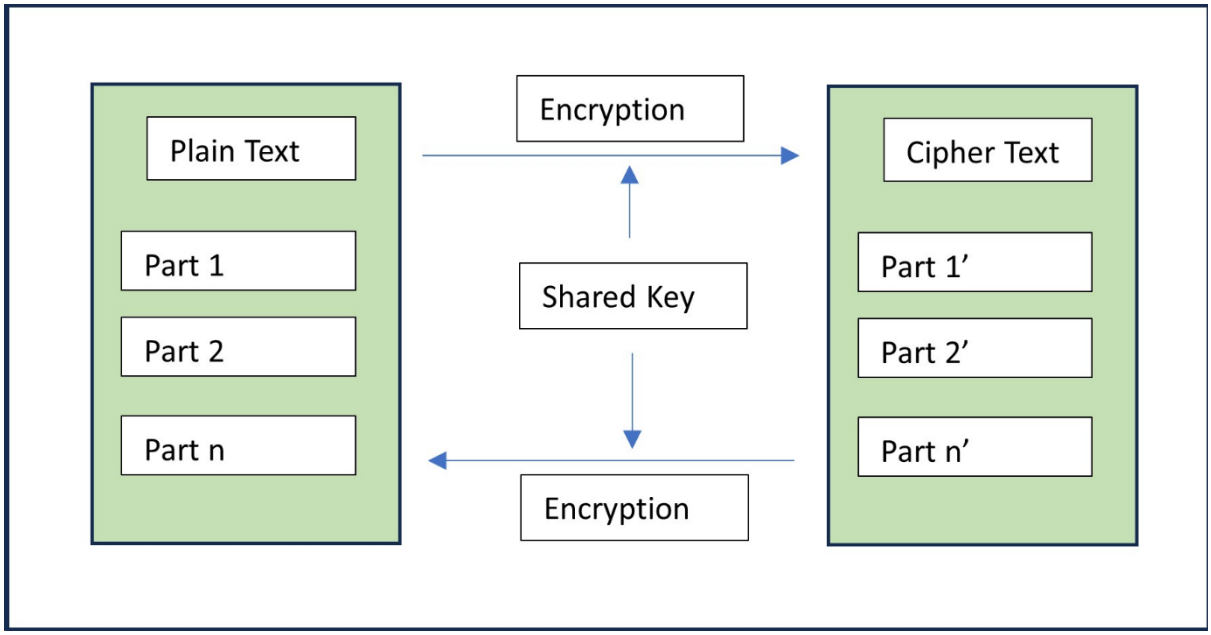


Figure 10: Proposed Security Chiplet Design

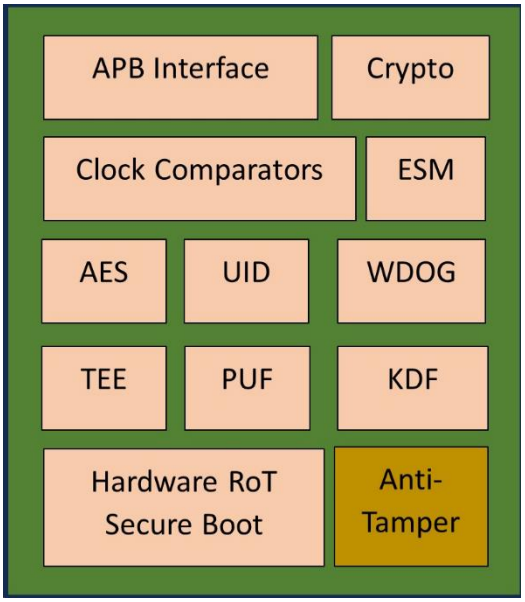


Figure 11: Block Diagram

5. A NOVEL NEAR 3D INTERCONNECT TECHNOLOGY

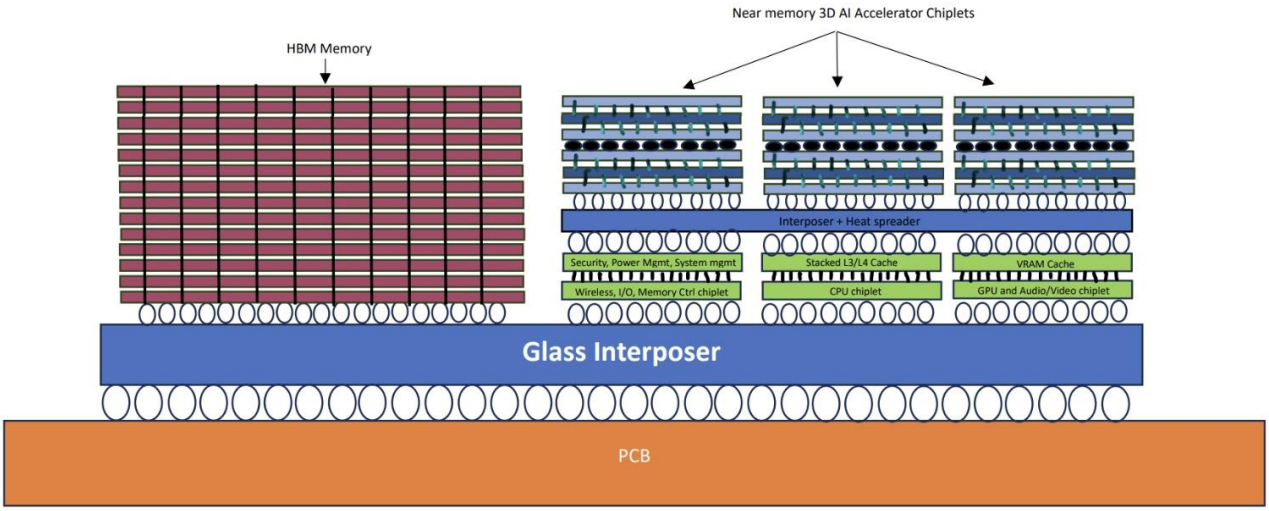


Figure 12: Novel Architecture Diagram

VRAM Cache: Video RAM cache (for efficient graphics processing), FPU: Floating point unit, Stacked L3/L4 Cache for higher system performance, AI engines (chiplets) enabled with near-memory computing features

This is a near 3D hybrid approach that combines the advantages of both 2.5D and 3D packaging.

2.5D aspects:

- Interposer: glass interposer provides a platform for mounting and interconnecting most of the chiplets like the HBM memory, near memory, Sec/Sys Mgmt chiplet, and MemCtrl, 1/0, CXL chiplet horizontally using high-density wiring channels.
- Side-by-side chiplet placement: Most of the chiplets, including the HBM memory, near memory, Sec/Sys Mgmt chiplet, and MemCtrl, 1/0, CXL chiplet, are positioned side-by-side on the interposer, another characteristic of 2.5D.

3D aspects:

- 3D AI engine chiplets: These chiplets are having very dense TGV connections, which are vertical electrical connections, enabling 3D stacking and communication within these specific chiplets.
- Stacked L3/L4 cache: The L3/L4 cache are positioned directly on top of the CPU chiplet and VRAM cache on the GPU chiplet, implementing a 3D stacking configuration for improved performance and bandwidth.

Memory:

- HBM memory: High-bandwidth memory (HBM) sits at the top of the chip and is responsible for storing data that the AI engine needs to process quickly. It offers significantly higher bandwidth than traditional DRAM, allowing for faster data transfer between memory and the AI engine. It's connected to the engine through TGV connections. Dense TGVs provide much shorter and wider data paths compared to traditional wire connections, further increasing bandwidth and reducing latency.

Processing:

- 3D-stacked AI engine chiplets: These are the brains of the operation, performing the actual computations needed for AI tasks. These AI engine chiplets are stacked together with very dense TGV connections (thickness roughly ~1 micron) that allow higher integration density and help implement near-memory computing.
- MemCtrl, I/O, CXL chiplet: This chiplet handles communication with other parts of the system, such as the CPU and external storage.

Cache:

- Stacked L cache: This cache stores frequently used data close to the AI engine for faster access.
- VRAM Cache: This cache stores data specifically for graphics processing.

Interposer, PCB and C4 bumps:

- PCB: This is the printed circuit board that holds the entire 3D-IC package. It provides power and connects the 3D-IC to other components in the system.

- Glass interposer: This is a thin glass substrate that sits between the memory and the processing engine chiplets. It provides electrical connections between them and helps to dissipate heat.
- C4 bumps: These are small solder balls that connect the chiplets to the interposer.

All die-to-die interconnections are based on Universal Chiplet Interconnect Express (UCIE).

Benefits of the hybrid approach:

- Increased integration density: By combining side-by-side placement on the interposer with 3D stacking within specific chiplets, this approach can pack more functionality into a smaller package compared to pure 2.5D.
- Improved performance: The 3D stacking of the VRAM on the GPU chiplet and L3/L4 cache on top of the CPU chiplet reduces the interconnect distance, leading to lower latency and higher bandwidth for these components.
- 3D-stacked AI engine chiplets allow higher integration density and help implement near-memory computing.
- Better thermal management: Stacking the hot GPU chiplet with the cache on top allows for more efficient heat dissipation through the interposer, also acting as a heat spreader on the top of the cache chiplets.

Heat Spreader Benefits:

- Improved heat dissipation: The large surface area of the heat spreader acts as a heat sink, effectively drawing away heat from the underlying chiplets. This is especially important for the 3D AI engines, which generate high heat due to their dense circuitry and high processing power.
- Reduced thermal hotspots: By distributing heat evenly across its surface, the heat spreader helps prevent the formation of localized hot spots that could damage the chiplets. This is critical for maintaining stable operation and long-term reliability of the package.
- Enhanced cooling efficiency: The heat spreader facilitates efficient heat transfer to the attached cooling system, such as a heatsink or fan. This allows for better overall thermal management of the entire package.

- Protection of underlying chiplets: The heat spreader acts as a physical barrier, protecting the chiplets from mechanical damage and external contaminants. This is especially important for the delicate TGV connections within the 3D AI engines.

Glass interposer offers features such as ultra high resistivity, ultra low loss, high modulus for minimum warpage, adjustable thermal expansion (CTE) among other qualities such as large panel processing as compared to small wafer for silicon interposers as can be seen below:

WHY GLASS?

Table 1: Material properties

Substrate Core	Silicon	Glass
Surface roughness(nm)	<10	<10
CTE(ppm/K)	2.9-4	3-9
Young's modulus	165	50-90
Moisture absorption	0	0
Thermal conductivity(W/m.K)	148	1.1

Table 2: Physical properties

Substrate Core	Silicon	Glass
Package size(mm)	35×35	100×100
Panel/Wafer size	300mm	710mm^2

- Surface Roughness: This refers to the unevenness of the material's surface. A smoother surface enables better connections between the chiplets and the interposer.
- CTE (Coefficient of Thermal Expansion): This is a measure of how much a material expands or contracts with changes in temperature. A material with a low CTE is important for maintaining the integrity of the 3D-IC during temperature fluctuations.

- Young's Modulus: This is a measure of a material's stiffness. A stiffer material is less likely to deform under stress, which is important for maintaining the alignment of the chiplets in a 3D-IC.
- Moisture Absorption: This is a measure of how much moisture a material can absorb. High moisture absorption can lead to corrosion and other problems.

Near memory 3D Al engine:

This refers to the close proximity of the memory to the AI engine, which enables faster data transfer and improves AI performance.

- Faster processing: Data can be accessed and processed much quicker, leading to significant performance improvements in AI tasks.
- Lower latency: Latency, the time it takes for data to be processed, is significantly reduced. This is crucial for applications requiring real-time responsiveness.
- Improved efficiency: Less data movement translates to lower power consumption, extending battery life and reducing energy costs.
- Reduced complexity: Less data movement simplifies system design and reduces the number of components needed, leading to smaller and more compact devices.
- Scalability: Near-memory architectures offer better scalability for future increases in data volume and processing complexity.

WHY TGVs?

Compared to traditional blind or buried vias in silicon interposers, TGVs offer several advantages:

1. Higher Density and Interconnect Flexibility:

- Smaller via diameter: TGVs can be drilled with significantly smaller diameters (5-10 μm) compared to silicon vias (75-150 μm), allowing more vias per unit area and increased routing density.
- 3D integration: They enable vertical interconnection between multiple layers, promoting 3D integration of chips, passives, and other components within a compact package.

2. Enhanced Electrical Performance:

- Lower signal loss: Glass exhibits lower dielectric constant compared to silicon, resulting in lower signal loss for high-frequency interconnects. This improves signal integrity and reduces power consumption.
- Better EMC performance: Glass acts as a natural EMI shield, reducing electromagnetic interference between layers and improving overall system signal integrity.
- Optical transparency: Enables visual inspection and potentially simplifies alignment and bonding processes.

3. Simplified Manufacturing and Assembly:

- Single-step fabrication: TGVs can be fabricated directly in the glass substrate during panel-level processing, eliminating the need for additional via formation steps on individual chips. This simplifies manufacturing and reduces cost.
- Direct PCB assembly: Glass interposers with TGVs can be directly bonded to PCBs without the need for intermediate organic packages, reducing package size and improving thermal management.

6. THERMAL MANAGEMENT –

The thermal management of chiplet packaging is a crucial factor. Thermal issue is not only critical to the performance and longevity of high-power devices, but also has become one of the most significant challenges for the advanced packaging architectures. Therefore, thermal analysis and management are essential at the early stage of 2.5-D CHI and 3-D stacked chip design.

It has been observed that 2.5D integration, which integrates small chiplets on a silicon interposer, is less prone to the thermal challenges observed in 3D vertical stacking which has more heating issues.

Some of the proposed techniques and cooling solutions to overcome the issue are discussed below.

A. DARK SILICON TECHNIQUE -

- The primary objective of this technique is to dynamically activate cores based on workload requirements, optimizing power consumption and heat dissipation. By selectively activating cores as needed, dark silicon facilitates a balance between performance and power efficiency.
- Running all cores concurrently becomes impracticable due to the resultant increase in temperatures. Hence, certain cores are made inactive, creating designated "dark regions" on the chip. These dark regions are strategically managed, with cores either powered down or operated at reduced frequencies to mitigate heat generation.
- This is useful when multiple cores have no functioning at most of times in order to save power and generate less heat overall when all the cores are functioning at all the times.
- However this also faces challenges including potential performance impact, dynamic workload complexity, communication overheads, programming intricacies, reduced fault tolerance, algorithmic overhead, hardware complexity, and optimization intricacies.

B. MICROFLUIDIC COOLING -

- Cooling is a key issue for 3D chiplet stacking since both the power dissipation per unit area and the thermal resistance for the dice in the stack to the heat sulk increase with the number of tiers.
- The thermal management method with microfluidics reduces the maximum temperature of 2.5D and 3D chiplet by 47.2°C and 63.83°C, respectively. (reference 4).
- Adopting an air-cooled heat sink (ACHS) to reject heat from a 3D stack is simpler to implement as shown in figure 13. However, it has limited vertical and lateral scalability, as well as limited cooling capability. An air-cooled heat sulk (and its heat spreader)

requires a large lateral footprint, which limits how close two chips (whether single-chips or a stack of chips) can be placed laterally if each has its own heat sulk. This clearly would impact interconnect length and thus energy and data rate.

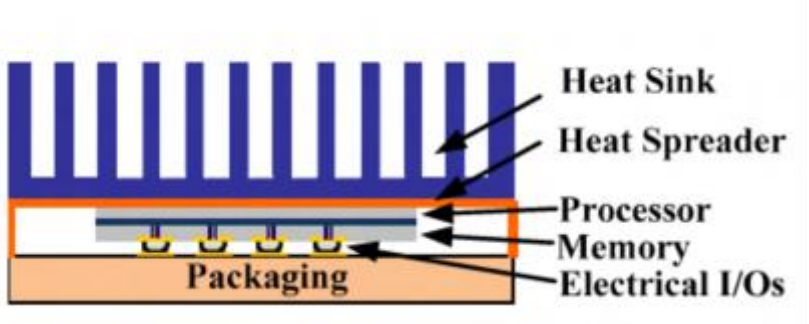


Figure 13: ACHS (reference 4)

- Due to the mentioned limitations of air-cooled heat sinks, many groups have investigated the use of integrated microfluidic heat sinks (MFHS) to reject heat. Figure 14 depicts a typical system with embedded MFHS where the fluid is supplied through a single inlet from the top of the stack.

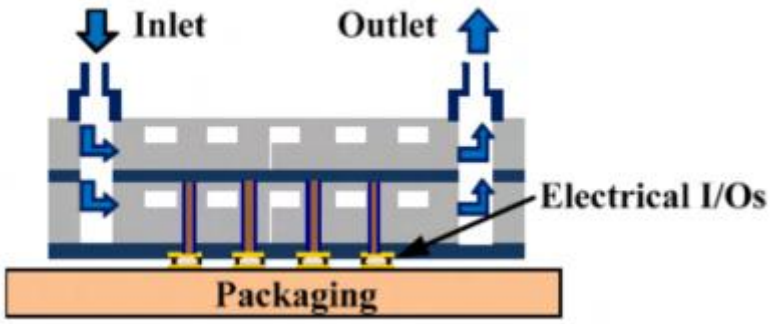


Figure 14: MFHS (reference 4)

- Another heterogeneous high-performance and high-power 3D IC system featuring a flip-chip compatible inlet/outlet system is shown in figure 15. The proposed 3D IC system features a silicon interposer with embedded fluidic delivery channels and an array of 3D stacked processor and memory tiers. The processor tiers each contain an embedded microfluidic heat sink. TSVs are routed through the integrated MFHS. The fluid is delivered from the interposer to each tier, independently through microscale fluidic I/Os formed using either solder or polymer. This approach allows on-demand cooling to each tier and helps minimize the thermal gradient across the stack when power dissipation varies in the stack.

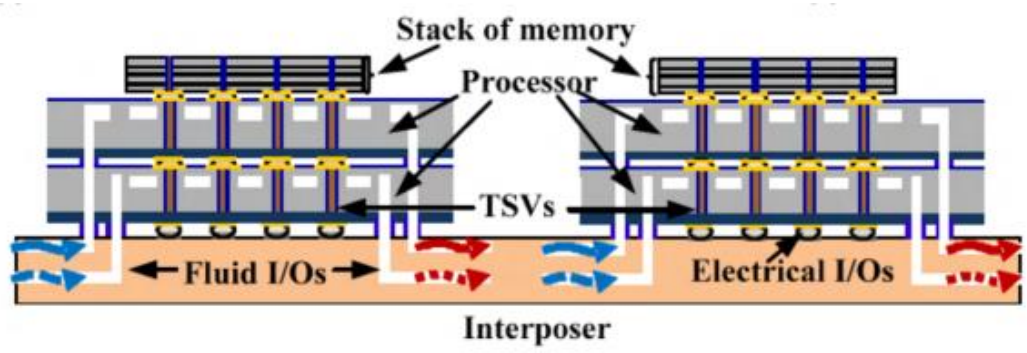


Figure 15: Integrated MFHS (reference 4)

- Experimental results (reference 1) show that a MFHS has superior heat removal capability relative to an ACHS for 3D ICs. The MFHS maintains the stack temperature below 50°C for a total power density of 200 W/CIU2 in a two-tier stack. Moreover, the thermal coupling effect is reduced when a MFHS is used. Finally, MFHS based on-demand cooling approach is shown to enable a reduction in the thermal gradient within the stack by supplying liquid at different flow rates to tiers with different power dissipation.

C. HEAT SINK, HEAT SPREADERS AND THERMAL INTERFACE MATERIALS -

- Heat sink is a passive cooling device that is used to dissipate heat generated by electronic components, such as chiplets, to prevent overheating and maintain optimal operating temperatures. The primary purpose of a heat sink is to absorb heat from the electronic component and transfer it to the surrounding environment, typically through the air.
- The heat sink with higher thermal conductivity is more efficient to conduct heat from chiplets, A greater heat transfer coefficient means that it is easier for the heat sink to remove heat to the ambient air. (reference 4)
- A typical 2.5D stacking diagram is shown below in figure 16 with Silicon interposer.

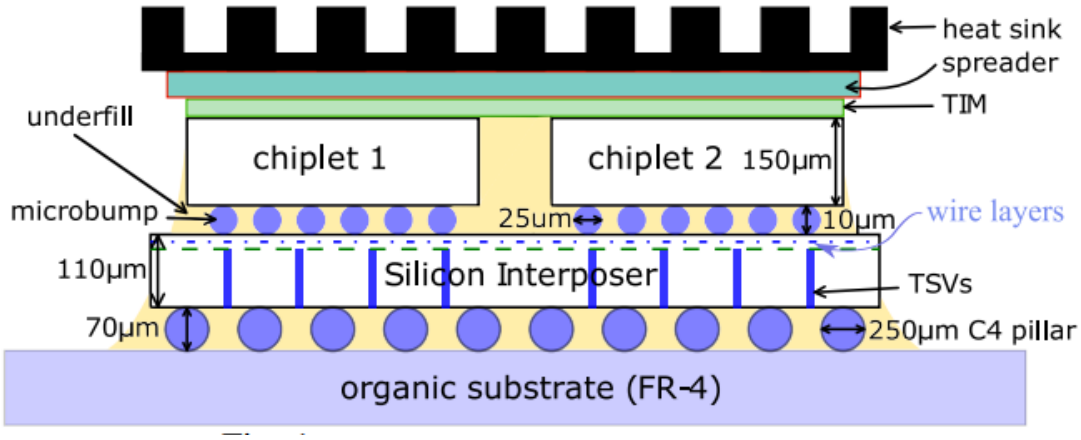


Figure 16: 2.5D with heat sink and spreader (reference 4)

- A heat spreader is basically used to provide cost effective means of cooling and is usually placed right below the heat sink, helping to transfer all of the generated heat to the sink.
- Thermally conductive materials are placed between two solid surfaces (heat generating surface e.g. microprocessor) and heat dissipating surface such as heat spreader to help improve heat transfer.
- These materials are applied as a thin layer, and typical materials are filled polymers, soldiers, PCMs, etc.

Function	Typical Material	Important Properties
Heat Spreader/Sink	Al, Cu	• Thermal conductivity • CTE • Thermal and Interface Resistances
Thermal Interface Materials	Thermal Grease, (ZnO, Ag, AlN in oil), Thermal Pads, CNT….	

- Some of the TIMs (Thermal Interface Materials) are listed in the below table - (reference 3)

TIM	Characteristic Composition	Advantages	Disadvantages
Thermal Grease	Inorganic powders in oil (AlN, ZnO..)	•High thermal conductivity •Good conformity	•Pump out and phase separation in thermal cycling

		•Less delamination •High rework ability	•Difficult thickness control
Thermal Gel	Carbon black, high conductivity metal oxide, metal powders in olefin, silicone oil.	•Easy application •Less susceptibility to pump out •Rework ability	•Curing required •Lower thermal conductivity •Low adhesion
Phase Change Material	Low melting point materials (e.g. wax, polyolefin) filled with high conducting inorganic salts (Al2O3, BN, AlN, ..), CNT, Graphene	•Curing not needed •Good surface conformity •Less susceptibility to pump out •No delamination or dry out •Reworkable •Easy handling	•Non-uniform BLT •Lower thermal conductivity than grease •Contact pressure required
PCMA	Low melting point metals and alloys (e.g. In, InAg…)	•High thermal conductivity •No curing required	•Intermetallics •Susceptibility to high temperature corrosion
Soldiers	Eutectic binary or ternary alloys	•High thermal conductivity •No curing required	•Reflow needed •Thermo-mechanical stress •Possibility of voids

D. INCREASING SPACING BETWEEN CHIPLETS -

- This is applicable to 2.5D packaging as increasing the spacing in 3D is not a viable option.
- In general (reference 4), for all 2.5D integration cases, the peak temperature decreases as chiplet spacing increases. High-power benchmarks need larger chiplet spacing to stay below the 85 degree Celsius threshold.
- So we strategically insert spacing between the chiplets to reduce the operating temperature of the overall system, thus allowing more cores to operate at a higher frequency under the same safe peak temperature threshold.
- In a 2.5D multi-chiplet system, the peak temperature of the chip increases with higher power density when the chiplet count and interposer size remain constant.
- Conversely, increasing the interposer size decreases the peak temperature due to greater spacing between chiplets, and raising the chiplet count while maintaining a consistent interposer size results in a reduction in peak temperature.
- The critical insight is that, despite efforts to insert spacing between chiplets for improved heat dissipation, hotspots may still form in regions with high power density. Consequently, the placement of chiplets needs to be carefully considered from a thermal perspective to manage power density and heat effectively.

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