Performance Engineering of a 1D Heat Transfer Simulation

1 Problem 1: Analysis of Initial Code Versions

Version	Data Layout	Observed Performance	Performance Explanation
HeatBase	2D array $U[x][t]$, non-contiguous memory access in inner loop	11.9 s runtime 48.8 cycles/stencil ~ 3.8 cache misses/stencil	Poor cache re-use : data accesses generate cache misses, which lowers IPC.
HeatBaseT	2D array $U[t][x]$, contiguous spatial access	1.04 s runtime 1.63 cycles/stencil $\sim 8 \times 10^{-4}$ cache misses/stencil	Transposing the matrix addresses the cache re-use issues of the BASE version.
Heat	Two 1D arrays with double buffering	0.33 s runtime 1.43 cycles/stencil $\sim 10^{-6}$ cache misses/stencil	One further optimization : using a buffer swap we keep the working line for one iteration to another to avoid an extra memory accesses.