## CPU Performance Analysis Report 4.2.1

Measured time	Sat Jul 9 20:47:32 2022
Node name	e31-2201c

Process no.	0
CMG no.	0
leasured region	axhelm_kernel, 1

ector length (bit)	512
PU frequency (GHz)	1.999

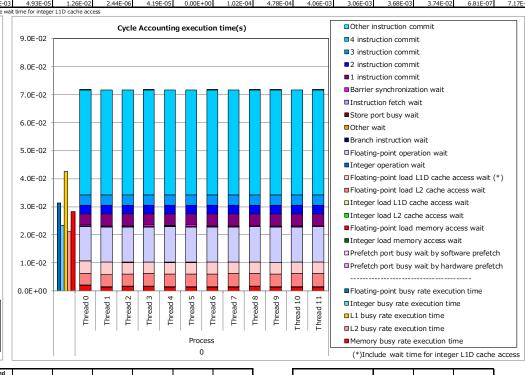
Stati	stics	Execution time (s)	GFLOPS	Floating- point operation peak ratio (%)	Memory throughput (GB/s)	Memory throughput peak ratio (%)	Effective instruction	Floating- point operation	SIMD instruction rate (%) (/Effective instruction)	SVE operation rate (%)	point pipeline Active element rate	IPC	GIPS
Process	Thread												
0	0	7.17E-02	12.23	19.11%	8.42		3.41E+08	8.77E+08	45.66%	100.00%	87.22%	2.38	4.76
0	1	7.17E-02	12.23	19.11%	8.31		3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	2	7.17E-02	12.23	19.12%	8.39		3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	3	7.17E-02	12.23	19.11%	8.26		3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	4	7.17E-02	12.23	19.11%	8.34		3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	5	7.17E-02	12.23	19.11%	8.44	39.40%	3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	6	7.17E-02	12.23	19.12%	8.58	39.40%	3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	7	7.17E-02	12.23	19.11%	8.44		3.41E+08	8.77E+08	45.67%	100.00%	87.17%	2.38	4.76
0	8	7.17E-02	12.23	19.12%	8.55		3.41E+08	8.77E+08	45.67%	100.00%	87.16%	2.38	4.76
0	9	7.17E-02	12.23	19.11%	8.48		3.41E+08	8.77E+08	45.67%	100.00%	87.16%	2.38	4.76
0	10	7.17E-02	12.23	19.12%	8.26		3.41E+08	8.77E+08	45.67%	100.00%	87.16%	2.38	4.76
0	11	7.17E-02	12.23	19.12%	8.39		3.41E+08	8.77E+08	45.67%	100.00%	87.25%	2.38	4.76
	CMG 0 total	7.17E-02	146.74	19.12%	100.87	39.40%	4.10E+09	1.05E+10	45.67%	100.00%	87.18%	2.38	57.15

		Prefetch po	ort busy wait			ry access wait	& Cache acces	s wait		Operati	on wait	Other	r wait						Other instruc	tion commit		
Cycle Ac	counting	Prefetch port busy wait by hardware prefetch	Prefetch port busy wait by software prefetch	Integer load memory access wait	Floating- point load memory access wait	Integer load L2 cache access wait	L1D cache	Floating- point load L2 cache access wait	point load L1D cache access wait	Integer operation wait	Floating- point operation wait	Branch instruction wait	Other wait	Store port busy wait	Instruction fetch wait	Barrier synchronizati on wait	1 instruction commit	2 instruction commit	3 instruction commit	4 instruction commit	Other instruction commit	Total
Process	Thread																					
0	0	2.25E-08	5.81E-08	8.37E-05	1.75E-03	4.70E-05	1.34E-04	4.22E-03	4.38E-03	5.68E-05	1.23E-02	2.55E-06	3.07E-05	0.00E+00	3.54E-05	4.30E-04	3.99E-03	3.07E-03	3.63E-03	3.75E-02	5.45E-06	7.17E-02
0	1	1.05E-08	4.46E-08	7.37E-05	1.24E-03	5.59E-05	1.75E-04	4.33E-03	4.31E-03	0.00E+00	1.26E-02	2.53E-06	3.97E-05	0.00E+00	9.13E-05	5.75E-04	4.06E-03	3.07E-03	3.67E-03	3.74E-02	0.00E+00	7.17E-02
0	2	1.19E-07	8.71E-08	8.30E-05	1.29E-03	5.84E-05	1.59E-04	4.46E-03	4.09E-03	6.99E-05	1.26E-02	2.40E-06	4.26E-05	0.00E+00	1.02E-04	5.09E-04	4.06E-03	3.07E-03	3.69E-03	3.74E-02	0.00E+00	7.17E-02
0	3	1.25E-08	4.11E-08	8.70E-05	1.30E-03	5.72E-05	1.52E-04	4.51E-03	4.09E-03	6.75E-05	1.25E-02	2.49E-06	4.05E-05	0.00E+00	9.47E-05	5.33E-04	4.04E-03	3.04E-03	3.66E-03	3.75E-02	1.22E-06	7.17E-02
0	4	1.35E-08	2.80E-08	7.89E-05	1.25E-03	5.79E-05	1.68E-04	4.49E-03	4.12E-03	6.46E-05	1.26E-02	2.27E-06	5.48E-05	0.00E+00	1.99E-04	2.92E-04	4.12E-03	3.07E-03	3.69E-03	3.74E-02	0.00E+00	7.17E-02
0	5	5.31E-08	9.46E-08	7.52E-05	1.29E-03	5.86E-05	1.46E-04	4.50E-03	4.03E-03	7.28E-05	1.26E-02	2.40E-06	4.00E-05	0.00E+00	9.10E-05	6.12E-04	4.05E-03	3.05E-03	3.67E-03	3.74E-02	0.00E+00	7.17E-02
0	6	2.85E-08	6.51E-08	8.70E-05	1.23E-03	6.12E-05	1.67E-04	4.45E-03	4.22E-03	0.00E+00	1.26E-02	2.50E-06	4.09E-05	0.00E+00	8.27E-05	5.00E-04	4.06E-03	3.04E-03	3.67E-03	3.74E-02	9.17E-07	7.17E-02
0	7	9.52E-09	3.61E-08	7.55E-05	1.28E-03	5.92E-05	1.50E-04	4.59E-03	4.08E-03	6.77E-05	1.25E-02	2.33E-06	3.90E-05	0.00E+00	8.60E-05	4.91E-04	4.06E-03	3.09E-03	3.71E-03	3.74E-02	0.00E+00	7.17E-02
0	8	0.00E+00	4.35E-08	9.28E-05	1.29E-03	5.93E-05	1.58E-04	4.58E-03	4.11E-03	5.88E-05	1.25E-02	2.51E-06	3.78E-05	0.00E+00	7.68E-05	4.68E-04	4.06E-03	3.05E-03	3.68E-03	3.74E-02	1.90E-08	7.17E-02
0	9	1.85E-08	3.35E-08	8.16E-05	1.21E-03	5.94E-05	1.75E-04	4.45E-03	4.11E-03	6.08E-05	1.26E-02	2.47E-06	5.60E-05	0.00E+00	1.89E-04	3.68E-04	4.14E-03	3.04E-03	3.68E-03	3.74E-02	4.32E-07	7.17E-02
0	10	2.65E-08	4.75E-08	8.44E-05	1.27E-03	5.92E-05	1.50E-04	4.58E-03	4.07E-03	7.22E-05	1.25E-02	2.28E-06	4.07E-05	0.00E+00	8.54E-05	5.07E-04	4.05E-03	3.03E-03	3.68E-03	3.74E-02	0.00E+00	7.17E-02
0	11	2.65E-08	7.36E-08	8.45E-05	1.26E-03	5.95E-05	1.65E-04	4.52E-03	4.17E-03	0.00E+00	1.26E-02	2.55E-06	3.97E-05	0.00E+00	9.01E-05	4.49E-04	4.06E-03	3.05E-03	3.68E-03	3.74E-02	1.33E-07	7.17E-02
	CMG 0 total	2.84F-08	5.44F-08	8.23F-05	1.31E-03	5.77F-05	1.58F-04	4.47F-03	4.15F-03	4.93F-05	1.26F-02	2.44F-06	4.19F-05	0.00E+00	1.02E-04	4.78F-04	4.06F-03	3.06E-03	3.68F-03	3.74F-02	6.81E-07	7.17F-02

Ві	ısy	point operation pipeline A busy rate (%)	point operation pipeline B busy rate (%)	Integer operation pipeline A busy rate (%)	Integer operation pipeline B busy rate (%)	L1 busy rate (%)	L2 busy rate (%)	Memory busy rate (%)	Address calculation operation pipeline A busy rate	Address calculation operation pipeline B busy rate		pipeline B Active element rate	L1 pipeline 0 Active element rate (%)	L1 pipeline 1 Active element rate (%)	SFI(Store Fetch Interlock) rate
Process	Thread								(%)	(%)	(%)	(%)			
0	0	57.61%	29.91%	25.70%	39.43%	59.49%			53.42%	53.52%	80.55%	100.00%	100.00%	100.00%	
0	1	57.53%	29.83%	25.98%	39.70%	59.25%			53.68%	53.76%	80.50%	100.00%	100.00%	100.00%	0.05
0	2	57.57%	29.83%	25.83%	39.56%	59.29%	]		53.48%	53.61%	80.51%	100.00%	100.00%	100.00%	0.05
0	3	57.54%	29.83%	25.94%	39.70%	59.27%			53.65%	53.75%	80.50%	100.00%	100.00%	100.00%	0.05
0	4	57.52%	29.88%	25.89%	39.51%	59.29%			53.47%	53.61%	80.49%	100.00%	100.00%	100.00%	0.05
0	5	57.53%	29.83%	25.87%	39.56%	59.26%	29.59%	39.40%	53.49%	53.61%	80.50%	100.00%	100.00%	100.00%	0.05
0	6	57.50%	29.84%	25.86%	39.48%	59.25%	29.59%	39.40%	53.48%	53.52%	80.49%	100.00%	100.00%	100.00%	0.05
0	7	57.52%	29.83%	25.86%	39.50%	59.26%			53.49%	53.56%	80.50%	100.00%	100.00%	100.00%	0.05
0	8	57.94%	30.05%	25.85%	39.48%	59.69%			53.46%	53.55%	80.50%	100.00%	100.00%	100.00%	0.05
0	9	57.52%	29.83%	25.87%	39.52%	59.27%	1		53.46%	53.56%	80.49%	100.00%	100.00%	100.00%	0.05
0	10	57.54%	29.82%	25.85%	39.52%	59.27%	1		53.46%	53.55%	80.50%	100.00%	100.00%	100.00%	0.05
0	11	57.68%	29.91%	25.97%	39.61%	59.41%			53.63%	53.78%	80.59%	100.00%	100.00%	100.00%	0.05
	CMG 0 total	57.58%	29.87%	25.87%	39.55%	59.33%	29.59%	39.40%	53.51%	53.62%	80.51%	100.00%	100.00%	100.00%	0.05

											0.0.00				
	CMG 0 total	57.58%	29.87%	25.87%	39.55%	59.33%	29.59%	39.40%	53.51%	53.62%	80.51%	100.00%	100.00%	100.00%	0.05
			1			1		1		I		1	I	I	
Cac	che	L1I miss rate (/Effective instruction)	Load-store instruction	L1D miss	L1D miss rate (/Load- store instruction)	L1D miss demand rate (%) (/L1D miss)	L1D miss hardware prefetch rate (%) (/L1D miss)	L1D miss software prefetch rate (%) (/L1D miss)	L2 miss	L2 miss rate (/Load-store instruction)	L2 miss demand rate (%) (/L2 miss)	L2 miss hardware prefetch rate (%) (/L2 miss)	L2 miss software prefetch rate (%) (/L2 miss)	L1D TLB miss rate (/Load- store instruction)	L2D TLB miss rate (/Load- store instruction)
Process	Thread														
0	0	0.00	1.16E+08	2.14E+06	0.02	2.04%	1.30%	96.65%	2.10E+06	0.02	8.87%	0.70%	90.43%	0.00000	0.00000
0	1	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.86%	2.10E+06	0.02	8.73%	0.62%	90.65%	0.00000	0.00000
0	2	0.00	1.16E+08	2.14E+06	0.02	3.12%	0.03%	96.84%	2.10E+06	0.02	8.73%	0.65%	90.62%	0.00000	0.00000
0	3	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.03%	96.84%	2.10E+06	0.02	8.72%	0.63%	90.65%	0.00000	0.00000
0	4	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.86%	2.10E+06	0.02	8.73%	0.64%	90.63%	0.00000	0.00000
0	5	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.77%	0.57%	90.66%	0.00000	0.00000
0	6	0.00	1.16E+08	2.14E+06	0.02	3.14%	0.00%	96.86%	2.10E+06	0.02	8.75%	0.60%	90.65%	0.00000	0.00000
0	7	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.74%	0.63%	90.64%	0.00000	0.00000
0	8	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.74%	0.61%	90.65%	0.00000	0.00000
0	9	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.75%	0.60%	90.66%	0.00000	0.00000
0	10	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.75%	0.58%	90.67%	0.00000	0.00000
0	11	0.00	1.16E+08	2.14E+06	0.02	3.13%	0.00%	96.87%	2.10E+06	0.02	8.72%	0.64%	90.64%	0.00000	0.00000
	CMG 0 total	0.00	1.39E+09	2.57E+07	0.02	3.04%	0.12%	96.85%	2,52E+07	0.02	8.75%	0.62%	90.63%	0.00000	0.00000

Statistics	Cache L1D,L2 miss rate	
	(/Load-store instruction)	9.0E-02
100%	1.00	8.0E-02
90%	0.90	
80%	0.80	7.0E-02
70%	0.70	6.0E-02
60%	0.60	5.0E-02
50%	0.50	4.0E-02
40%	0.40	3.0E-02
30%	0.30	3.01-02
20%	0.20	2.0E-02
10%	0.10	1.0E-02
0%	0.00	
CMG	L1D miss L2 miss	0.0E+00
SIMD instruction ratio	■software prefetch rate(L1D,L2 miss)	Thread 0
(/Effective instruction)  Floating-point operation peak ratio	□ hardware prefetch rate(L1D,L2 miss)	
■Memory throughput peak ratio	demand rate(L1D,L2 miss)	



								Load-store	instruction							Pr	efetch instructi	ion		Floati	ng-point instru	ıction	Floating-poin	t move and						
					Load in	struction						Store inst	truction						1				conversion i	instruction						I
					SIMD				Non-SIMD			SIMD			Non-SIMD					Floating-										I
Instruction Process Three		ingle vector contiguous load instruction	vector contiguous structure load	Non- contiguous gather load instruction	Broadcast load instruction	Floating- point register fill instruction	Predicate register fill instruction	First-fault load instruction	Non-SIMD load instruction	Single vector contiguous store instruction	vector contiguous structure store	Non- contiguous scatter store instruction	Floating- point register spill instruction	Predicate register spill instruction	Non-SIMD store instruction	Contiguous prefetch instruction	Gathering prefetch instruction	Scalar prefetch instruction	DCZVA instruction	point instruction except FMA and reciprocal	FMA instruction	Floating- point reciprocal instruction	conversion	Floating- point move instruction	Integer instruction	Branch instruction	Predicate instruction	Crypto- graphic instruction	Other instruction	Total
0	0	3.99F+07	0.00F+00	0.00F+00	0.00F+00	1.28F+06	1.70F+01	0.00F+00	5.86F+07	5.12F+06	0.00F+00	0.00F+00	1.60F+03	0.00F+00	1.08F+07	0.00F+00	0.00F+00	1.40F+07	8.00F+00	1.13F+07	4.92F+07	0.00F+00	0.00F+00	4.92F+07	0.00F+00	9.45F+05	1.01F+02	0.00F+00	1.01F+08	3.41E+0
0	1	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4,92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	2	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	
0	3	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	4	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	5	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	6	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	7	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	8	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	9	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	10	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
0	11	3.99E+07	0.00E+00	0.00E+00	0.00E+00	1.28E+06	1.70E+01	0.00E+00	5.86E+07	5.12E+06	0.00E+00	0.00E+00	1.60E+03	0.00E+00	1.08E+07	0.00E+00	0.00E+00	1.40E+07	8.00E+00	1.13E+07	4.92E+07	0.00E+00	0.00E+00	4.92E+07	0.00E+00	9.41E+05	1.01E+02	0.00E+00	1.01E+08	3.41E+0
CMG 0	total	4.79E+08	0.00E+00	0.00E+00	0.00E+00	1.54E+07	2.04E+02	0.00E+00		6.14E+07	0.00E+00	0.00E+00	1.92E+04	0.00E+00	1.30E+08	0.00E+00	0.00E+00	1.67E+08	9.60E+01	1.35E+08	5.90E+08	0.00E+00	0.00E+00	5.90E+08	0.00E+00	1.13E+07	1.21E+03	0.00E+00	1.21E+09	4.10E+0
Cirio	Cocal							1.39	E+09								1.67E+08		9.60E+01		7.25E+08		5.90E	+08	0.00E+00	1.13E+07	1.21E+03	0.00E+00	1.21E+09	4.10E+0

Power Con (V		Power consumption used by core	Power consumption used by L2 cache	Power consumption used by memory
Process	Thread			
0	0	2.24E+00		
0	1	2.24E+00		
0	2	2.24E+00		
0	3	2.24E+00		
0	4	2.23E+00		
0	5	2.24E+00	2.32E+00	7.95F+00
0	6	2.24E+00	2.32L+00	7.55L+00
0	7	2.24E+00		
0	8	2.24E+00		
0	9	2.24E+00		
0	10	2.24E+00		
0	11	2.24E+00		
	CMG 0 total	2.69E+01	2.32E+00	7.95E+00

Hardware	Prefetch		L1			L2		L1/L2
Rate (/Hard Prefe	dware etch)	Stream mode prefetch rate	Injection mode allocate prefetch rate	Injection mode unallocate prefetch rate	Stream mode prefetch rate	Injection mode allocate prefetch rate	Injection mode unallocate prefetch rate	Other hardware prefetch
Process	Thread							
0	0	0.28%	0.00%	0.00%	0.07%	0.00%	0.00%	99.65%
0	1	0.33%	0.00%	0.00%	0.11%	0.00%	0.00%	99.55%
0	2	0.32%	0.00%	0.00%	0.08%	0.00%	0.00%	99.59%
0	3	0.33%	0.00%	0.00%	0.08%	0.00%	0.00%	99.59%
0	4	0.29%	0.00%	0.00%	0.08%	0.00%	0.00%	99.63%
0	5	0.33%	0.00%	0.00%	0.08%	0.00%	0.00%	99.59%
0	6	0.32%	0.00%	0.00%	0.08%	0.00%	0.00%	99.60%
0	7	0.31%	0.00%	0.00%	0.08%	0.00%	0.00%	99.60%
0	8	0.33%	0.00%	0.00%	0.08%	0.00%	0.00%	99.59%
0	9	0.31%	0.00%	0.00%	0.11%	0.00%	0.00%	99.57%
0	10	0.34%	0.00%	0.00%	0.08%	0.00%	0.00%	99.59%
0	11	0.34%	0.00%	0.00%	0.09%	0.00%	0.00%	99.57%
	CMG 0 total	0.32%	0.00%	0.00%	0.09%	0.00%	0.00%	99.60%

FLO	PS	Double precision floating- point operation	Single precision floating- point operation	Half precision floating- point operation	GFLOPS by Active element rate
Process	Thread				
0	0	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	1	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	2	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	3	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	4	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	5	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	6	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	7	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	8	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	9	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	10	8.77.E+08	0.00.E+00	0.00.E+00	10.66
0	11	8.77.E+08	0.00.E+00	0.00.E+00	10.67
	CMG 0 total	1.05.E+10	0.00.E+00	0.00.E+00	127.92

Extra  Process Thread		Gather instruction rate (%)			Instruction					l	
		0 flow rate (%)	1 flow rate (%)	2 flows rate (%)	Micro- operation instruction	Element manipulated instruction	Register manipulated instruction	MOVPRFX instruction	Math functional instruction	Micro decompositio n instruction rate (%)	Branch prediction miss rate (%)
0	0	0.00%	0.00%	0.00%	3,44E+08	4.92E+07	6.41E+03	1.92E+06	0.00E+00	100.00%	0.1
0	1	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	3.0
0	2	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.:
0	3	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.
0	4	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.0
0	5	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.:
0	6	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.8
0	7	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	1.
0	8	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.8
0	9	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.
0	10	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.
0	11	0.00%	0.00%	0.00%	3.44E+08	4.92E+07	1.00E+00	1.92E+06	0.00E+00	100.00%	0.
CMG 0 total		0.00%	0.00%	0.00%	4.13E+09	5.90E+08	6.42E+03	2.30E+07	0.00E+00	100.00%	0.5
			0.00%		4.13E+09	5.90	E+08	2.30E+07	0.00E+00	100.00%	0.5

(W)	Power Cons	umption
4.0E+01 T		
3.5E+01		
3.0E+01		used by memory
2.5E+01		used by L2 cache
2.0E+01	_	■used by core
1.5E+01		
1.0E+01		
5.0E+00	_	
0.0E+00	1 CMG	

		Destination (GB/s)						
Data Tran	sfer CMGs	Own memory	Other	Tofu	PCI			
		Own memory	memory	1014	PCI			
CMG 0 total	read	8.99E+01	7.20E-03	0.00E+00	0.00			
CMG 0 total	write	1.10E+01	4.86E-03	0.00E+00	0.00			