CPU Performance Analysis Report 4.2.1

Measured time	Sat Jul 9 20:08:57 2022
Node name	i31-4201c

Process no.	0
CMG no.	0
Measured region	axhelm_kernel, 1

Vector length (bit)
CPU frequency (GHz)

Statistics		Execution time (s)	GFLOPS	Floating-point operation peak ratio (%)	Memory throughput (GB/s)	Memory throughput peak ratio (%)	Effective instruction	Floating-point operation	SIMD instruction rate (%) (/Effective instruction)	SVE operation rate (%)	Floating-point pipeline Active element rate (%)	IPC	GIPS
Process	Thread												
0	0	3.13E-01	5.48	8.56%	2.14	9.75%	6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	1	3.13E-01	5.48	8.56%	2.10		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	2	3.13E-01	5.48	8.56%	2.07		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	3	3.13E-01	5.48	8.56%	2.07		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	4	3.13E-01	5.48	8.56%	2.08		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	5	3.13E-01	5.48	8.56%	2.05		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	6	3.13E-01	5.48	8.56%	2.09		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	7	3.13E-01	5.48	8.56%	2.08		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	8	3.13E-01	5.48	8.56%	2.09		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	9	3.13E-01	5.48	8.56%	2.09		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	10	3.13E-01	5.48	8.56%	2.04		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
0	11	3.13E-01	5.48	8.56%	2.06		6.64E+08	1.71E+09	57.06%	91.87%	92.29%	1.06	2.13
CMG 0 total		3.13E-01	65.71	8.56%	24.95	9.75%	7.97E+09	2.05E+10	57.06%	91.87%	92.29%	1.06	25.50

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Busy		Floating-point operation pipeline A busy rate (%)	Floating-point operation pipeline B busy rate (%)	Integer operation pipeline A busy rate (%)	Integer operation pipeline B busy rate (%)	L1 busy rate (%)	L2 busy rate (%)	Memory busy rate (%)	Address calculation operation pipeline A busy rate (%)	Address calculation operation pipeline B busy rate (%)	Floating-point pipeline A Active element rate (%)	Floating-point pipeline B Active element rate (%)	L1 pipeline 0 Active element rate (%)	L1 pipeline 1 Active element rate (%)	SFI(Store Fetch Interlock) rate
Process	Thread														
0	0	44.42%	35.85%	3.08%	7.48%	30.73%	8.25%	9.75%	20.51%	22.85%	86.07%	100.00%	100.00%	100.00%	0.01
0	1	44.64%	35.64%	3.23%	7.62%	29.87%			20.38%	22.67%	86.13%	100.00%	100.00%	100.00%	0.01
0	2	44.65%	35.64%	3.25%	7.61%	29.87%			20.37%	22.68%	86.13%	100.00%	100.00%	100.00%	0.01
0	3	44.66%	35.62%	3.22%	7.63%	29.86%			20.37%	22.68%	86.14%	100.00%	100.00%	100.00%	0.01
0	4	44.64%	35.63%	3.24%	7.61%	29.87%			20.36%	22.69%	86.13%	100.00%	100.00%	100.00%	0.01
0	5	44.65%	35.62%	3.23%	7.62%	29.87%			20.37%	22.68%	86.13%	100.00%	100.00%	100.00%	0.01
0	6	44.65%	35.63%	3.25%	7.58%	29.87%			20.39%	22.69%	86.13%	100.00%	100.00%	100.00%	0.01
0	7	44.65%	35.63%	3.23%	7.61%	29.87%			20.37%	22.69%	86.13%	100.00%	100.00%	100.00%	0.01
0	8	44.64%	35.64%	3.22%	7.62%	29.87%			20.38%	22.69%	86.13%	100.00%	100.00%	100.00%	0.01
0	9	44.67%	35.62%	3.23%	7.61%	29.87%			20.39%	22.68%	86.14%	100.00%	100.00%	100.00%	0.01
0	10	44.65%	35.63%	3.24%	7.60%	29.87%			20.39%	22.69%	86.13%	100.00%	100.00%	100.00%	0.01
0	11	44.62%	35.65%	3.23%	7.61%	29.87%			20.38%	22.68%	86.13%	100.00%	100.00%	100.00%	0.01
CMG 0 total		44.63%	35.65%	3.22%	7.60%	29.94%	8.25%	9.75%	20.39%	22.70%	86.13%	100.00%	100.00%	100.00%	0.01

Cache	L1I miss rate (/Effective instruction)	Load-store instruction	L1D miss	L1D miss rate (/Load-store instruction)	L1D miss demand rate (%) (/L1D miss)	L1D miss hardware prefetch rate (%) (/L1D miss)	L1D miss software prefetch rate (%) (/L1D miss)	L2 miss	L2 miss rate (/Load-store instruction)	L2 miss demand rate (%) (/L2 miss)	L2 miss hardware prefetch rate (%) (/L2 miss)	L2 miss software prefetch rate (%) (/L2 miss)	L1D TLB miss rate (/Load-store instruction)	L2D TLB miss rate (/Load-store instruction)

Process	Thread														
0	0	0.00	1.35E+08	2.28E+06	0.02	25.85%	73.49%	0.66%	2.28E+06	0.02	15.84%	89.80%	0.00%	0.00000	0.00000
0	1	0.00	1.35E+08	2.33E+06	0.02	26.59%	72.70%	0.71%	2.30E+06	0.02	14.88%	90.43%	0.00%	0.00000	0.00000
0	2	0.00	1.35E+08	2.33E+06	0.02	26.57%	72.67%	0.76%	2.30E+06	0.02	15.07%	90.48%	0.00%	0.00000	0.00000
0	3	0.00	1.35E+08	2.31E+06	0.02	26.44%	72.81%	0.75%	2.28E+06	0.02	14.83%	90.49%	0.00%	0.00000	0.00000
0	4	0.00	1.35E+08	2.33E+06	0.02	26.56%	72.71%	0.73%	2.29E+06	0.02	14.90%	90.52%	0.00%	0.00000	0.00000
0	5	0.00	1.35E+08	2.33E+06	0.02	26.53%	72.76%	0.71%	2.30E+06	0.02	14.61%	90.61%	0.00%	0.00000	0.00000
0	6	0.00	1.35E+08	2.31E+06	0.02	26.43%	72.80%	0.77%	2.28E+06	0.02	14.67%	90.57%	0.00%	0.00000	0.00000
0	7	0.00	1.35E+08	2.31E+06	0.02	26.45%	72.87%	0.68%	2.27E+06	0.02	14.70%	90.48%	0.00%	0.00000	0.00000
0	8	0.00	1.35E+08	2.31E+06	0.02	26.49%	72.80%	0.71%	2.27E+06	0.02	14.84%	90.47%	0.00%	0.00000	0.00000
0	9	0.00	1.35E+08	2.32E+06	0.02	26.49%	72.77%	0.75%	2.28E+06	0.02	14.46%	90.48%	0.00%	0.00000	0.00000
0	10	0.00	1.35E+08	2.31E+06	0.02	26.41%	72.90%	0.69%	2.27E+06	0.02	14.66%	90.61%	0.00%	0.00000	0.00000
0	11	0.00	1.35E+08	2.32E+06	0.02	26.52%	72.78%	0.70%	2.28E+06	0.02	14.48%	90.53%	0.00%	0.00000	0.00000
CMG 0 total		0.00	1.62E+09	2.78E+07	0.02	26.44%	72.84%	0.72%	2.74E+07	0.02	14.83%	90.46%	0.00%	0.00000	0.00000

Instruction		Load-store instruction													
		Load instruction								Store instruction					
		SIMD							Non-SIMD	SIMD					Non-SIMD
Process	Thread	Single vector contiguous load instruction	Multiple vector contiguous structure load instruction	Non-contiguous gather load instruction	Broadcast load instruction	Floating-point register fill instruction	Predicate register fill instruction	First-fault load instruction	Non-SIMD load instruction	Single vector contiguous store instruction	Multiple vector contiguous structure store instruction	Non-contiguous scatter store instruction	Floating-point register spill instruction	Predicate register spill instruction	Non-SIMD store instruction
0	0	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.06E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	1	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	2	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	3	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	4	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	5	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	6	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	7	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	8	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	9	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	10	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
0	11	4.22E+06	0.00E+00	2.79E+07	0.00E+00	1.02E+06	1.70E+01	0.00E+00	6.05E+07	1.02E+06	0.00E+00	0.00E+00	8.00E+02	0.00E+00	4.05E+07
CMG 0 total		5.07E+07	0.00E+00	3.35E+08	0.00E+00	1.23E+07	2.04E+02	0.00E+00	7.27E+08	1.23E+07	0.00E+00	0.00E+00	9.60E+03	0.00E+00	4.86E+08
		1.62E+09													

Hardware Prefetch Rate (%) (/Hardware Prefetch)		L1			L2			L1/L2
		Stream mode prefetch rate	Injection mode allocate prefetch rate	Injection mode unallocate prefetch rate	Stream mode prefetch rate	Injection mode allocate prefetch rate	Injection mode unallocate prefetch rate	Other hardware prefetch
Process	Thread							
0	0	38.38%	0.00%	0.00%	53.07%	0.00%	0.00%	8.54%
0	1	37.93%	0.00%	0.00%	53.41%	0.00%	0.00%	8.65%
0	2	38.34%	0.00%	0.00%	53.00%	0.00%	0.00%	8.66%
0	3	38.06%	0.00%	0.00%	53.28%	0.00%	0.00%	8.66%
0	4	38.77%	0.00%	0.00%	52.42%	0.00%	0.00%	8.81%
0	5	38.28%	0.00%	0.00%	53.03%	0.00%	0.00%	8.69%
0	6	38.81%	0.00%	0.00%	52.33%	0.00%	0.00%	8.87%
0	7	38.44%	0.00%	0.00%	52.82%	0.00%	0.00%	8.75%

FLOPS		Double precision floating-point operation	Single precision floating-point operation	Half precision floating-point operation	GFLOPS by Active element rate
Process	Thread				
0	0	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	1	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	2	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	3	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	4	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	5	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	6	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	7	1.71.E+09	0.00.E+00	0.00.E+00	5.05

0	8	38.42%	0.00%	0.00%	52.85%	0.00%	0.00%	8.73%
0	9	38.27%	0.00%	0.00%	52.99%	0.00%	0.00%	8.74%
0	10	38.66%	0.00%	0.00%	52.54%	0.00%	0.00%	8.80%
0	11	39.50%	0.00%	0.00%	51.50%	0.00%	0.00%	9.00%
CMG 0 total		38.49%	0.00%	0.00%	52.77%	0.00%	0.00%	8.74%

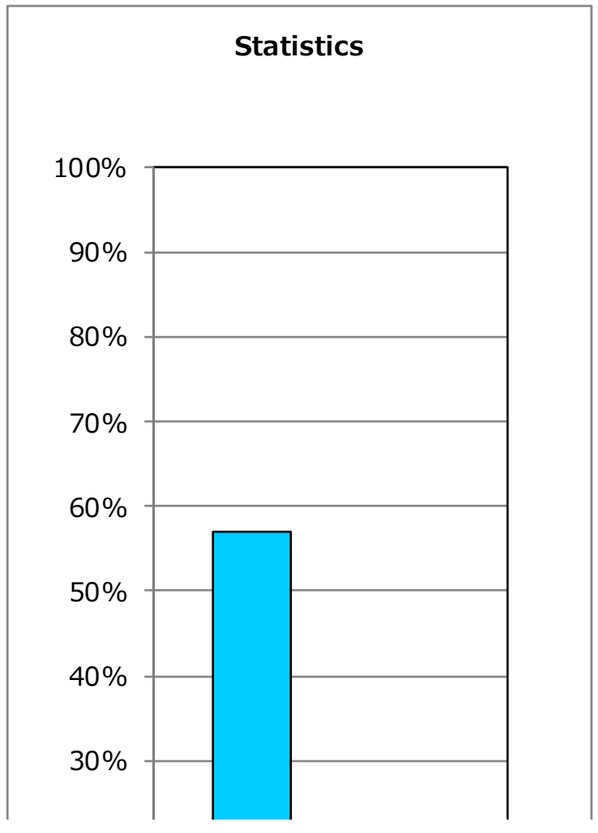
0	8	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	9	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	10	1.71.E+09	0.00.E+00	0.00.E+00	5.05
0	11	1.71.E+09	0.00.E+00	0.00.E+00	5.05
CMG 0 total		2.05.E+10	0.00.E+00	0.00.E+00	60.65

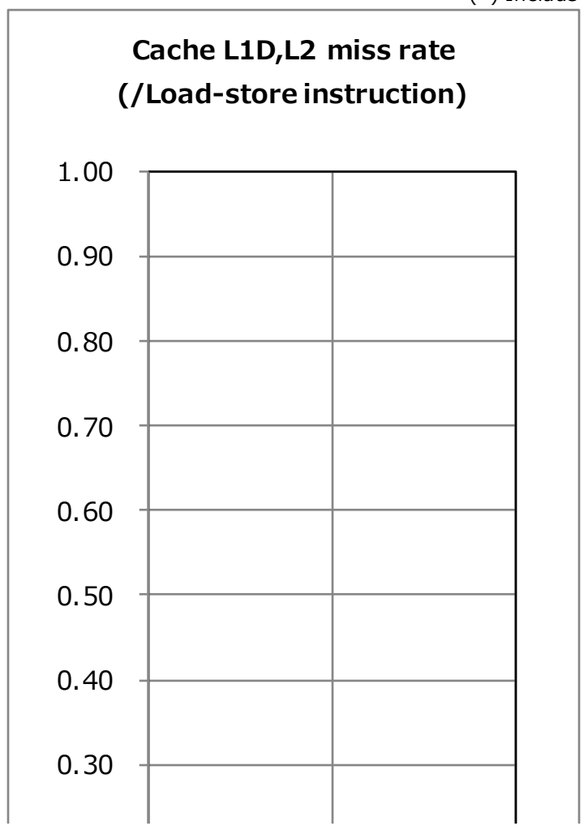
Data Transfer CMGs		Destination (GB/s)			
		Own memory	Other memory	Tofu	PCI
CMG 0 total	read	2.24E+01	4.84E-03	0.00E+00	0.00E+00
	write	2.52E+00	4.35E-03	0.00E+00	0.00E+00

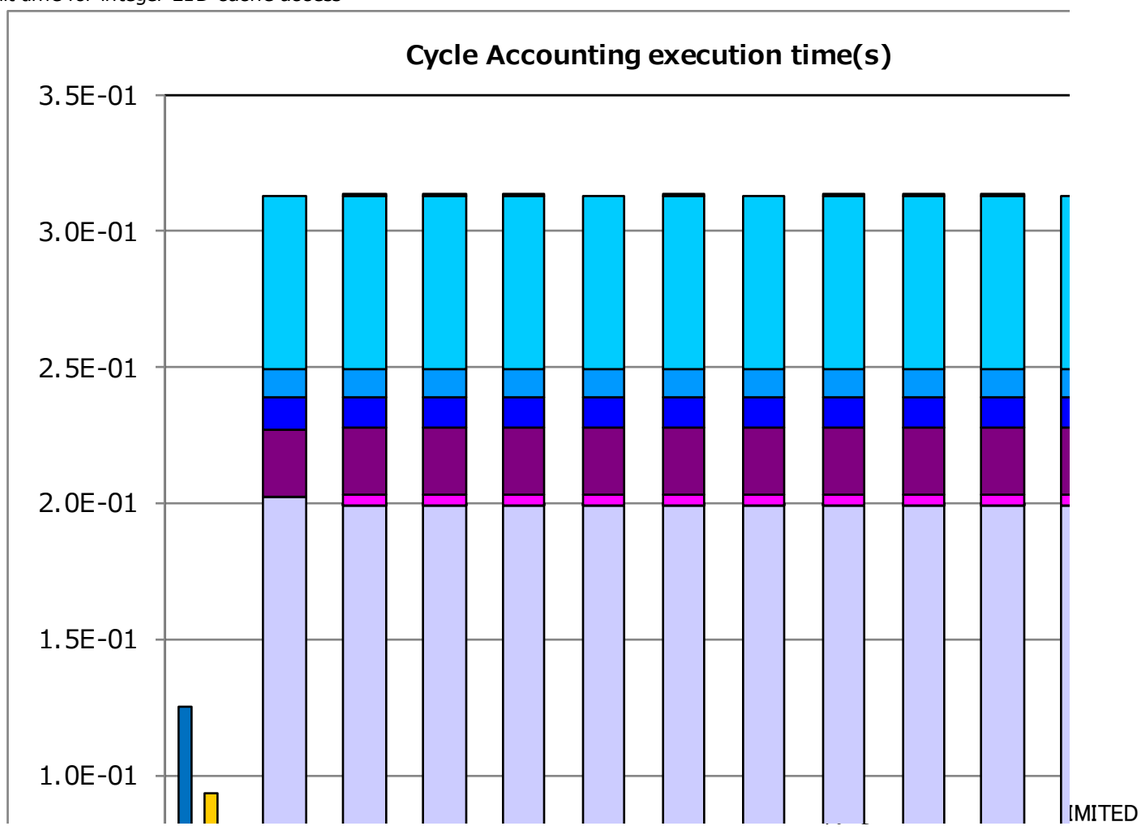
512
2.000

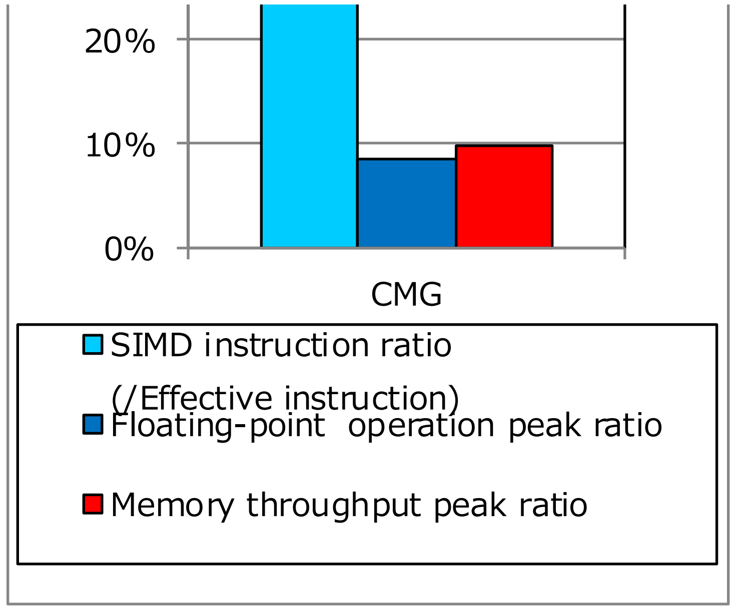
counting	Prefetch port busy wait		Memory access wait & Cache access wait						Operation wait		Other wait				
	Prefetch port busy wait by hardware prefetch	Prefetch port busy wait by software prefetch	Integer load memory access wait	Floating-point load memory access wait	Integer load L2 cache access wait	Integer load L1D cache access wait	Floating-point load L2 cache access wait	Floating-point load L1D cache access wait (*)	Integer operation wait	Floating-point operation wait	Branch instruction wait	Other wait	Store port busy wait	Instruction fetch wait	Barrier synchronization wait
Thread															
0	0.00E+00	0.00E+00	7.96E-05	1.12E-02	4.90E-05	1.72E-03	1.75E-03	2.25E-03	5.18E-04	1.85E-01	2.53E-06	3.31E-06	0.00E+00	1.49E-05	9.50E-05
1	0.00E+00	0.00E+00	7.71E-05	1.09E-02	4.71E-05	1.49E-03	2.22E-03	6.79E-04	5.23E-04	1.83E-01	2.51E-06	3.50E-06	0.00E+00	1.72E-05	4.05E-03
2	0.00E+00	0.00E+00	6.68E-05	1.09E-02	4.83E-05	1.52E-03	2.32E-03	6.88E-04	5.12E-04	1.83E-01	2.42E-06	3.37E-06	0.00E+00	1.67E-05	3.89E-03
3	5.50E-09	0.00E+00	6.90E-05	1.09E-02	4.87E-05	1.50E-03	2.26E-03	6.43E-04	4.88E-04	1.83E-01	2.37E-06	2.90E-06	0.00E+00	1.63E-05	4.03E-03
4	5.00E-09	0.00E+00	8.25E-05	1.10E-02	4.91E-05	1.51E-03	2.47E-03	7.36E-04	4.98E-04	1.83E-01	2.34E-06	3.26E-06	0.00E+00	1.46E-05	3.66E-03
5	0.00E+00	0.00E+00	7.05E-05	1.09E-02	4.92E-05	1.50E-03	2.38E-03	7.03E-04	4.97E-04	1.83E-01	2.47E-06	3.30E-06	0.00E+00	1.68E-05	3.88E-03
6	0.00E+00	0.00E+00	8.40E-05	1.09E-02	5.11E-05	1.48E-03	2.61E-03	5.81E-04	4.98E-04	1.83E-01	2.39E-06	3.46E-06	0.00E+00	1.67E-05	3.87E-03
7	5.00E-09	0.00E+00	8.11E-05	1.09E-02	5.28E-05	1.49E-03	2.58E-03	6.10E-04	5.02E-04	1.83E-01	2.43E-06	2.85E-06	0.00E+00	1.52E-05	3.72E-03
8	0.00E+00	0.00E+00	8.85E-05	1.10E-02	4.91E-05	1.49E-03	2.62E-03	6.75E-04	5.06E-04	1.83E-01	2.20E-06	3.26E-06	0.00E+00	1.58E-05	3.58E-03
9	0.00E+00	0.00E+00	5.99E-05	1.10E-02	4.96E-05	1.48E-03	2.66E-03	6.01E-04	5.09E-04	1.83E-01	2.43E-06	3.31E-06	0.00E+00	1.57E-05	3.72E-03
10	0.00E+00	0.00E+00	8.14E-05	1.07E-02	5.00E-05	1.50E-03	2.64E-03	6.67E-04	4.84E-04	1.83E-01	2.40E-06	3.30E-06	0.00E+00	1.64E-05	3.89E-03
11	0.00E+00	0.00E+00	7.29E-05	1.08E-02	5.16E-05	1.50E-03	2.79E-03	7.40E-04	4.87E-04	1.83E-01	2.28E-06	3.28E-06	0.00E+00	1.54E-05	3.58E-03
CMG 0 total	1.29E-09	0.00E+00	7.61E-05	1.09E-02	4.96E-05	1.51E-03	2.44E-03	7.98E-04	5.02E-04	1.83E-01	2.40E-06	3.26E-06	0.00E+00	1.60E-05	3.50E-03

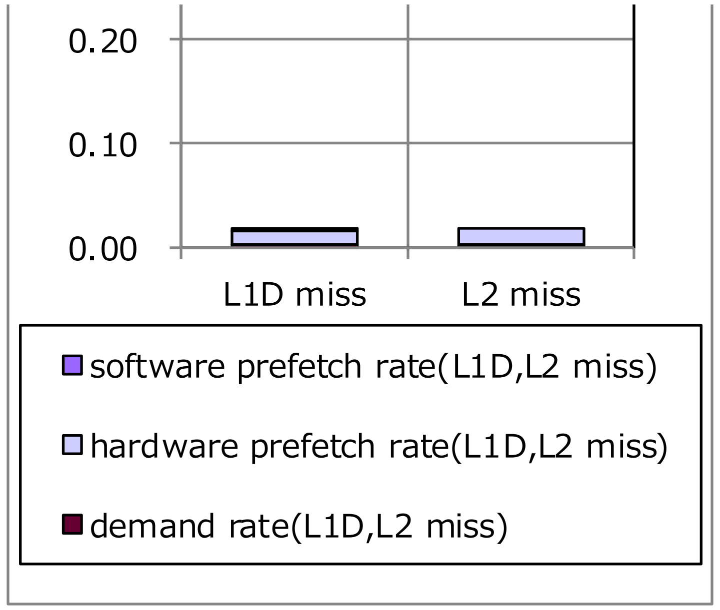
(*) Include wait time for integer L1D cache access

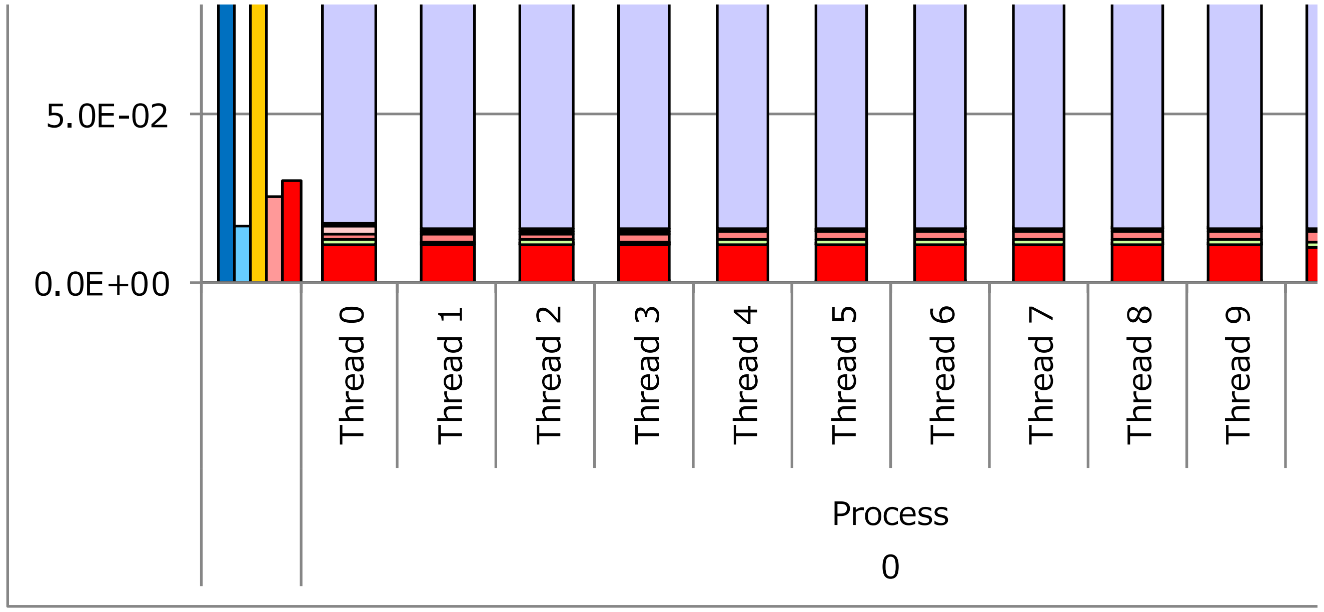










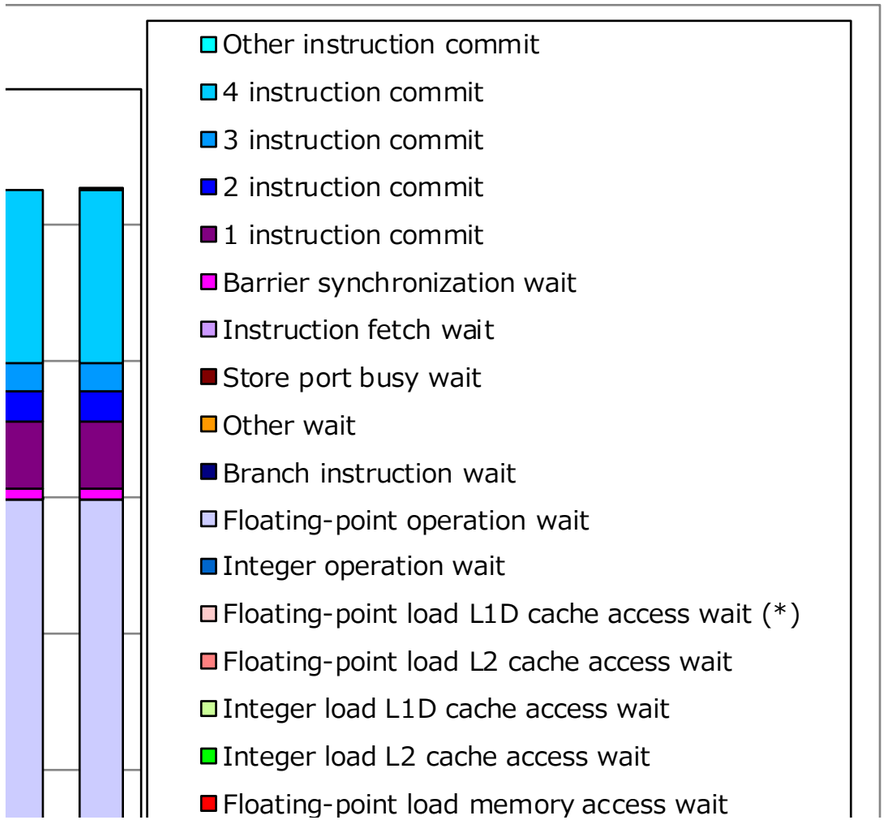


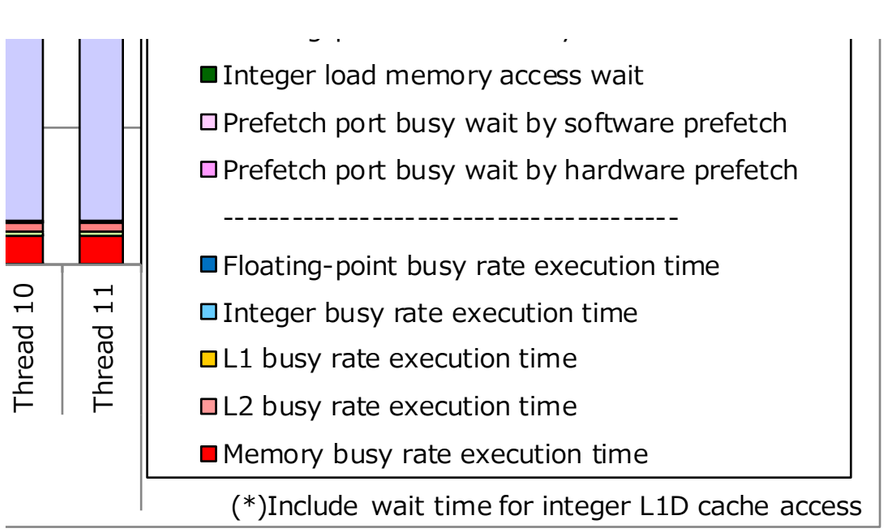
Prefetch instruction			DCZVA instruction	Floating-point instruction			Floating-point move and conversion instruction		Integer instruction	Branch instruction	Predicate instruction	Crypto-graphic instruction	Other instruction	Total
Contiguous prefetch instruction	Gathering prefetch instruction	Scalar prefetch instruction		Floating-point instruction except FMA and reciprocal	FMA instruction	Floating-point reciprocal instruction	Floating-point conversion instruction	Floating-point move instruction						
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	6.14E+06	8.00E+00	2.38E+08	4.92E+07	0.00E+00	0.00E+00	1.48E+08	0.00E+00	1.31E+06	1.01E+02	0.00E+00	8.67E+07	6.64E+08
0.00E+00	0.00E+00	7.37E+07	9.60E+01	2.85E+09	5.90E+08	0.00E+00	0.00E+00	1.78E+09	0.00E+00	1.57E+07	1.21E+03	0.00E+00	1.04E+09	7.97E+09
7.37E+07			9.60E+01	3.44E+09			1.78E+09		0.00E+00	1.57E+07	1.21E+03	0.00E+00	1.04E+09	7.97E+09

Extra		Gather instruction rate (%)			Instruction						Branch prediction miss rate (%)
Process	Thread	0 flow rate (%)	1 flow rate (%)	2 flows rate (%)	Micro-operation instruction	Element manipulated instruction	Register manipulated instruction	MOVPRFX instruction	Math functional instruction	Micro decomposition instruction rate (%)	
0	0	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.07%
0	1	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	2	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	3	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	4	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	5	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	6	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	7	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%

0	8	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	9	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	10	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
0	11	0.00%	25.92%	74.08%	8.12E+08	1.48E+08	6.56E+05	1.47E+08	0.00E+00	100.00%	0.06%
CMG 0 total		0.00%	25.92%	74.08%	9.74E+09	1.78E+09	7.87E+06	1.77E+09	0.00E+00	100.00%	0.06%
		25.92%			9.74E+09	1.79E+09		1.77E+09	0.00E+00	100.00%	0.06%

1 instruction commit	Other instruction commit				Total
	2 instruction commit	3 instruction commit	4 instruction commit	Other instruction commit	
2.48E-02	1.16E-02	1.06E-02	6.32E-02	0.00E+00	3.13E-01
2.44E-02	1.11E-02	1.03E-02	6.37E-02	6.81E-07	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	7.64E-07	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	1.20E-06	3.13E-01
2.44E-02	1.11E-02	1.03E-02	6.37E-02	0.00E+00	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	1.36E-07	3.13E-01
2.45E-02	1.11E-02	1.03E-02	6.37E-02	0.00E+00	3.13E-01
2.44E-02	1.11E-02	1.03E-02	6.37E-02	1.35E-06	3.13E-01
2.44E-02	1.11E-02	1.03E-02	6.37E-02	5.30E-06	3.13E-01
2.44E-02	1.11E-02	1.03E-02	6.37E-02	4.30E-06	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	0.00E+00	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	3.21E-06	3.13E-01
2.44E-02	1.12E-02	1.03E-02	6.37E-02	1.41E-06	3.13E-01





Power Consumption (W)		Power consumption used by core	Power consumption used by L2 cache	Power consumption used by memory
Process	Thread			
0	0	1.94E+00		
0	1	1.94E+00		
0	2	1.94E+00		
0	3	1.94E+00		
0	4	1.94E+00		
0	5	1.94E+00	1.53E+00	3.33E+00
0	6	1.94E+00		
0	7	1.94E+00		
0	8	1.94E+00		
0	9	1.94E+00		
0	10	1.94E+00		
0	11	1.94E+00		
CMG 0 total		2.32E+01	1.53E+00	3.33E+00