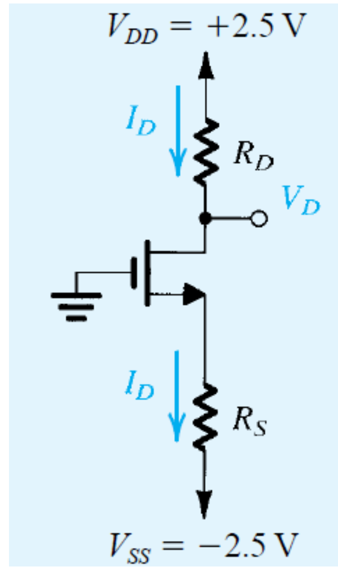
EE210: HW-14

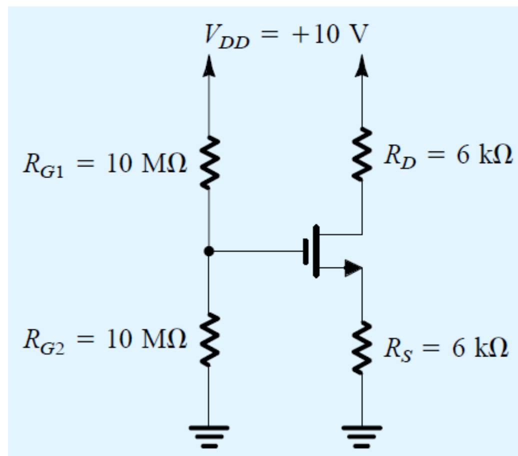
Date: 11/04/2019

Q.1 What are different regions of operation of the Enhancement mode NMOS Transistor?

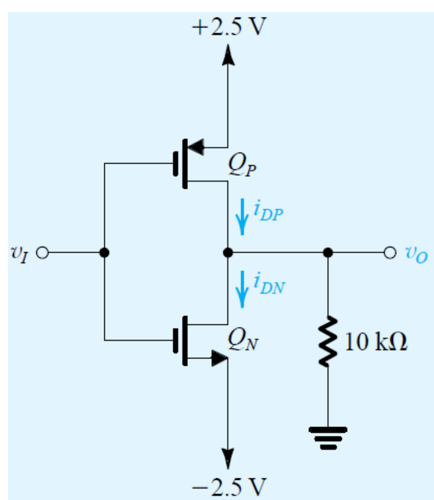
Q.2 Design the circuit of Fig. shown below, that is, determine the values of R_D and R_S, so that the transistor operates at I_D = 0.4 mA and V_D = +0.5 V. The NMOS transistor has Vt = 0.7 V, $\mu_n C_{ox}$ = 100 μA/V^2, L = 1 μm, and W = 32 μm. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).



Q.3 Analyze the circuit shown in Fig. below to determine the voltages at all nodes and the currents through all branches. Let V_{tn} = 1 V and k_n' (W / L) = 1 mA/V^2 and Neglect the channel-length modulation effect.



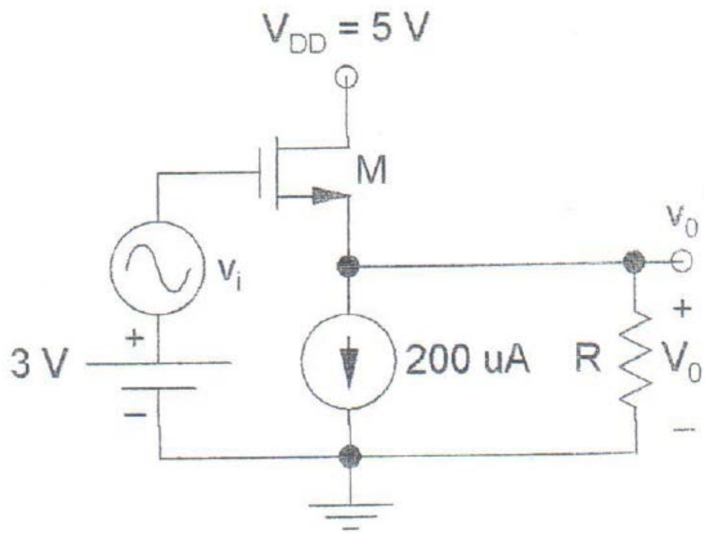
Q.4 The NMOS and PMOS transistors in the circuit shown below are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p)$ = 1 mA/V^2 and, $V_{tn} = -V_{tp}$ = 1 V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for v_I = 0 V, +2.5 V, –2.5 V.



Q.5 For the Common Drain circuit shown in Fig. below, assume that the MOSFET M has $W/L = 10$ and $\lambda = 0$. Other parameters are: $k_n' = 40\ \mu A/V^2$, $\gamma = 0.4\ V^{1/2}$, $2\phi_F = 0.6V$, and $V_{TN0} = 0.7V$. Find the dc output voltage V_0, and the ac small-signal midband voltage gain v_0/v_i under the following conditions:

(i) Ignoring body effect and with $R \rightarrow \infty$.

(ii) Including body effect and with $R \rightarrow \infty$.



Q.6 Repeat Q.5 under the following conditions:

(i) Ignoring body effect and with $R \rightarrow 100k\Omega$.

(ii) Including body effect and with $R \rightarrow 10k\Omega$.