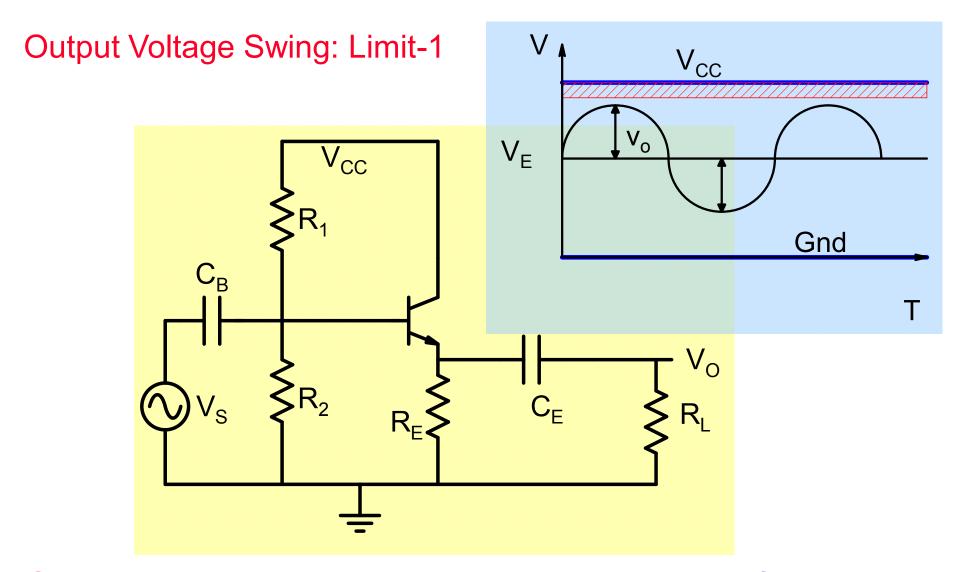
EE210: Microelectronics-I

Lecture-26 : Common Collector Amplifier-2

Instructor - Y. S. Chauhan

Slides - B. Mazhari Dept. of EE, IIT Kanpur

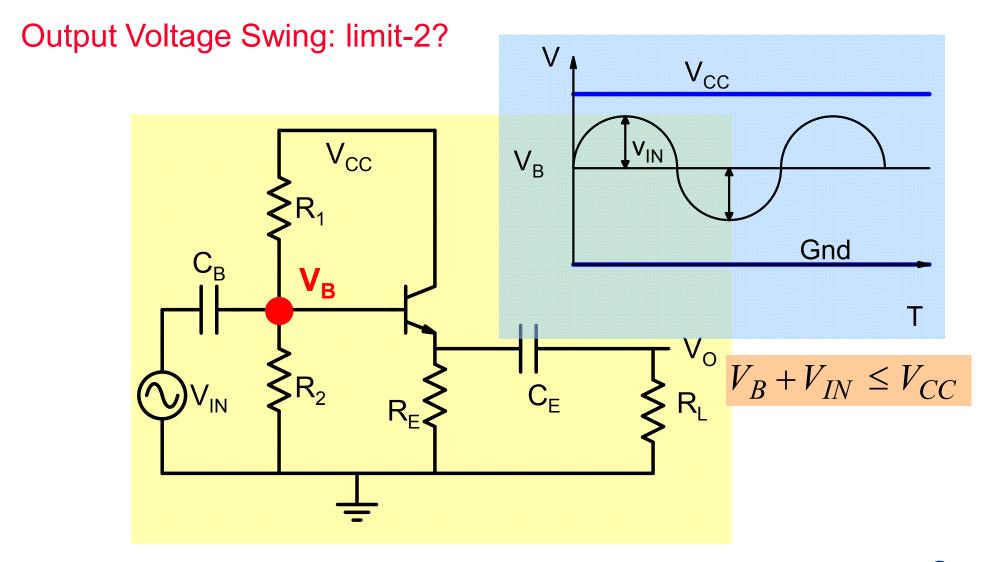
Output Voltage Swing



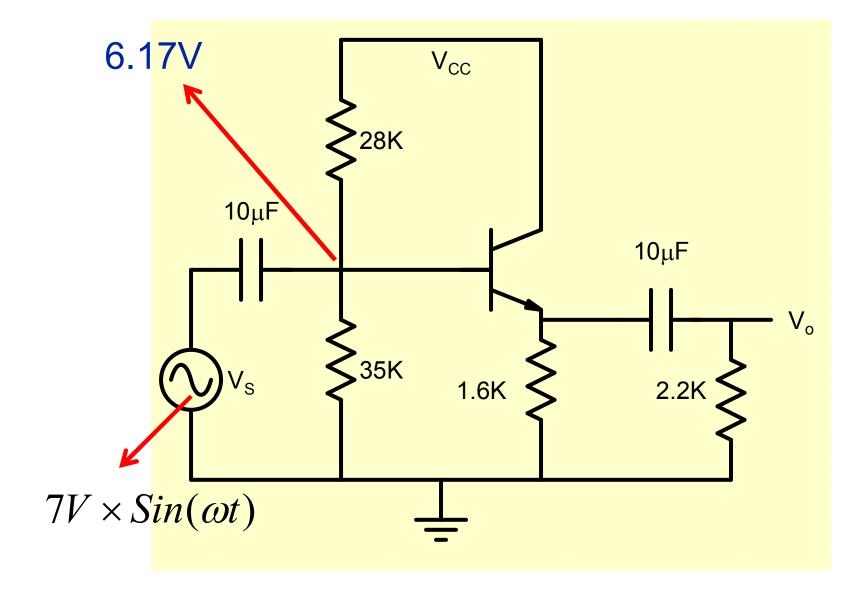
One constraint: Transistor should stay out of saturation

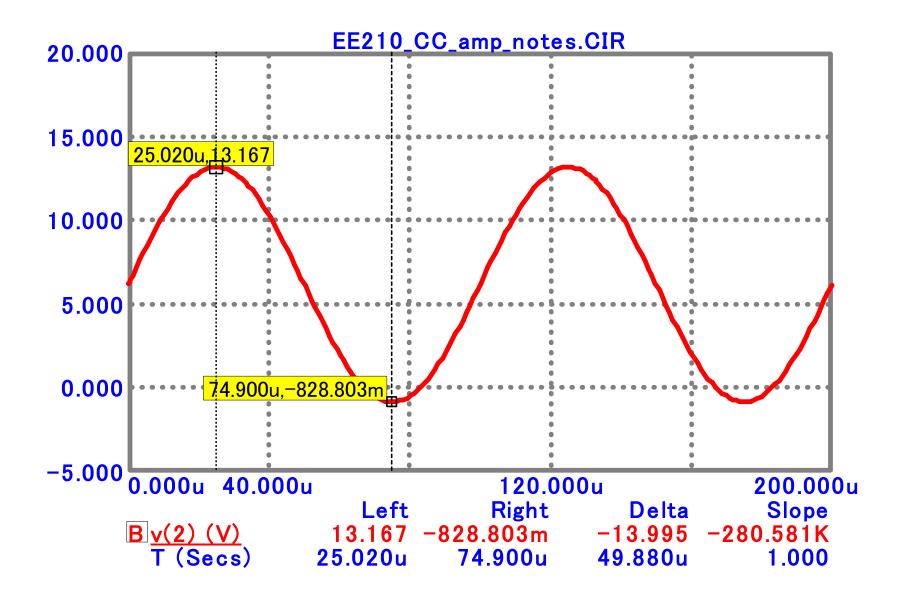
$$V_{CC} - (V_E + V_O) \ge V_{CEsat}$$

$$V_O \le V_{CC} - V_{CEsat} - I_{CQ} R_E$$

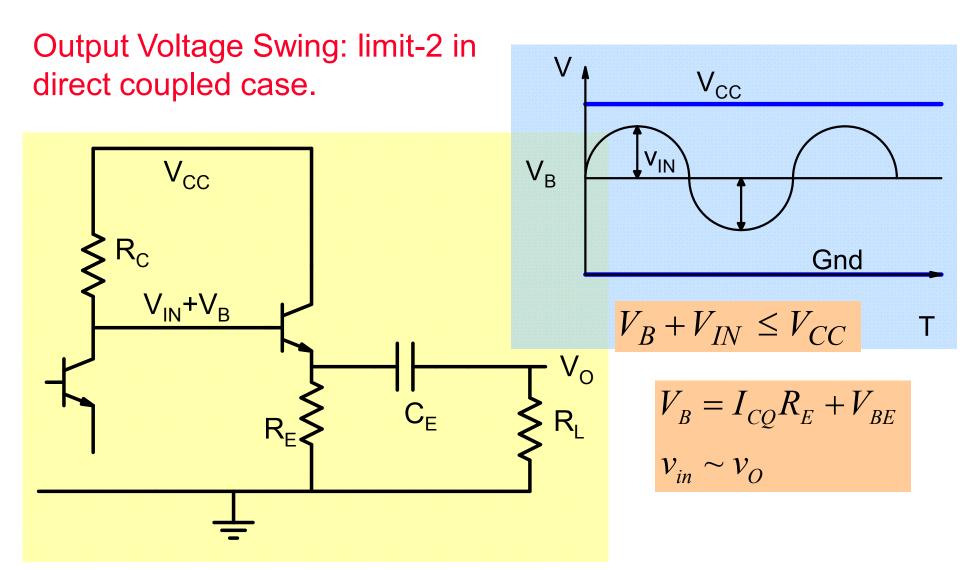


Constraint-2: Maximum voltage at base is always less than V_{CC}?





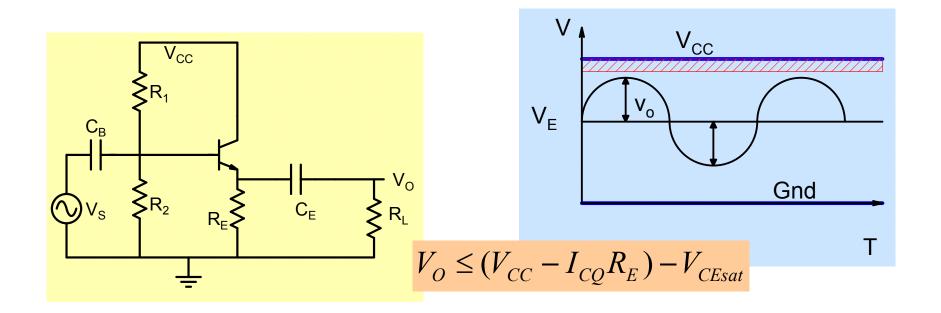
Voltage can exceed +12V supply voltage

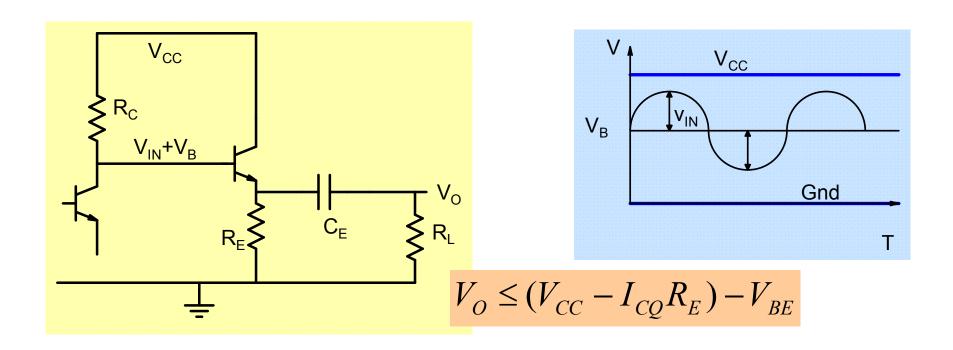


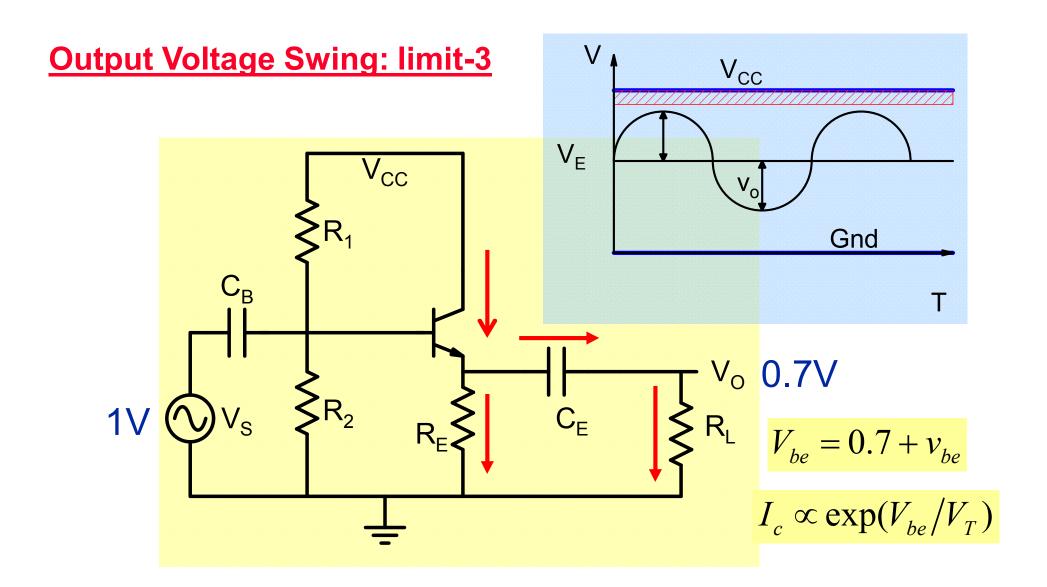
Constraint-2: Maximum voltage is always less than V_{CC}

$$I_{CQ}R_E + V_{BE} + v_O \le V_{CC}$$

$$v_O \le V_{CC} - V_{BE} - I_{CQ} R_E$$

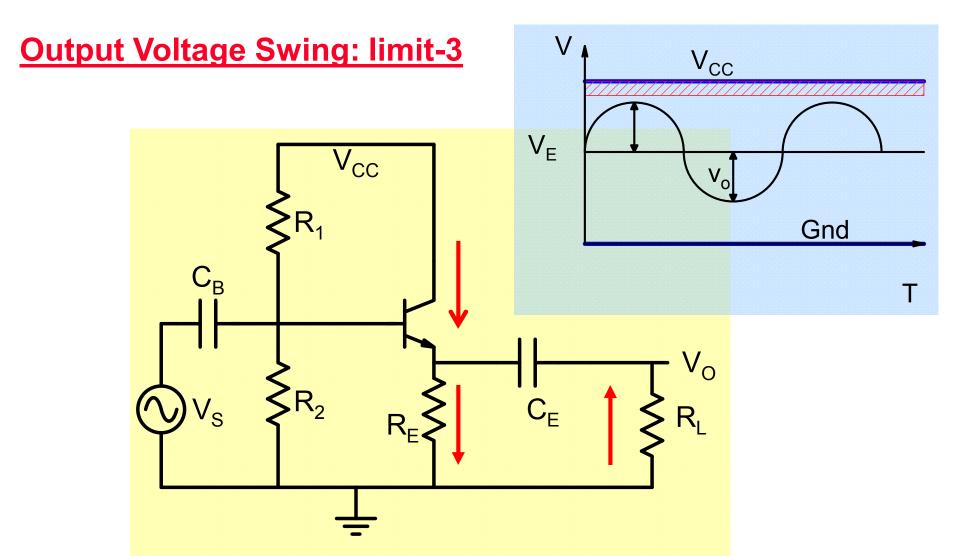






Constraint-3: There should be enough drive current

$$I_c = \frac{V_E + v_O}{R_E} + \frac{v_O}{R_L}$$



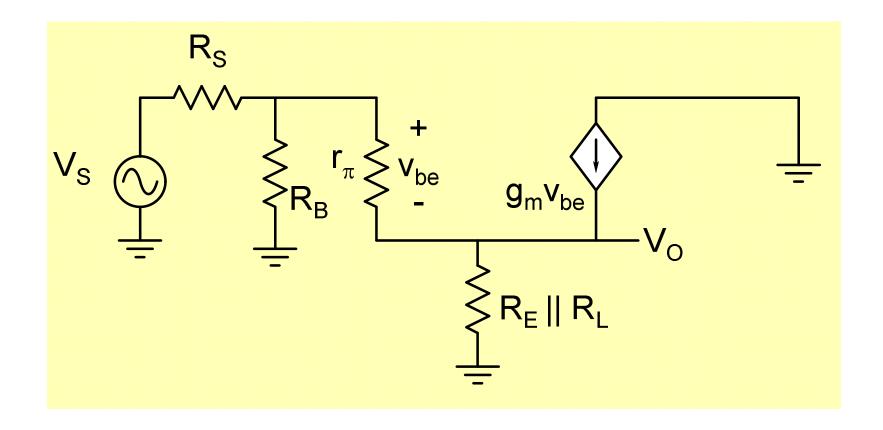
Constraint-3: There should be enough drive current

$$\frac{V_{E} - v_{O}}{R_{E}} = \frac{v_{O}}{R_{L}} + I_{c} \qquad \frac{I_{CQ}R_{E} - v_{O}}{R_{E}} \ge \frac{v_{O}}{R_{L}} \qquad v_{O} \le I_{CQ}R_{E} \| R_{L}$$

$$\frac{I_{CQ}R_E - v_O}{R_E} \ge \frac{v_O}{R_L}$$

$$v_O \leq I_{CQ} R_E \| R_L$$

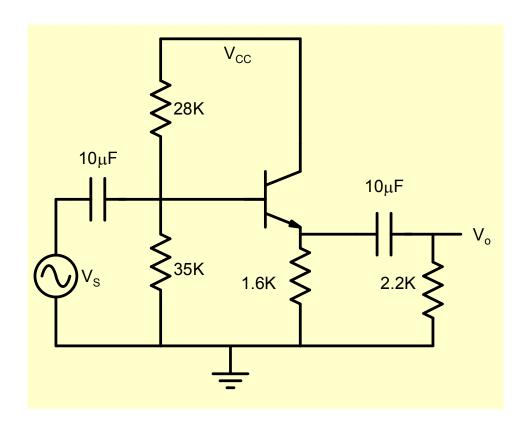
Nonlinearity leading to harmonic distortion



$$v_S' = i_b R_S' + v_{be} + v_O \approx v_O$$

Thus transfer characteristics is expected to be quite linear

Example

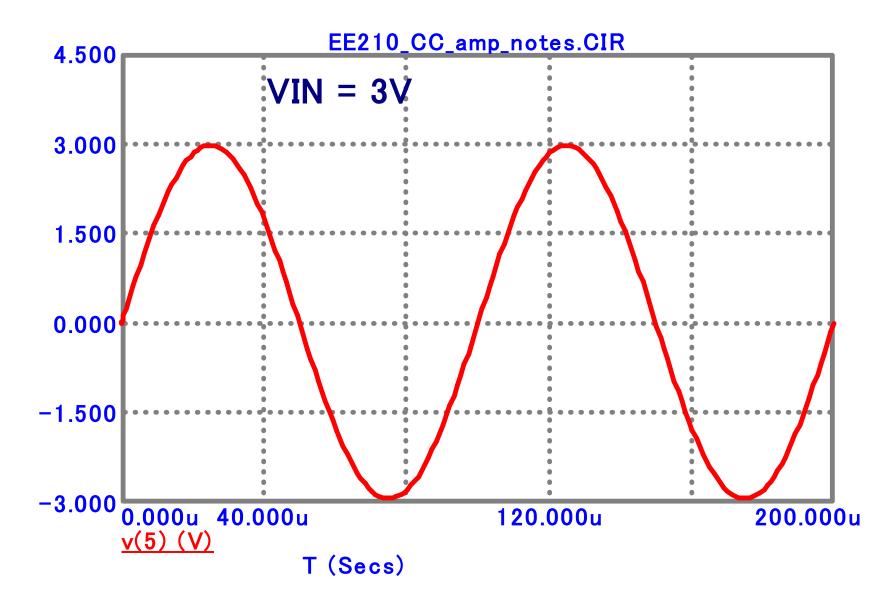


$$\beta = 100$$
 $I_{CQ} = 3.4 mA; V_{CEQ} = 6.5 V$
 $A_{V} = 0.99;$
 $R_{in} = 13.4 K (R_{B} = 16 k)$
 $R_{O} = 9.5 \Omega$

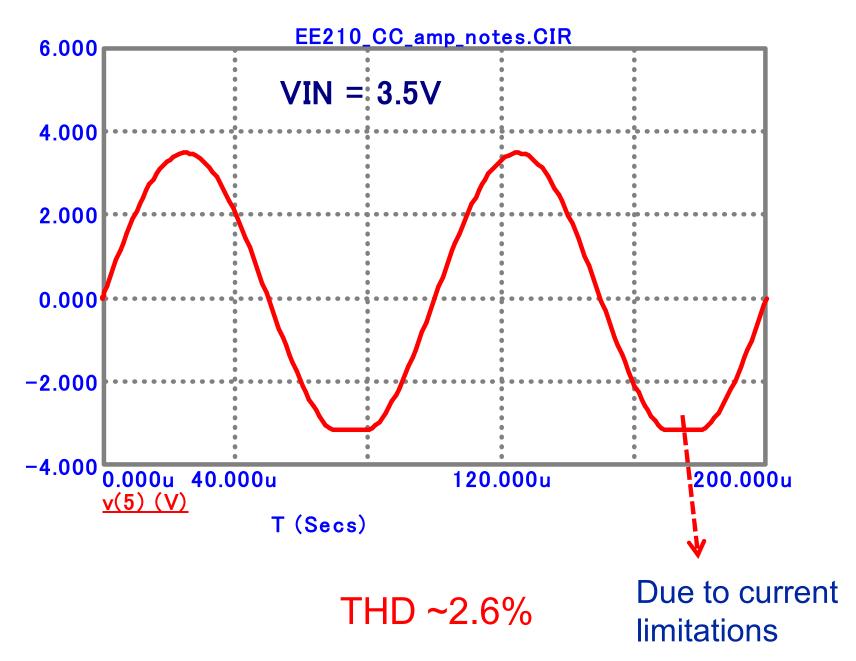
$$V_O \le V_{CC} - V_{BE} - I_{CQ} R_E = 5.85V$$

$$V_O \leq I_{CQ} R_E \| R_L = 3.2V$$

$$V_{OM} \sim 3.2V$$



THD ~0.5%



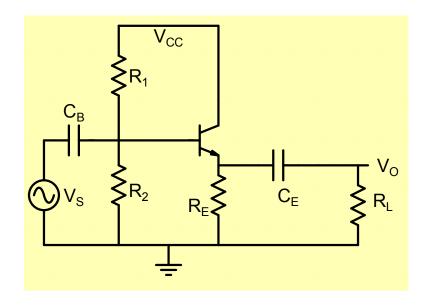
Design for Maximum Voltage Swing

$$V_O \leq I_{CQ} R_E \| R_L$$

$$V_O \leq V_{CC} - V_{BE} - I_{CQ} R_E$$

$$\begin{split} V_{O} &= Min \{ V_{CC} - V_{BE} - I_{CQ} R_{E}; I_{CQ} R_{E} \| R_{L} \} \\ V_{CC} - V_{BE} - I_{CQ} R_{E} &= I_{CQ} R_{E} \| R_{L} \\ I_{CQ} &= \frac{V_{CC} - V_{BE}}{R_{E}} \times \frac{1 + R_{E} / R_{L}}{2 + R_{E} / R_{L}} \\ V_{O} &= \frac{V_{CC} - V_{BE}}{2 + R_{E} / R_{L}} \end{split}$$

Design For Maximum Voltage Swing



$$\begin{split} V_{O} &= \frac{V_{CC} - V_{BE}}{2 + R_{E}/R_{L}} \\ I_{CQ} &= \frac{V_{CC} - V_{BE}}{R_{E}} \times \frac{1 + R_{E}/R_{L}}{2 + R_{E}/R_{L}} \end{split}$$

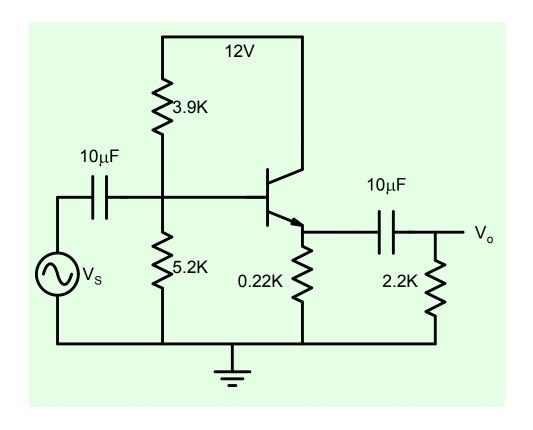
Design criterion: Choose $R_E \ll R_L$

$$v_{om} \sim 5.6$$
 for $V_{CC} = 12V$

However, this makes I_{CQ} large leading to high power dissipation and lower input resistance

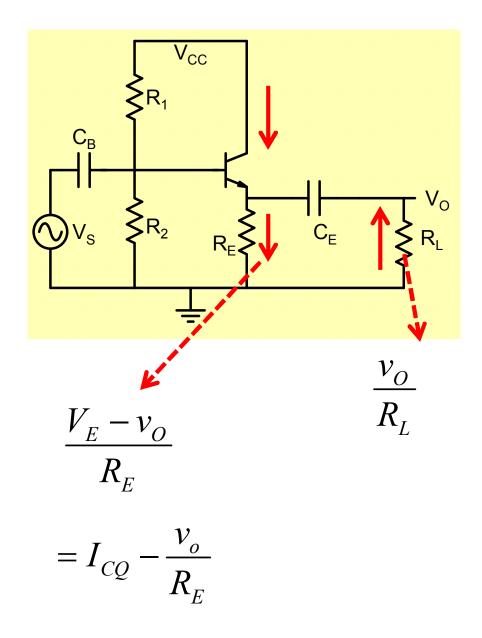
$$\begin{split} V_{O} &= \frac{V_{CC} - V_{BE}}{2 + R_{E}/R_{L}} \\ I_{CQ} &= \frac{V_{CC} - V_{BE}}{R_{E}} \times \frac{1 + R_{E}/R_{L}}{2 + R_{E}/R_{L}} \end{split}$$

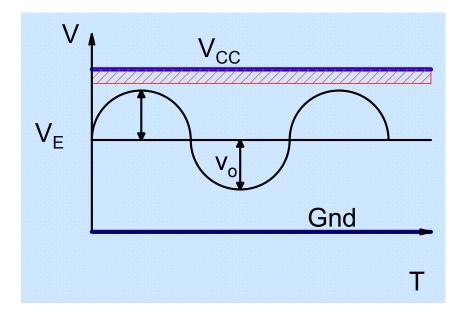
For
$$R_E \ll R_L$$
:
$$I_{CQ} \sim \left(\frac{V_o}{R_L}\right) \times \left(\frac{R_L}{R_E}\right)$$

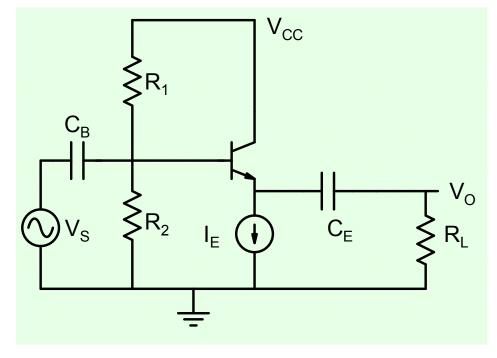


$$I_{CQ} = 25mA; V_{CEQ} = 6.5V$$

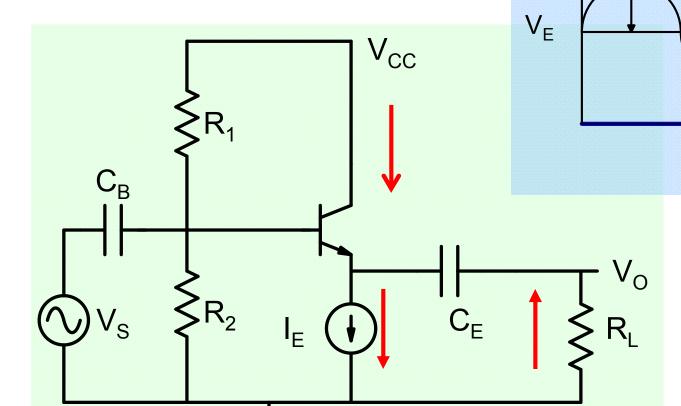
 $A_V = 0.98; R_{in} = 2K; R_O = 3\Omega$
 $V_{om} = 5.6V$







Current Source Biasing



$$I_E = \frac{v_O}{R_L} + I_c$$

$$I_E \ge \frac{v_O}{R_L}$$

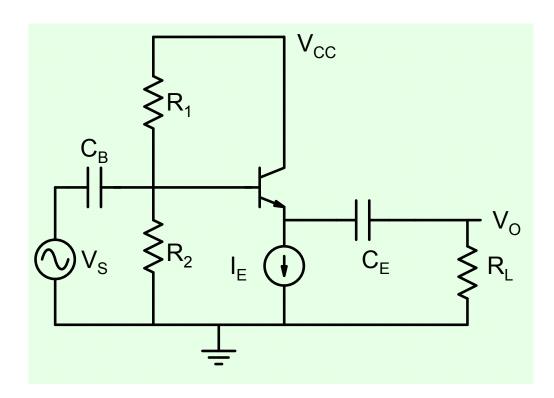
$$v_O \leq I_{EQ} R_L$$

Gnd

 V_{CC}

$$V_E - v_O \ge 0$$

Maximum Voltage Swing



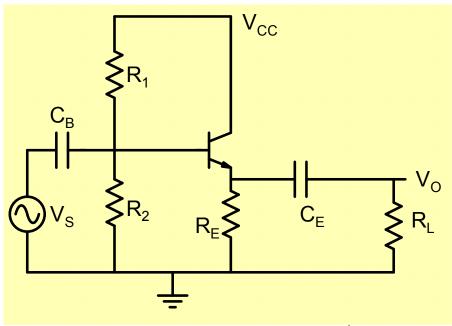
$$V_O \leq V_{CC} - V_{BE} - V_E$$

$$V_E - v_O \ge 0$$

$$V_O = V_E = \frac{V_{CC} - V_{BE}}{2}$$

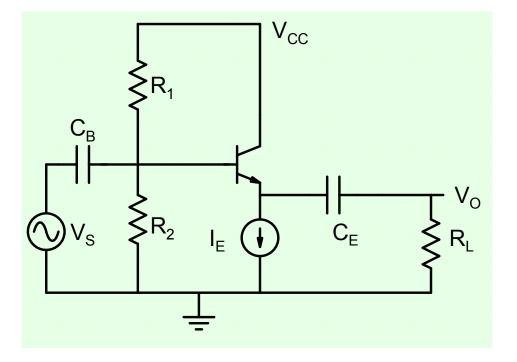
$$v_O \leq I_{EQ} R_L \Rightarrow I_{EQ} \geq \frac{V_O}{R_L}$$

Design for Maximum Voltage Swing



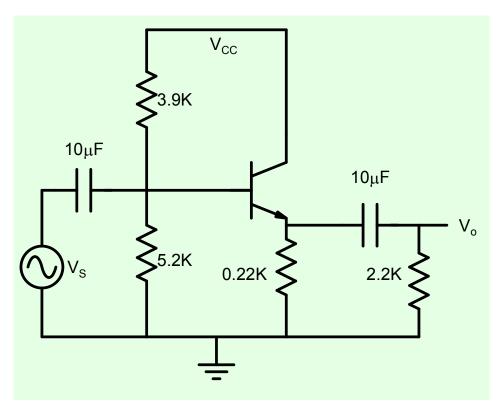
$$I_{CQ} = rac{V_{CC} - V_{BE}}{R_E} imes rac{1 + R_E/R_L}{2 + R_E/R_L}$$
 $V_O = rac{V_{CC} - V_{BE}}{2 + R_E/R_L}$

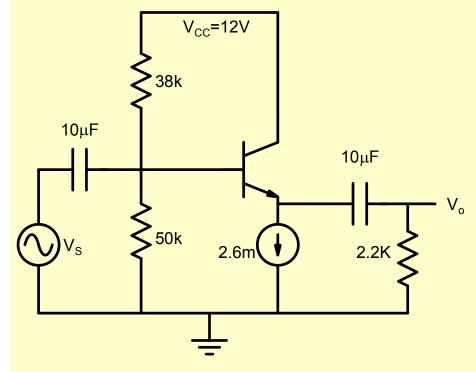
For
$$R_E << R_L : I_{CQ} = \frac{V_{CC} - V_{BE}}{2R_E}$$



$$V_O = \frac{V_{CC} - V_{BE}}{2}$$

$$I_E \cong \frac{V_{CC} - V_{BE}}{2R_L}$$





$$I_{CQ} = 25mA; V_{CEQ} = 6.5V$$

$$A_{V} = 0.98; R_{in} = 2K; R_{O} = 3\Omega$$

$$V_{om} = 5.6V$$

$$\begin{split} I_{CQ} &= 2.6 mA; V_{CEQ} = 6.5 V \\ A_{V} &= 0.99; R_{in} = 19.7 K; R_{O} = 9.5 \Omega \\ V_{om} &= 5.6 V \end{split}$$

