1. An npn transistor has a maximum operable frequency (f_{max}) of 5 GHz, and the ratio of its alpha cutoff frequency (f_α) to unity gain cutoff frequency (f_T) is 1.01.

a) The transistor needs to be biased such that the following performance requirements are met:
   * The small-signal output resistance (r_0) is 100 kΩ
   * The common-emitter current gain (β) is 10 at a frequency of 100 MHz

   Determine the required bias point (I_{CQ}, V_{CEQ}). Assume that the base-collector junction is linearly graded with a built-in potential of 0.7 V. Data: I_S = 14 fA, V_A = 100 V, C_{je0} = 2 pF, $C_{\mu 0}$ = 1.5 pF. **13**

b) Now, keeping I_{CQ} constant, if V_{CE} is *increased* beyond V_{CEQ}, state with clear justification whether the value of β (at 100 MHz) would increase or decrease from its design value of 10. **2**

a) $f_{max} = \frac{1}{2\pi \tau_F} \Rightarrow \tau_F = \frac{1}{2\pi f_{max}} = \frac{1}{2\pi \times 5 \times 10^9} =$ **31.83 ps**

$f_\alpha = (\beta_0 + 1) f_\beta$ & $f_T = \beta_0 f_\beta \Rightarrow \frac{f_\alpha}{f_T} = \frac{\beta_0 + 1}{\beta_0} = 1 + \frac{1}{\beta_0} = 1.01 \Rightarrow$ **$\beta_0 = 100$**

$r_o = \frac{V_A}{I_{CQ}} = 100\ k\Omega \Rightarrow I_{CQ} = \frac{V_A}{100\ k\Omega} = \frac{100\ V}{100\ k\Omega} =$ **1 mA** ⟸

$I_{CQ} = I_S e^{V_{BEQ}/V_T} \Rightarrow V_{BEQ} = V_T \ln \frac{I_{CQ}}{I_S} = (26\ mV) \times \ln \frac{1\ mA}{14\ fA} =$ **0.65 V**

At f = 100 MHz, β has dropped to 10 ($\ll \beta_0$ of 100)

$\Rightarrow f_\beta = \frac{\beta f}{\beta_0} = \frac{10 \times 100\ MHz}{100} =$ **10 MHz** $\Rightarrow f_T = \beta_0 f_\beta =$ **1 GHz**

$C_{je} = 2 C_{je0} =$ **4 pF** $\quad g_m \tau_F = \frac{I_{CQ}}{V_T} \times \tau_F = \frac{1\ mA}{26\ mV} \times 31.83\ ps =$ **1.22 pF**

$\Rightarrow C_\pi = C_{je} + g_m \tau_F =$ **5.22 pF**

$f_T = \frac{g_m}{2\pi (C_\pi + C_\mu)} \Rightarrow C_\mu = \frac{g_m}{2\pi f_T} - C_\pi = \frac{1}{26} \times \frac{1}{2\pi \times 10^9} - 5.22\ pF =$ **0.9 pF**

$C_\mu = \frac{C_{\mu 0}}{\left(1 - \frac{V_{BCQ}}{V_0}\right)^m}$ with $m = \frac{1}{3}$ (linearly graded jn.)

$\Rightarrow \left(1 - \frac{V_{BCQ}}{V_0}\right) = \left(\frac{C_{\mu 0}}{C_\mu}\right)^{1/m} = \left(\frac{1.5\ pF}{0.9\ pF}\right)^3 = 4.63 \Rightarrow V_{BCQ} =$ **− 2.54 V**

$\Rightarrow V_{CEQ} = V_{BEQ} - V_{BCQ} = 0.65 - (-2.54) =$ **3.19 V** ⟸

Reqd. bias pt. $I_{CQ} =$ **1 mA** $\quad V_{CEQ} =$ **3.19 V**

b) I_{CQ} const ⇒ g_m const. $\quad V_{CEQ} \uparrow \Rightarrow V_{CBQ} \uparrow \Rightarrow$ CB jn. getting more rev. biased

$\Rightarrow C_\mu \downarrow \Rightarrow f_T \uparrow \Rightarrow f_\beta \uparrow \Rightarrow \beta \uparrow \Rightarrow$ **β would increase**

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2. An n-channel MOSFET is operated with its source tied at −1 V (*minus* 1 V).
   a) Determine the body voltage (V_B) that would make it operate with a body factor (χ) of 0.1. **2**
   b) Now, with the value of V_B calculated in part a), but with small-signal $v_{bs} = 0$, the device is desired to have a transconductance (g_m) of 100 μA/V and a unity gain cutoff frequency (f_T) of 1 GHz, at a gate voltage (V_G) of 1 V. Determine the required values (*in μm*) of channel length and width (L and W respectively) that would ensure this. Neglect gate-source and gate-drain overlap capacitances. **9**
   c) In order to achieve the performance specifications given in part b), calculate the *minimum* required value of the drain voltage (V_D). What is the power dissipation of the device under this condition? **4**

Data: $V_{TN0} = 1$ V, $k'_N = 40\ \mu A/V^2$, $\gamma = 0.4\ V^{1/2}$, $2\phi_F = 0.6$ V, $\mu_n = 400\ cm^2/V\text{-sec}$, $\lambda \to 0$.

a) $\chi = \dfrac{\gamma}{2\sqrt{2\phi_F - V_{BS}}} = 0.1 \Rightarrow \dfrac{0.4}{2\sqrt{0.6 - V_{BS}}} = 0.1 \Rightarrow V_{BS} = \underline{-3.4\,V}$

$\Rightarrow V_B = -3.4 + V_S = \boxed{-4.4\,V}$ ($\because V_S = -1V$)

b) $V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) = 1 + 0.4\left(\sqrt{0.6+3.4} - \sqrt{0.6}\right) = \underline{1.49V}$

$V_{GS} = V_G - V_S = \underline{2V} \Rightarrow V_{GT} = V_{GS} - V_{TN} = \underline{0.51V}$

$g_m = K_n' \frac{W}{L} V_{GT} = 100\,\mu A/V \Rightarrow \frac{W}{L} = \frac{100}{40 \times 0.51} = \boxed{4.9}$

C_{gso}, C_{gdo} neglected. $C_{ox}' = \dfrac{K_n'}{\mu_n} = \dfrac{40\,\mu A/V^2}{400\ cm^2/V\text{-s}} = \underline{10^{-7}\ F/cm^2}$

$f_T = \dfrac{g_m}{2\pi C_{gs}}$ $\because C_{gd} = 0$ & $C_{gs} = C_{gsi} = \frac{2}{3} WL C_{ox}'$ (assumed saturated)

$\Rightarrow C_{gs} = \dfrac{100\,\mu A/V}{2\pi \times 1\,GHz} = \underline{15.92\,fF} \Rightarrow WL = \dfrac{15.92\,fF \times 3}{2 \times 10^{-7}\ F/cm^2} = \underline{2.39 \times 10^{-7}\ cm^2}$

Also, $W = 4.9L \Rightarrow 4.9L^2 = 2.39 \times 10^{-7} \Rightarrow L = \underline{2.2 \times 10^{-4}\ cm} = \boxed{2.2\,\mu m}$

& $W = 4.9L = \boxed{10.8\,\mu m}$

c) Obviously, all the above calculations are based on the assumption that the MOSFET is operating in the saturation region.

$\therefore V_{DS}|_{min} = V_{DS,sat} = \Delta V = V_{GT} = \underline{0.51V} \Rightarrow V_D = 0.51 + V_S = \boxed{-0.49V}$

Corresponding $I_D = \dfrac{K_n'}{2}\dfrac{W}{L} V_{GT}^2 = \dfrac{40}{2} \times 4.9 \times 0.51^2 = \underline{25.5\,\mu A}$

& Device Power Dissipation $= V_{DS} \times I_D = 0.51\,V \times 25.5\,\mu A = \boxed{13\,\mu W}$

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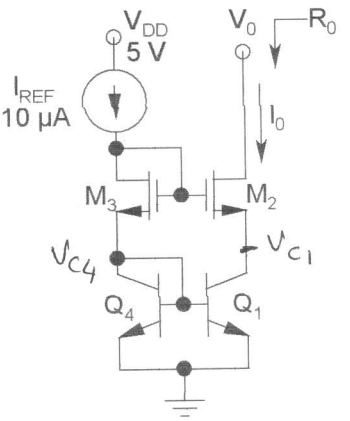
3. The circuit shown in the figure is a BiMOS (combination of bipolar and MOS) cascode current source. Transistors Q_1 and Q_4 are perfectly matched, and so are the transistors M_2 and M_3. Data: M_2-M_3: $V_{TN0} = 0.7$ V, $k'_N = 40\ \mu A/V^2$, and $dX_d/dV_{DS} = 0.05\ \mu m/V$ (but $\lambda V_{DS} \ll 1$), *neglect body effect*; Q_1-Q_4: $V_A = 50$ V (but $V_{CE}/V_A \ll 1$), *neglect base currents*. Assume the current source I_{REF} to be ideal.



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a) Clearly draw the ac small-signal equivalent of the circuit, and show that the output resistance (R_0) can be expressed as $R_0 \approx g_{m2}r_{02}r_{01}$, where all notations carry their usual meanings.

b) Design the values of the width and length (W and L respectively) of M_2 (and thus of M_3) to satisfy the following performance requirements:
   i) At $V_0 = V_{0(min)} = 0.9$ V, I_0 must be 10 μA, and
   ii) I_0 must not increase by more than 0.0625% (of 10 μA) for a 5 V increase in V_0 beyond $V_{0(min)}$.

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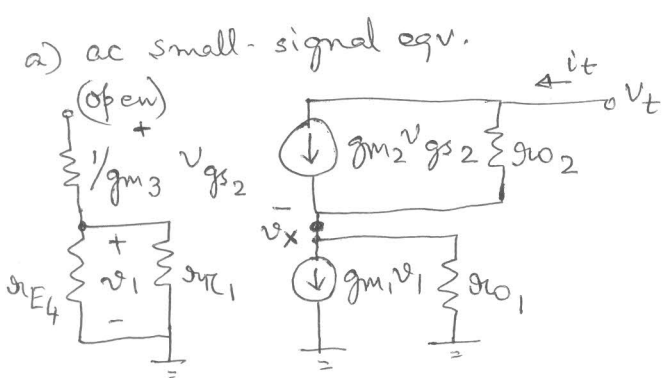
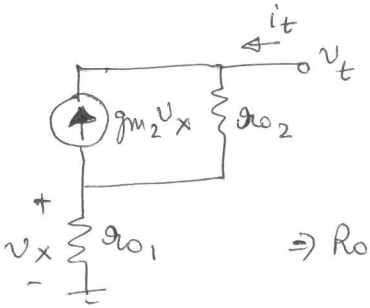
a) ac small-signal eqv.





$$i_t = -g_{m2}v_x + \frac{v_t - v_x}{r_{o2}}$$

with $v_x = i_t r_{o1}$

$$\Rightarrow R_o = \frac{v_t}{i_t} = r_{o2}(1 + g_{m2}r_{o1}) \simeq g_{m2}r_{o2}r_{o1} \quad \text{(Shown)}$$

No Source $\Rightarrow v_1 = 0 \Rightarrow g_{m1}v_1 = 0$, & $v_{gs2} = -v_x$

b) $V_{C4} = 0.7$ V ($\because V_{BE4} = 0.7$ V) $\Rightarrow V_{C1} = 0.7$ V (by symmetry)

$\therefore V_{o,min} = V_{C1} + \Delta V_2 = 0.9$ V $\Rightarrow \Delta V_2 = \underline{0.2\ V}$

$$I_0 = \frac{K_n'}{2}\left(\frac{W}{L}\right)_2 (\Delta V_2)^2 = 10\ \mu A \Rightarrow \left(\frac{W}{L}\right)_2 = \underline{12.5}$$

$$R_o = \frac{\Delta V_o}{\Delta I_o} = \frac{5\ V}{0.0625\%\ \text{of}\ 10\ \mu A} = \frac{5\ V}{6.25\ nA} = \underline{800\ M\Omega}$$

$$g_{m2} = \sqrt{2K_n'\left(\frac{W}{L}\right)_2 I_0} = \underline{10^{-4}\ \mho} \qquad r_{o1} = \frac{V_{A1}}{I_0} = \underline{5\ M\Omega}$$

$$\& \quad r_{o2} = \frac{R_o}{g_{m2}r_{o1}} = \frac{800\ M\Omega}{10^{-4}\ \mho \times 5\ M\Omega} = \underline{1.6\ M\Omega} = \frac{1}{\lambda I_0} \Rightarrow \boxed{\lambda = 0.0625\ V^{-1}}$$

$$\text{Also,} \quad \lambda = \frac{1}{L_2}\frac{dX_d}{dV_{DS}} \Rightarrow L_2 = \frac{1}{\lambda}\frac{dX_d}{dV_{DS}} = \frac{1}{0.0625} \times 0.05 = \underline{0.8\ \mu m}$$

$$\Rightarrow W_2 = 12.5 \times L_2 = \underline{10\ \mu m} \Rightarrow \boxed{L_2 = L_3 = 0.8\ \mu m\ \&\ W_2 = W_3 = 10\ \mu m}$$

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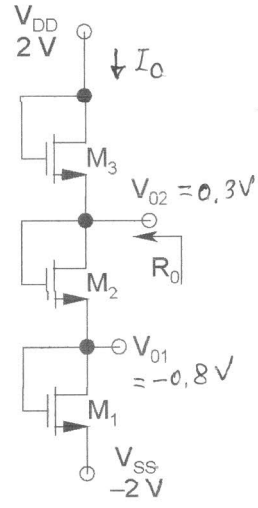
4. The NMOS voltage reference shown in the figure, is required to produce reference voltages V_{01} and V_{02} of –0.8 V and 0.3 V respectively. Data: MFS = 0.5 μm, $k'_N = 40\ \mu A/V^2$, $V_{TN0} = 0.7$ V, $\gamma = 0.4\ V^{1/2}$, $2\phi_F = 0.6$ V, and *neglect channel length modulation effect*.



a) Which of the three transistors (M_1-M_3) would you pick to be the minimum-sized unit transistor in order to produce the least dc power dissipation in the circuit? *You have to justify your answer quantitatively*. Calculate this minimum dc power. **6**

b) Based on the scheme chosen in a), determine the W and L for each of the transistors, and compute the total area of the circuit (*attempt should be made to reduce this area as much as possible*). **3**

c) *Neglecting body effect* in the ac analysis, calculate the output resistance (R_0) of the voltage reference V_{02}. **4**

d) Now, in part c), if body effect were included, how would the result change? *No calculation necessary, mere explanation will suffice*. **2**

a) Dual Supply Circuit ⇒ All Bodies Connected to the most –ve supply ($V_{SS} = -2V$).

$V_{BS_1} = 0$ $V_{GS_1} = V_{01} - V_{SS} = -0.8 - (-2) = \underline{1.2V}$ $V_{TN1} = V_{TN0} = \underline{0.7V} \Rightarrow \Delta V_1 = \underline{0.5V}$

$V_{BS_2} = V_{B_2} - V_{S_2} = (-2) - (-0.8) = \underline{-1.2V}$ $V_{TN_2} = V_{TN0} + \gamma\left(\sqrt{2\phi_F - V_{BS_2}} - \sqrt{2\phi_F}\right) = \underline{0.927V}$

$V_{GS_2} = V_{G_2} - V_{S_2} = 0.3 - (-0.8) = \underline{1.1V}$ $\Delta V_2 = \underline{0.173V}$

$V_{BS_3} = V_{B_3} - V_{S_3} = -2 - 0.3 = \underline{-2.3V}$ $V_{TN_3} = \underline{1.07V}$ $V_{GS_3} = \underline{1.7V}$ $\Delta V_3 = \underline{0.63V}$

$\because \Delta V_2$ is minimum, $\therefore$ pick M_2 as the min. sized unit transistor to produce least dc power dissipation in the circuit.

$\Rightarrow I_0 = \frac{K_n'}{2}\left(\frac{W}{L}\right)_2 \Delta V_2^2 = \frac{40}{2} \times 1 \times 0.173^2 = \boxed{0.6\mu A}$ & $P_{DC} = (V_{DD} + |V_{SS}|) \times I_0 = \boxed{2.4\mu W}$

b) We already have $\boxed{W_2 = L_2 = MFS = 0.5\mu m}$

$(W/L)_1 = \frac{2I_0}{K_n' \Delta V_1^2} = \frac{2 \times 0.6\mu A}{40\mu A/V^2 \times 0.5^2} = \underline{0.12} \Rightarrow \boxed{W_1 = MFS = 0.5\mu m}$ $\boxed{L_1 = 4.17\mu m}$

& $(W/L)_3 = \frac{2I_0}{K_n' \Delta V_3^2} = \frac{2 \times 0.6\mu A}{40\mu A/V^2 \times 0.63^2} = \underline{0.0756} \Rightarrow \boxed{W_3 = MFS = 0.5\mu m}$ $\boxed{L_3 = 6.615\mu m}$

Area $= \Sigma WL = 0.5\mu m \times (0.5 + 4.17 + 6.615)\mu m = \boxed{5.64\mu m^2}$

c) M_1 M_2 M_3 all are diode connected, $\therefore$ neglecting body effect, all of them produce a resistance of $1/g_m$ each. Thus, $R_0 = \frac{1}{g_{m3}} \| \left(\frac{1}{g_{m2}} + \frac{1}{g_{m1}}\right)$

$g_{m_1} = K_{n_1} V_{GT_1} = 40 \times 0.12 \times 0.5 = \underline{2.4\mu V}$ $g_{m_2} = K_{n_2} V_{GT_2} = 40 \times 1 \times 0.173 = \underline{6.92\mu V}$

& $g_{m_3} = K_{n_3} V_{GT_3} = 40 \times 0.0756 \times 0.63 = \underline{1.9\mu V}$ $\Rightarrow R_0 = 526.3k\Omega \| (144.5 + 416.7)k\Omega$

$\Rightarrow R_0 = 526.3k\Omega \| 560.8k\Omega = \boxed{271.5k\Omega}$

d) If body effect were included, then $g_{mb_3} V_{bs_3}$ will appear in $\|^l$ with $g_{m_3} V_{gs_3}$, also $g_{mb_2} V_{bs_2}$ will appear in parallel with $g_{m_2} V_{gs_2}$, but M_1 will be immune of body effect. Thus, g_{mb_2} & g_{m_2} as well as g_{mb_3} & g_{m_3} will come in parallel, increasing the conductance, & reducing the resistance ⇒ thus, R_0 will drop a bit from the value calculated in c).