EE210: Microelectronics-I

L37 : MOSFET-1

http://youtu.be/GgPefhL53Ok

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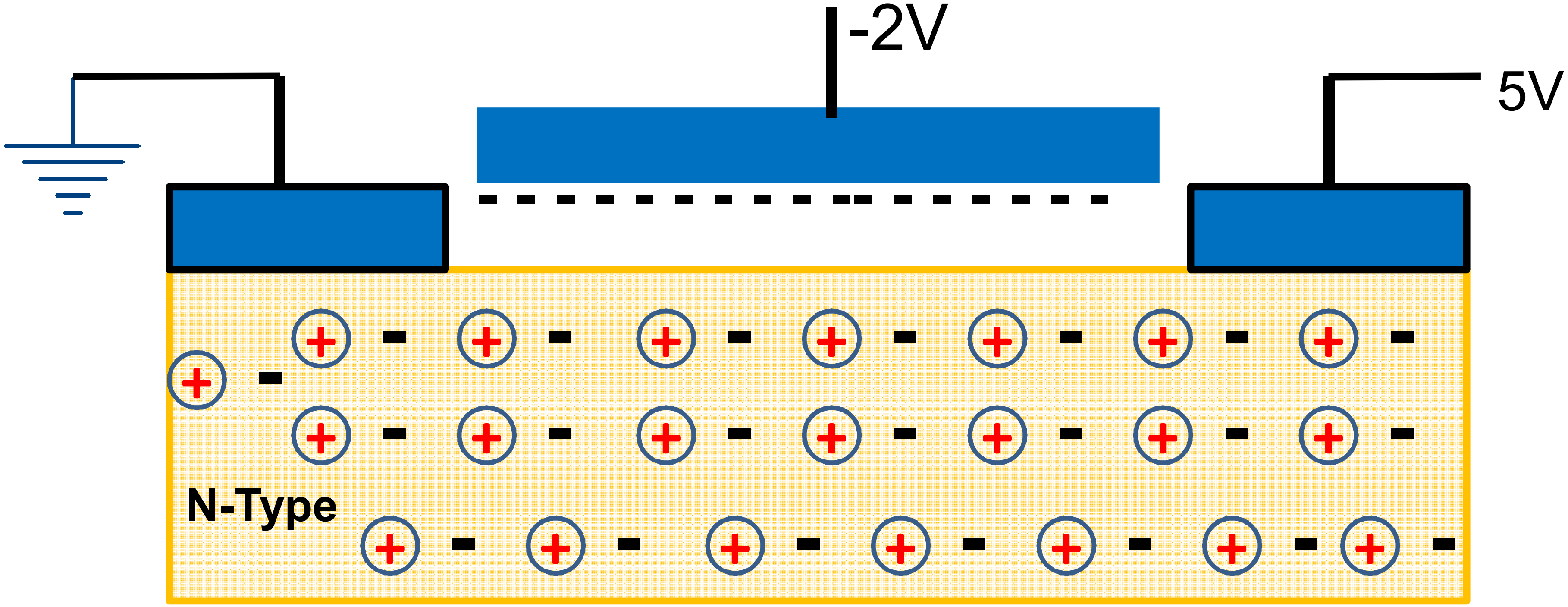
Transistor

Current I_O is much more sensitive to V_{IN} than V_O

$$\frac{\partial I_O}{\partial V_{in}} >> \frac{\partial I_O}{\partial V_o}$$

Field Effect Principle

$$\frac{\partial I_O}{\partial V_{in}} >> \frac{\partial I_O}{\partial V_o}$$



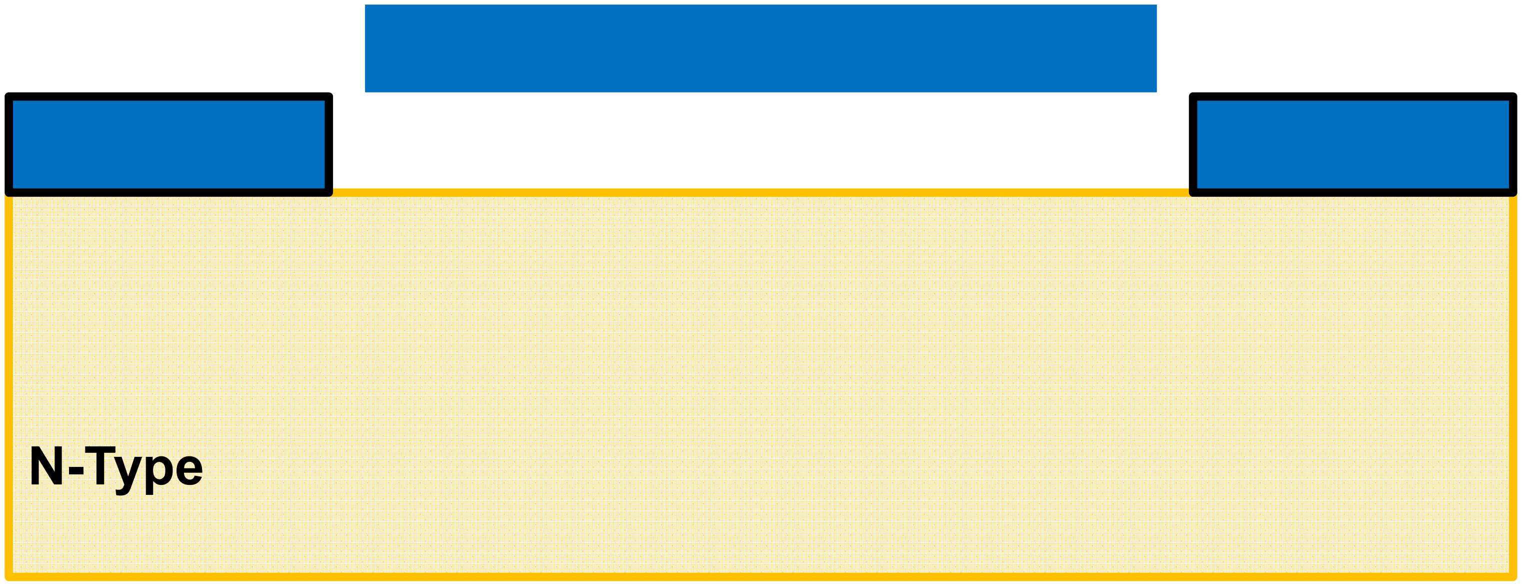
Modulation of conductivity using electric field

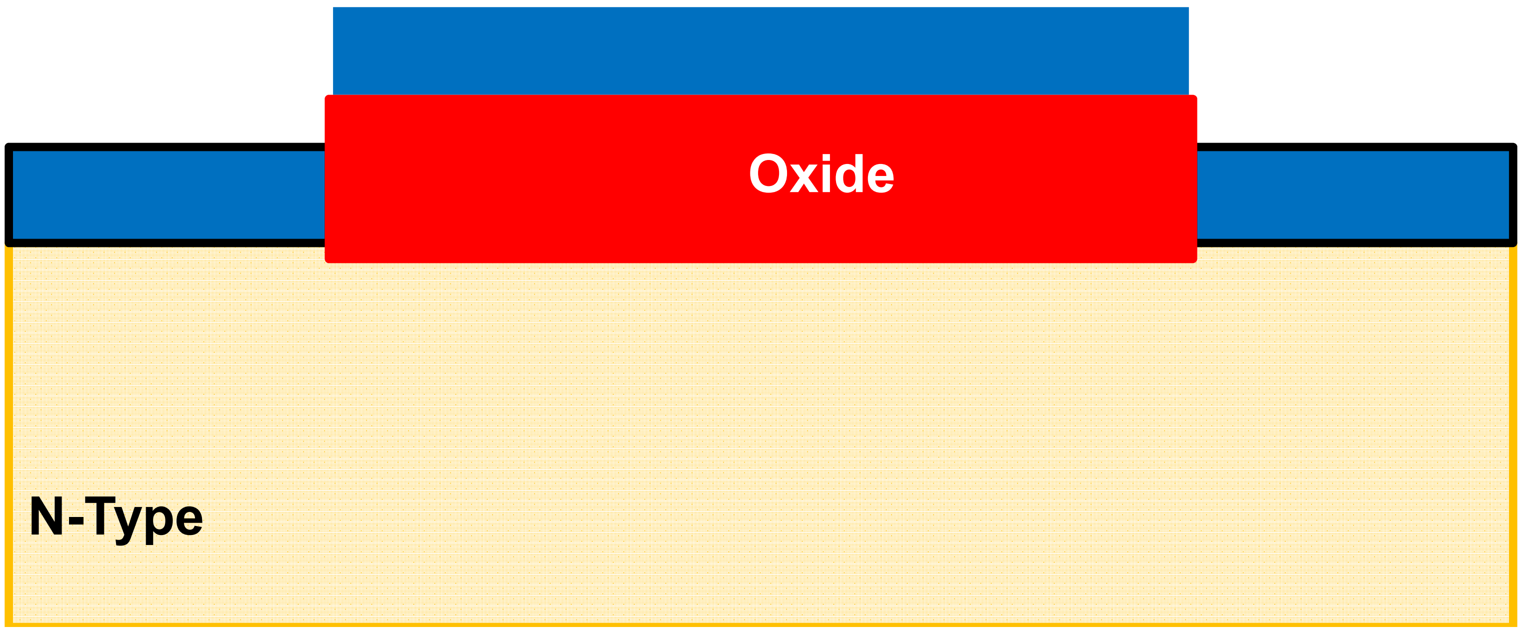
Transconductance

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

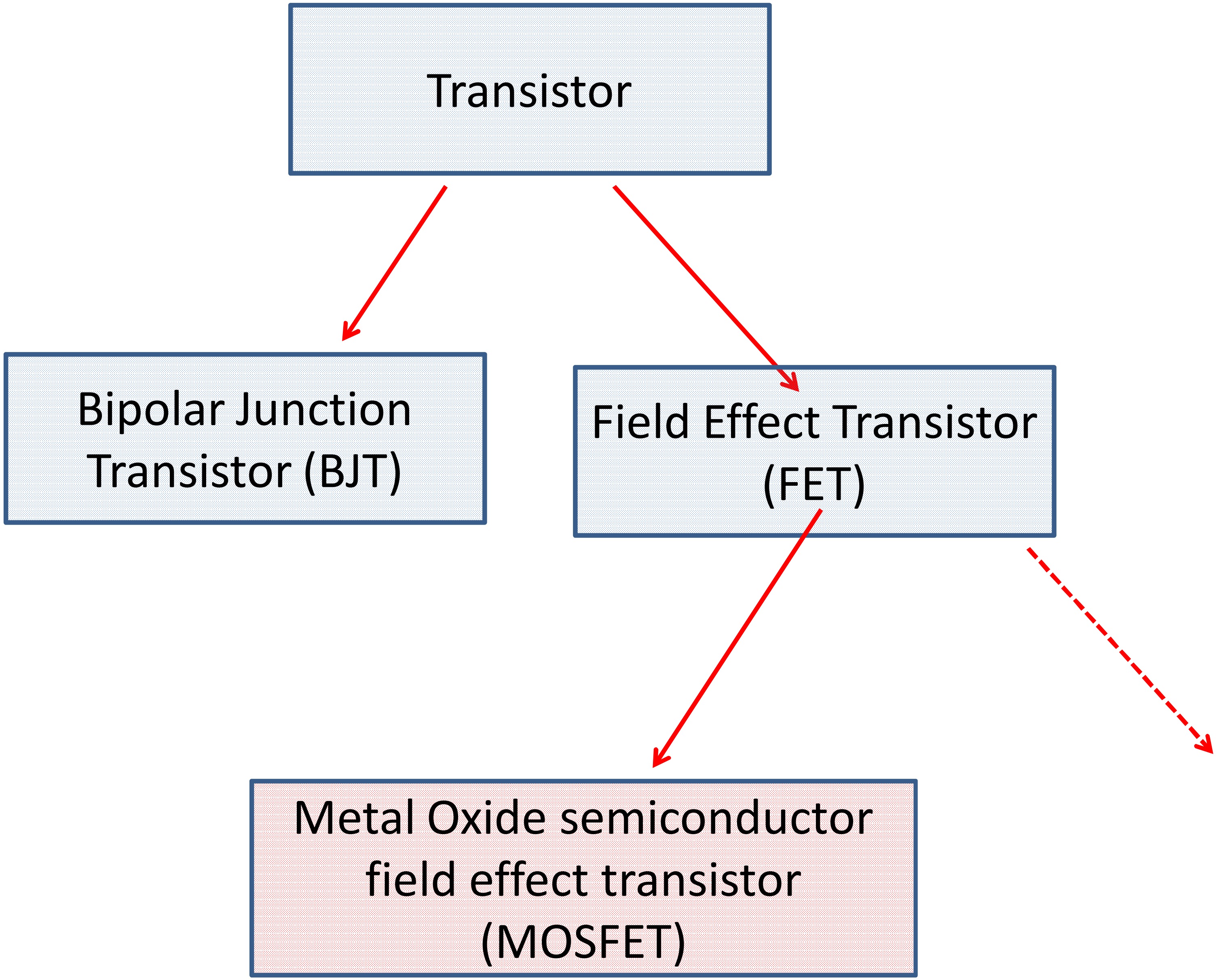
Filed Oct. 8, 1926

The invention relates to a method of and apparatus for controlling the flow of an electric current between two terminals of an electrically conducting solid by establishing a third potential between said terminals; and is particularly adaptable to the amplification of oscillating currents such as prevail, for example, in radio communication. Heretofore, thermionic tubes or valves have been generally employed for this purpose; and the present invention has for its object to dispense entirely with devices relying upon the transmission of electrons thru an evacuated space and especially to devices of this character wherein the electrons are given off from an incandescent filament. The invention has for a further object a simple, substantial and inexpensive relay or amplifier not involving the use of excessive voltages, and

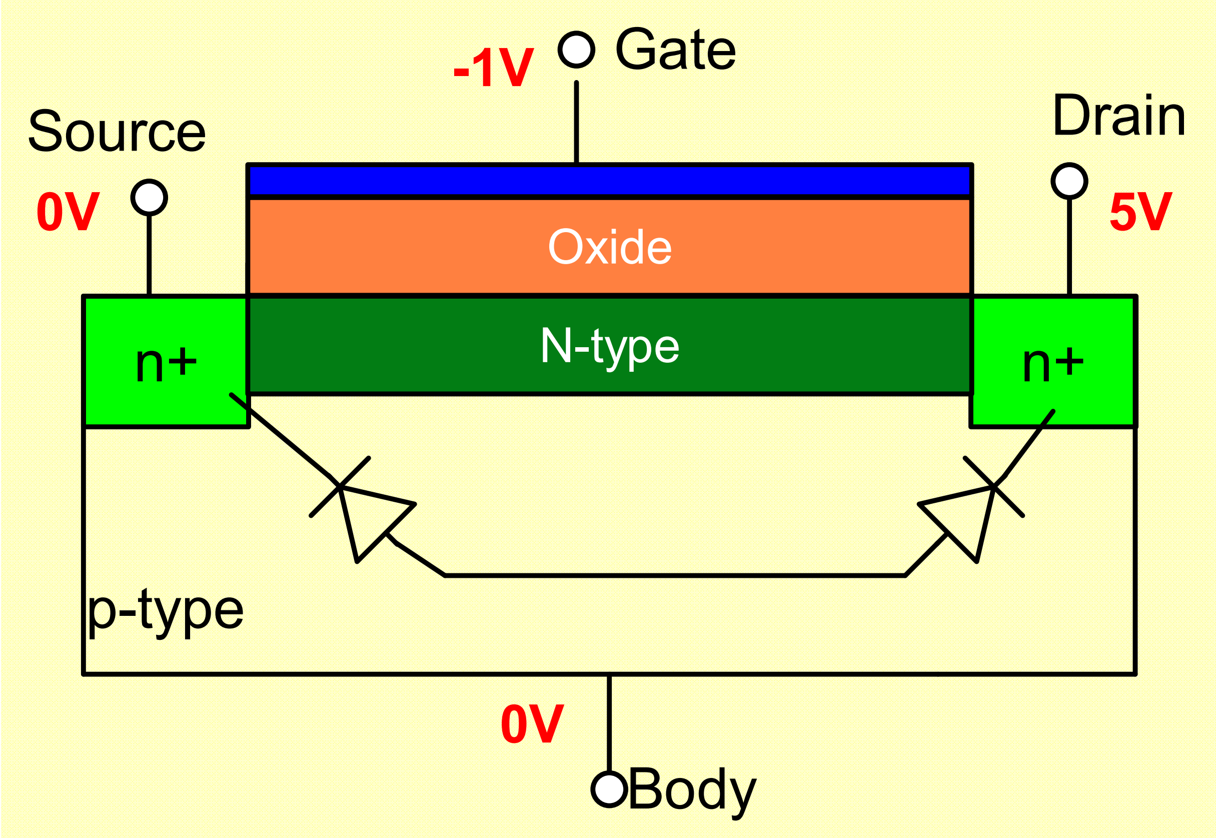

N-Type


Oxide
N-Type

Transistors



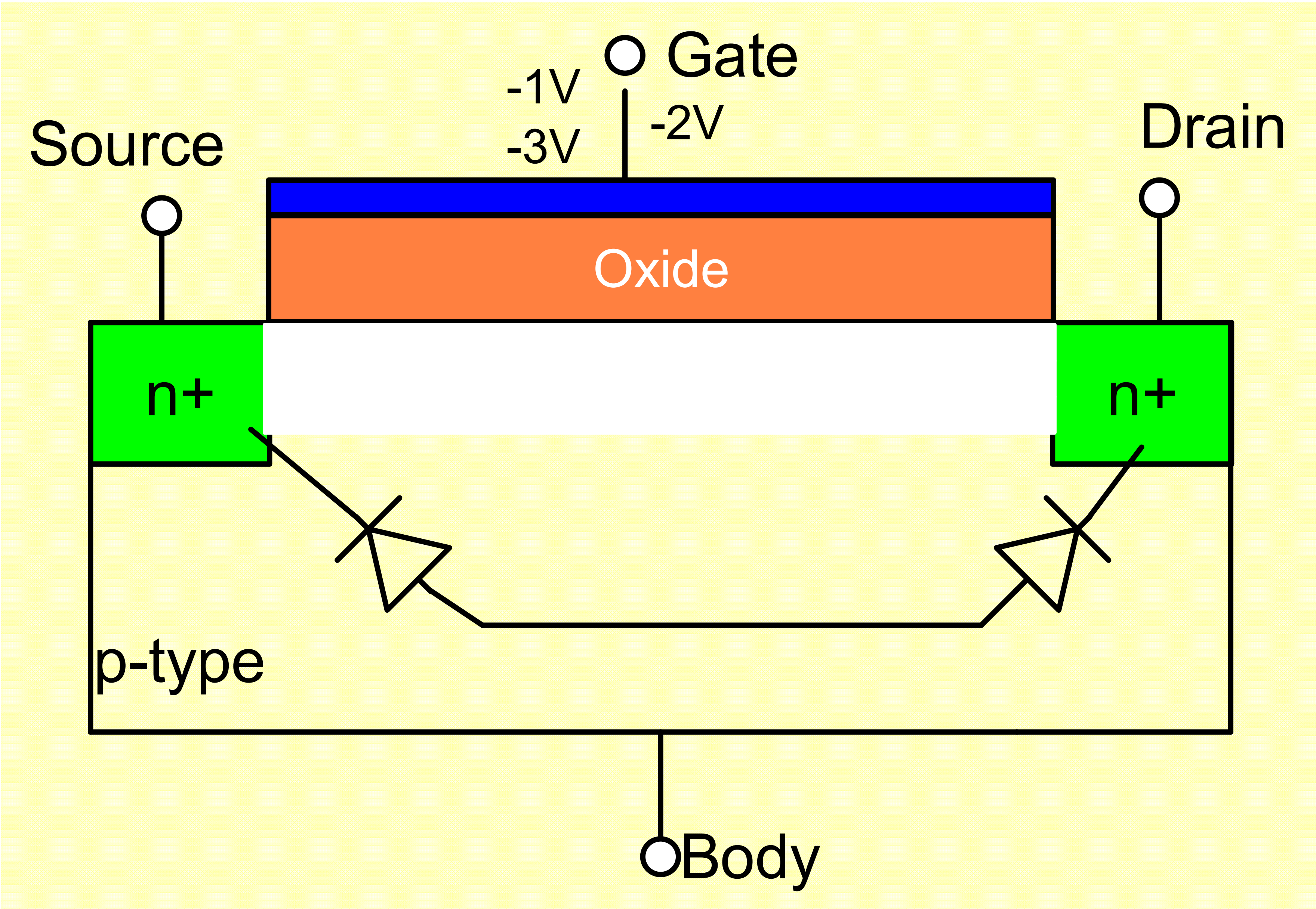
Depletion-Mode Transistor



In a depletion-mode transistor, a channel exists without any gate voltage being applied and current flows when drain voltage is applied.

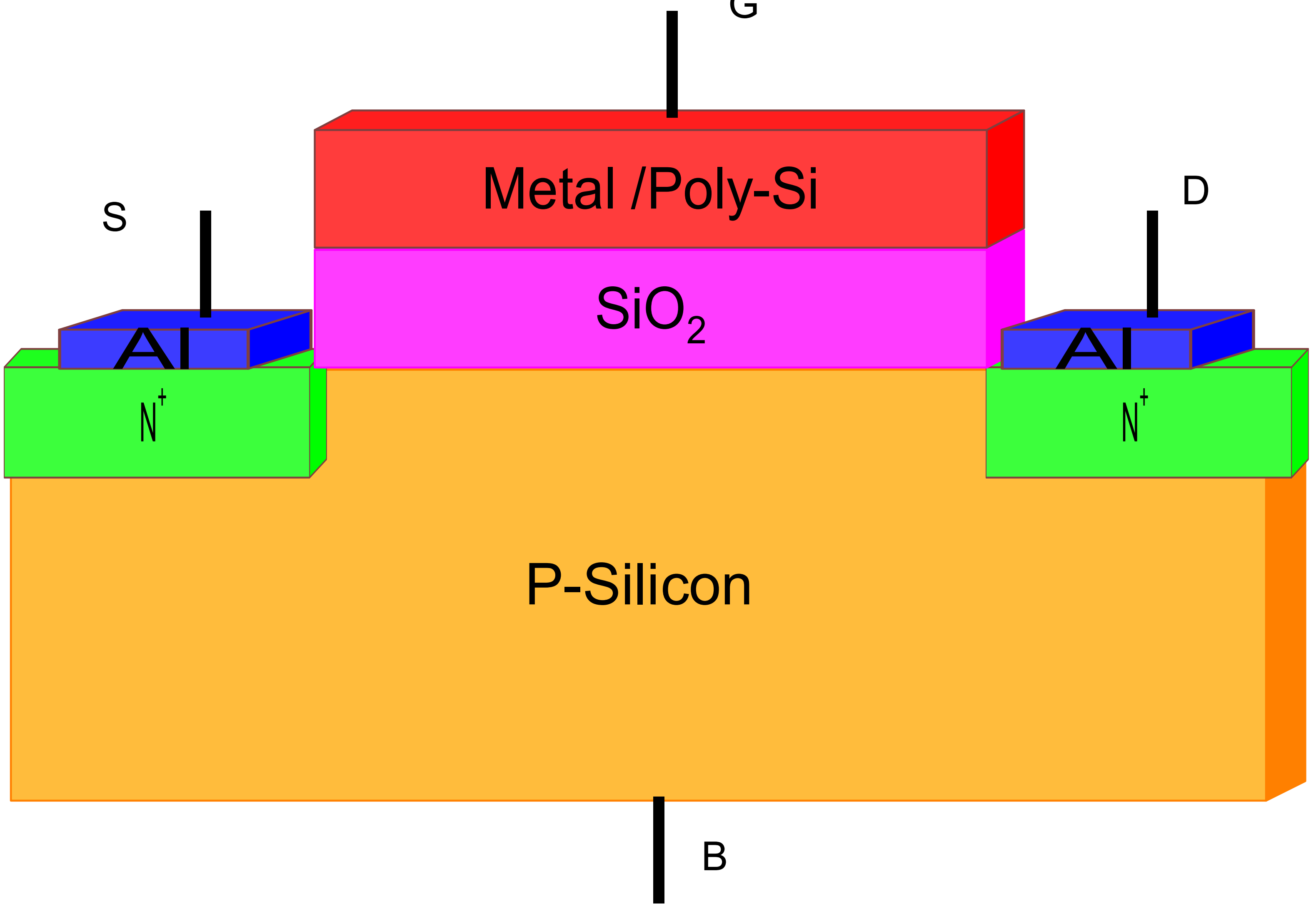
Negative gate voltage is applied to deplete the channel of carriers and cause current to reduce.

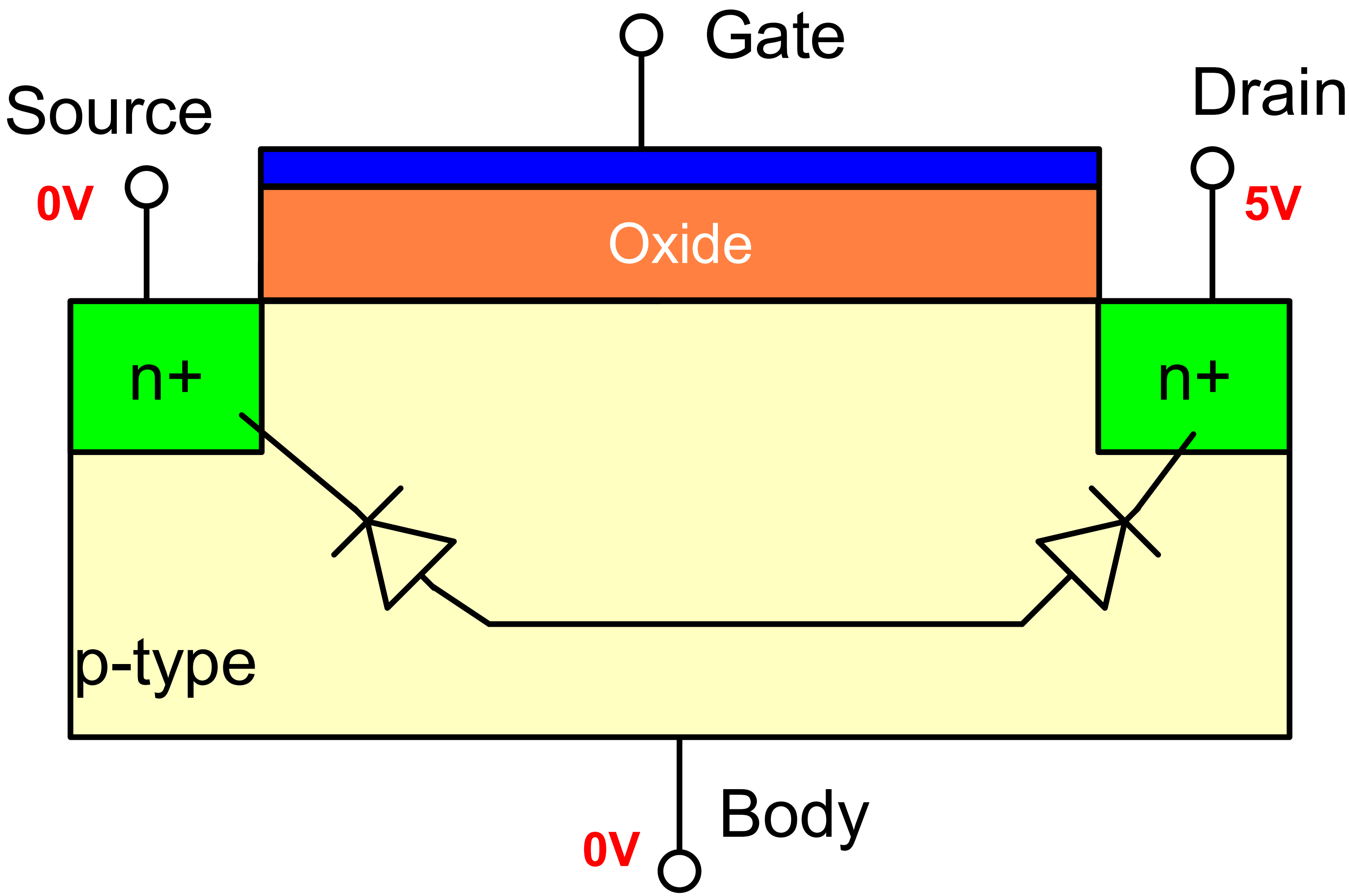
Channel exists at zero gate voltage and is depleted by gate voltage



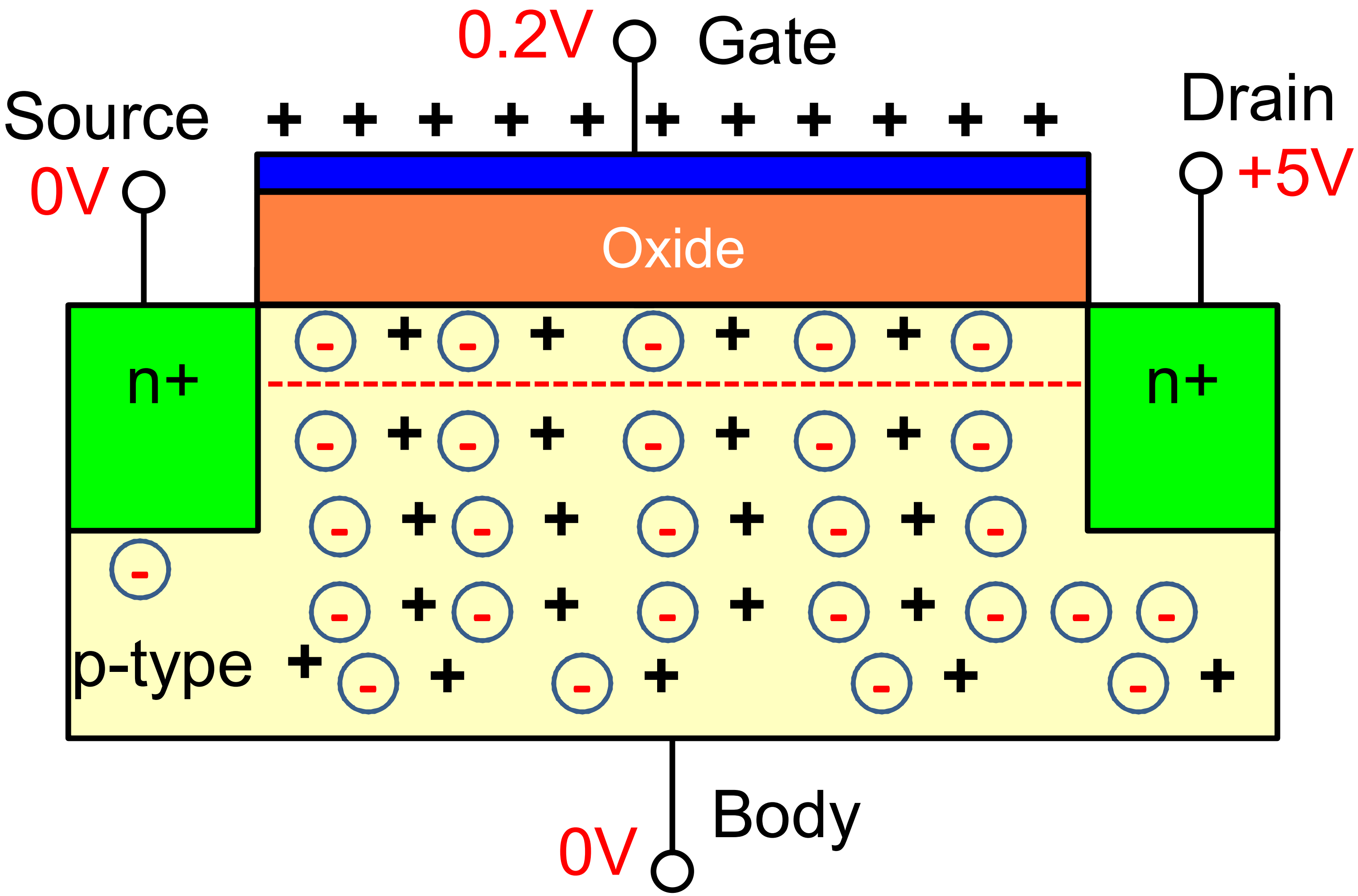
Channel is completely pinched off and current ~zero

NMOS Enhancement mode transistor: Inversion Mode Transistor

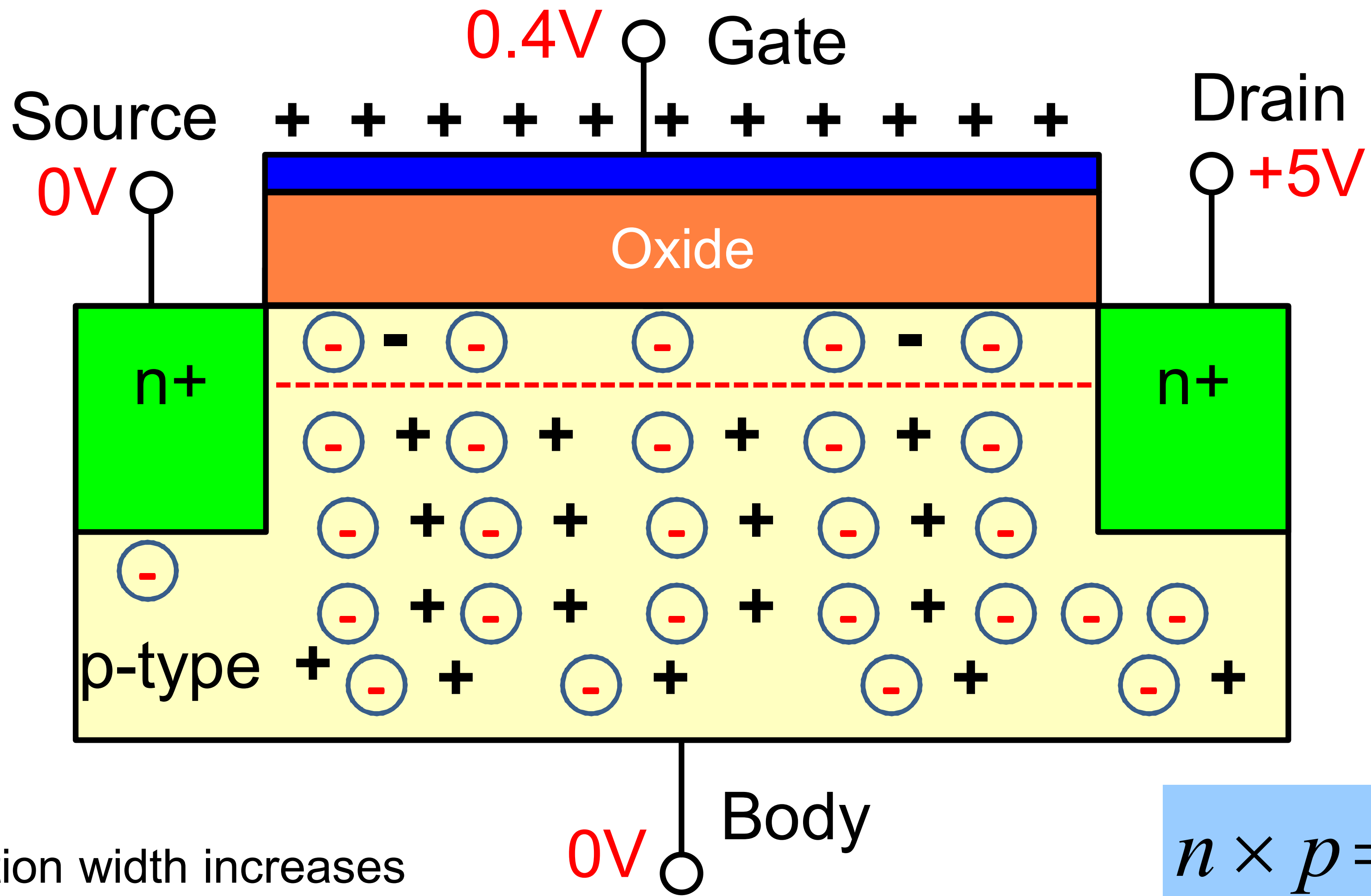




No channel exists when gate voltage is zero and current is zero as well.



Depletion Region is formed near the Si/SiO_2 interface

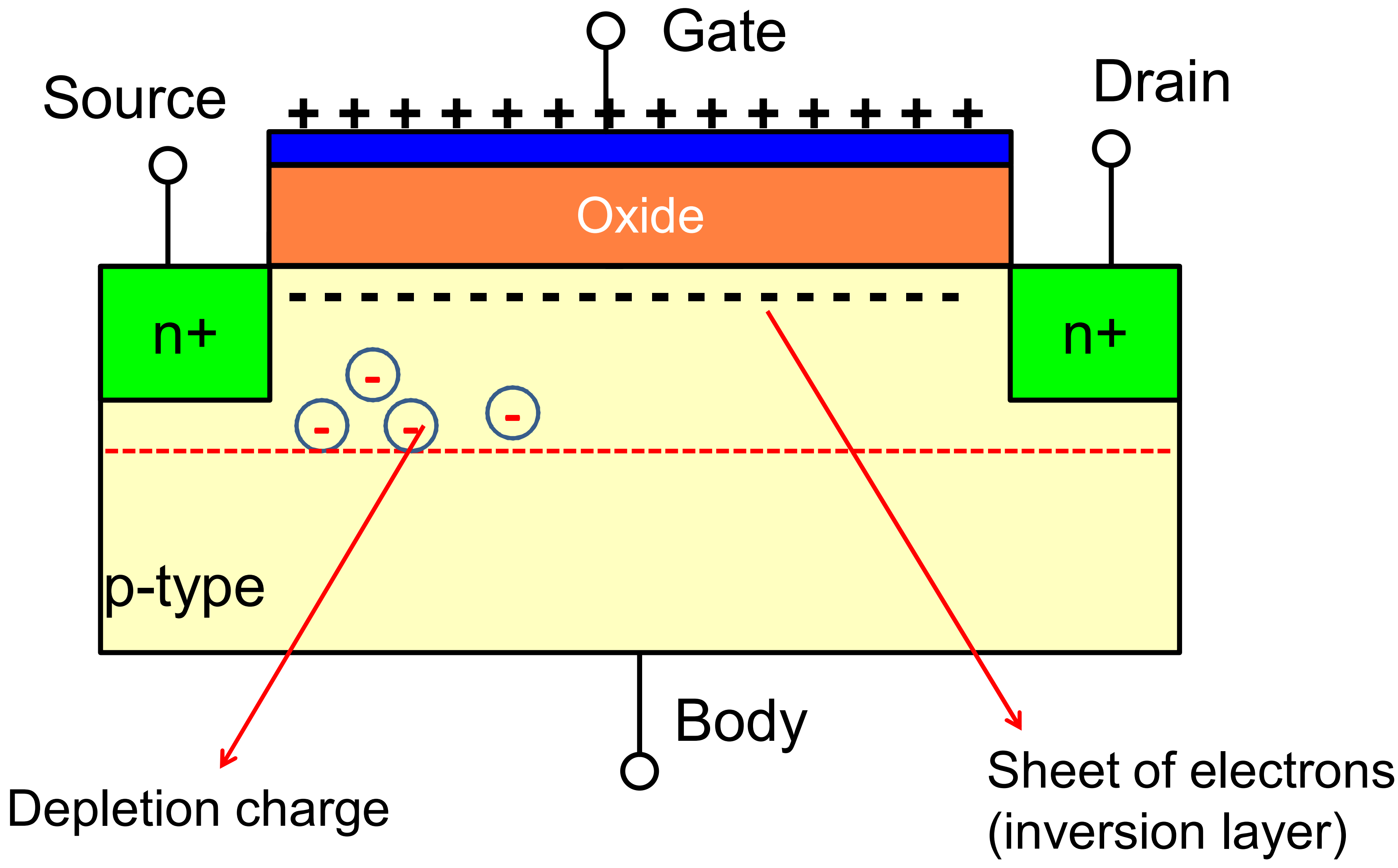


$$n \times p = n_i^2$$

Depletion width increases

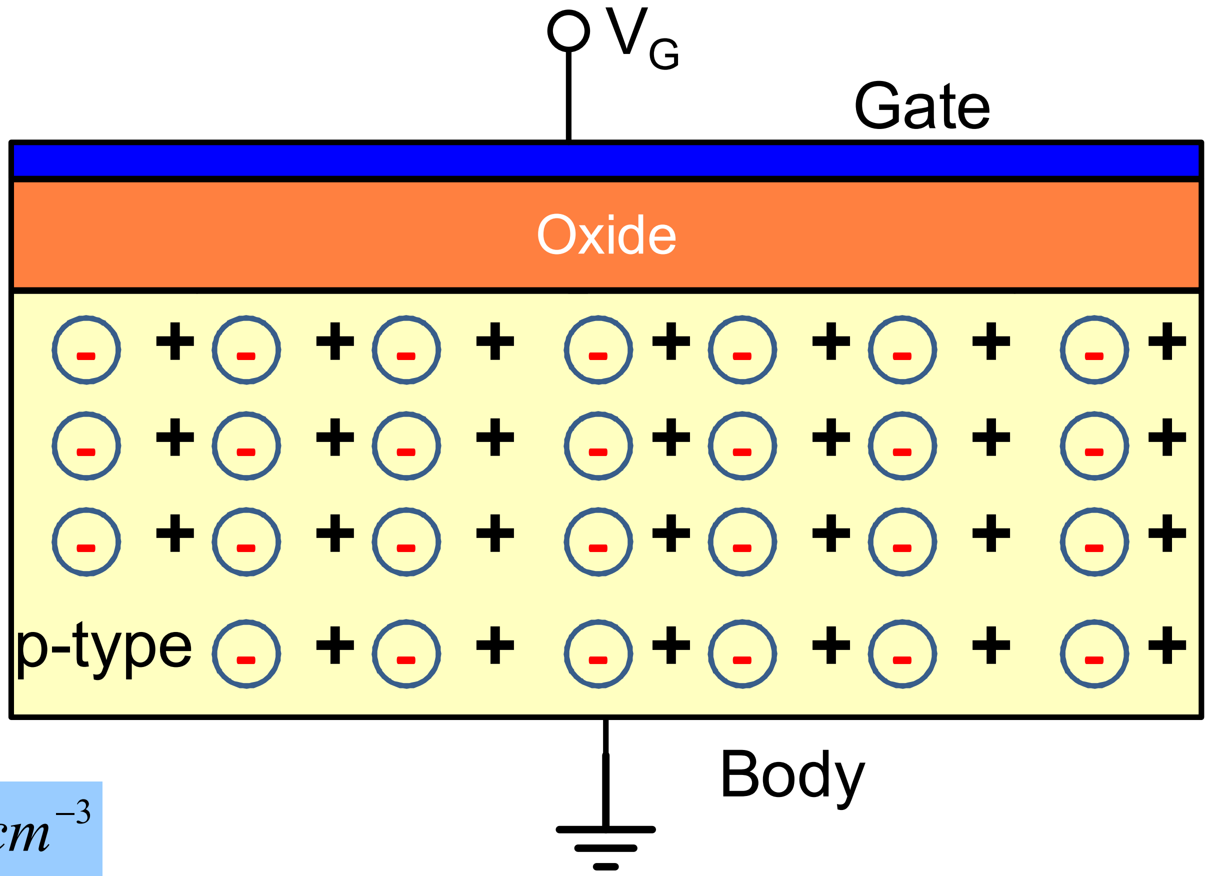
But something interesting happens: electron density at the surface also increases

At a sufficiently large voltage ($>V_{THN}$) a channel of electrons forms at the Si/SiO2 interface.



Conductivity modulation at the surface?

MOS capacitor constitutes the heart of a MOSFET

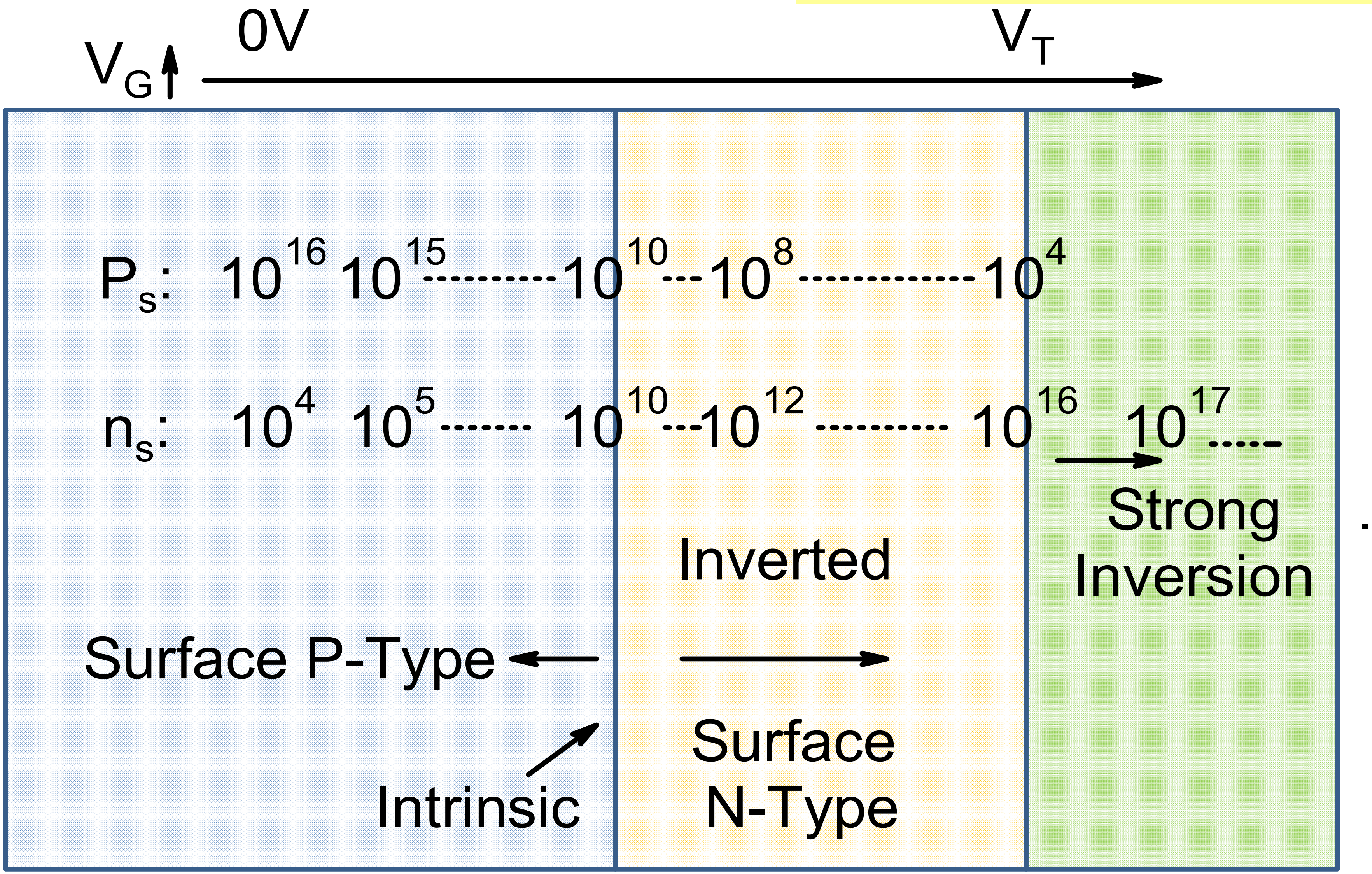


$$p = N_A = 10^{16}\,cm^{-3}$$

$$n = \frac{n_i^2}{N_A} \cong 10^4\,cm^{-3}$$

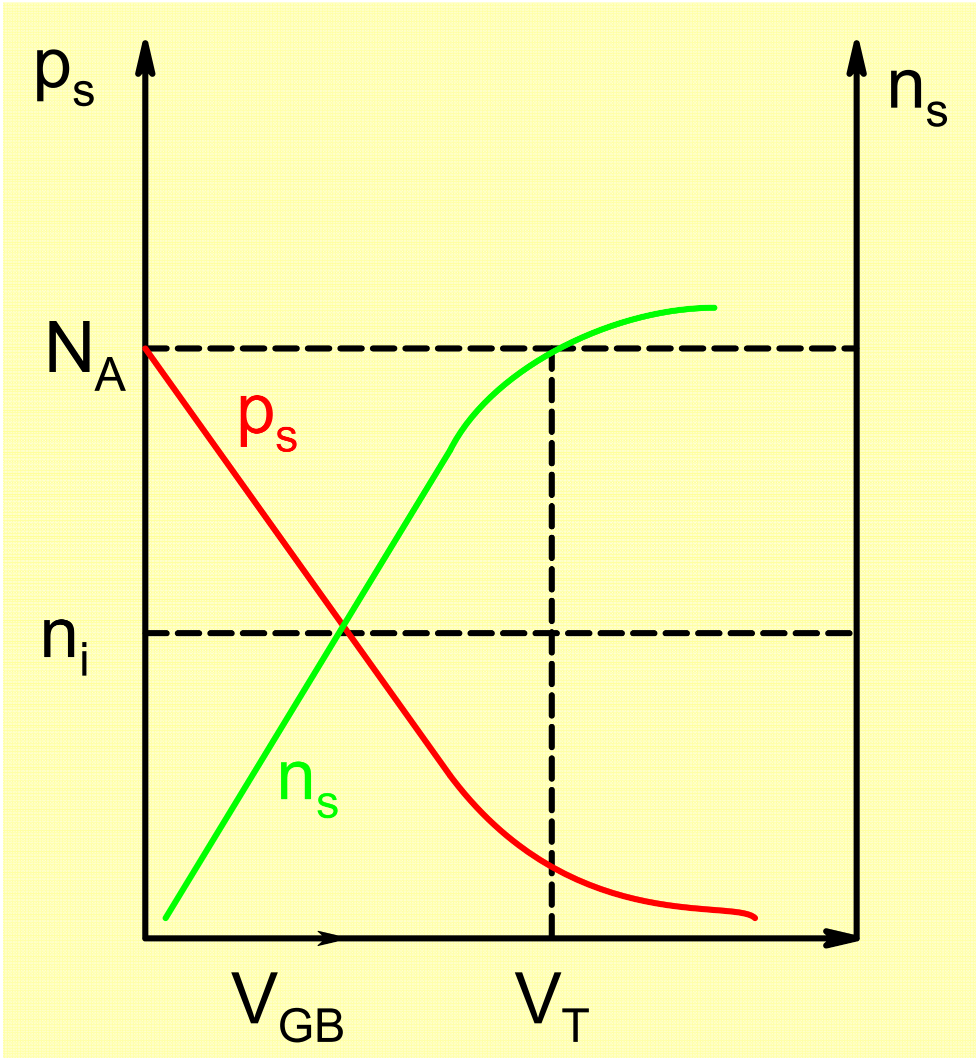
Field Effect…

$$n_s \times p_s = n_1^{\ 2} \cong 10^{20}\, cm^{-3}$$



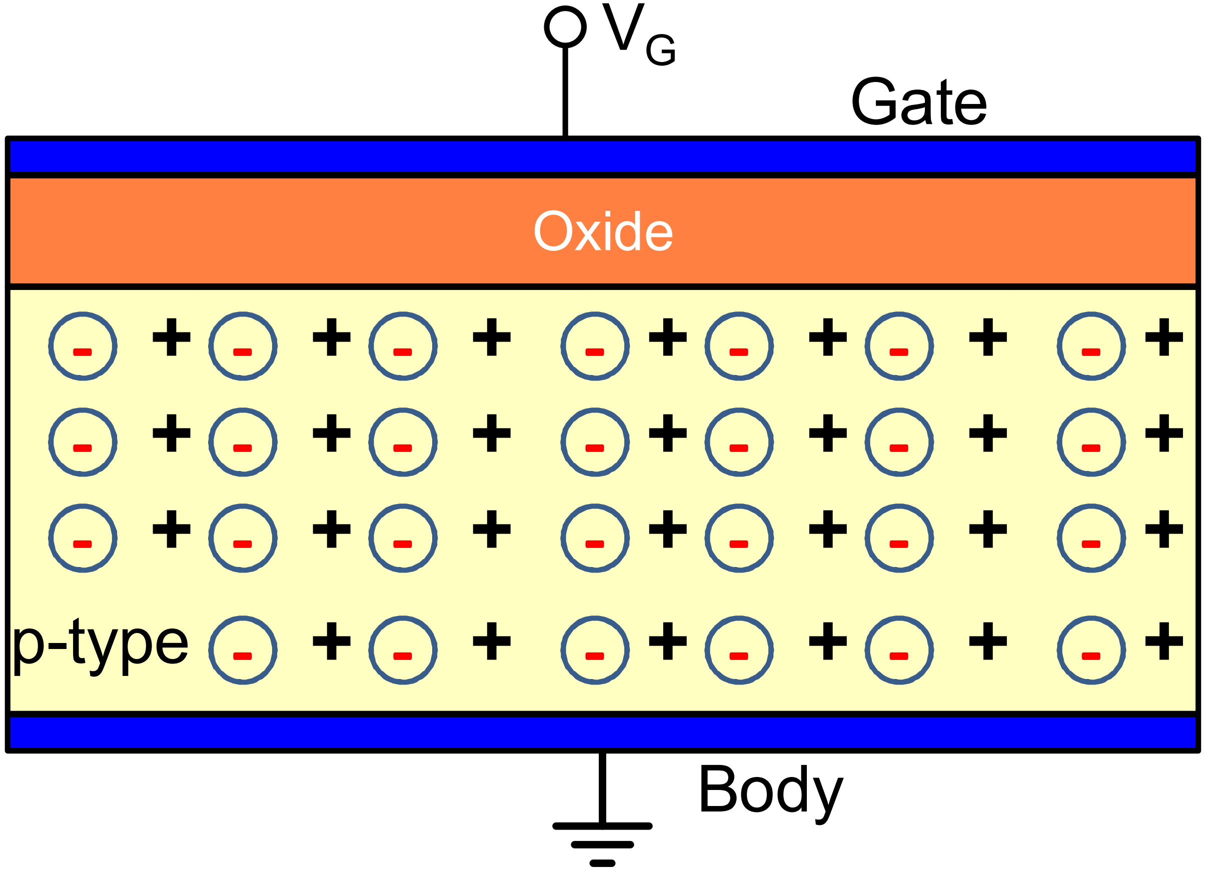
Surface carrier density can be changed from P-type to N-type

Surface Carrier Density



Flat band condition

$$V_G = V_{FB}$$

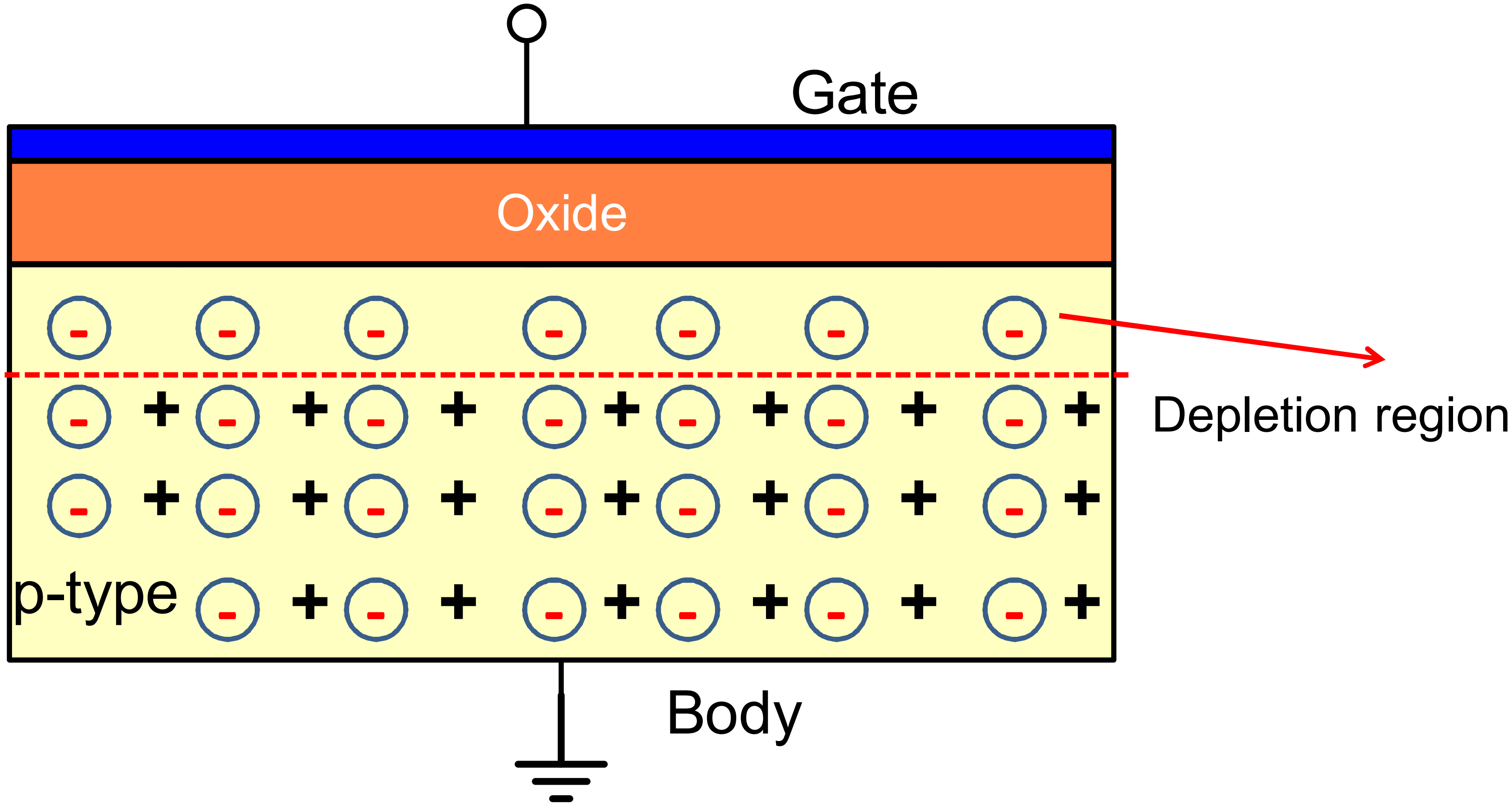


Whenever two different material are brought into contact, an internal potential difference develops like in a pn junction. Thus even when no gate voltage is applied, there is a voltage across the mos capacitor.

$V_G = V_{FB}$; Flat-band condition meaning no NET voltage across the capacitor. Uniform hole density everywhere

Depletion

$$V_G > V_{FB} \text{ but } V_G < V_{THN}$$

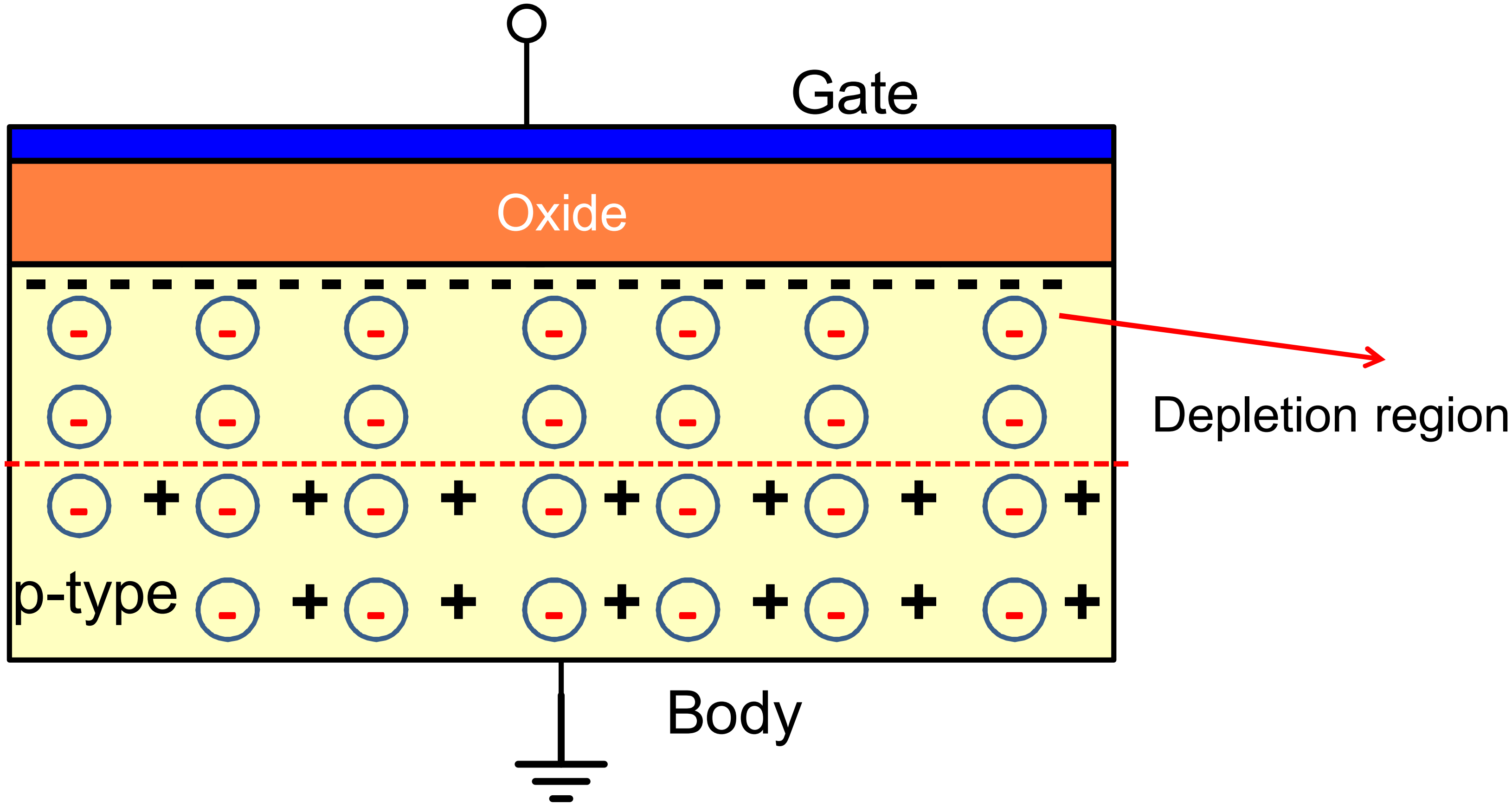


Holes are depleted from the surface $p_S < p_B$

Although $n_S > n_B$ electron density is also very small

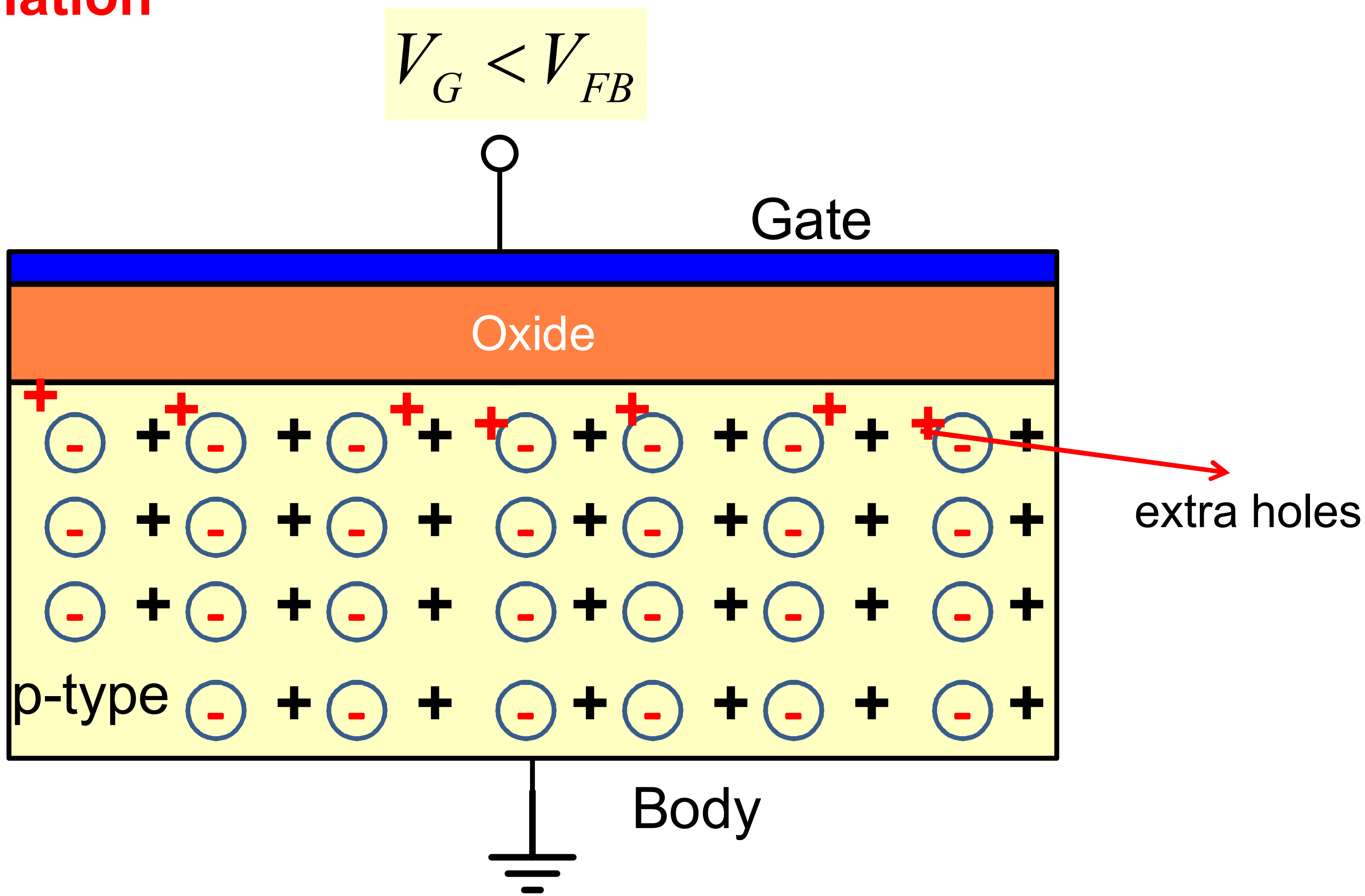
Strong Inversion

$$V_G > V_{THN}$$



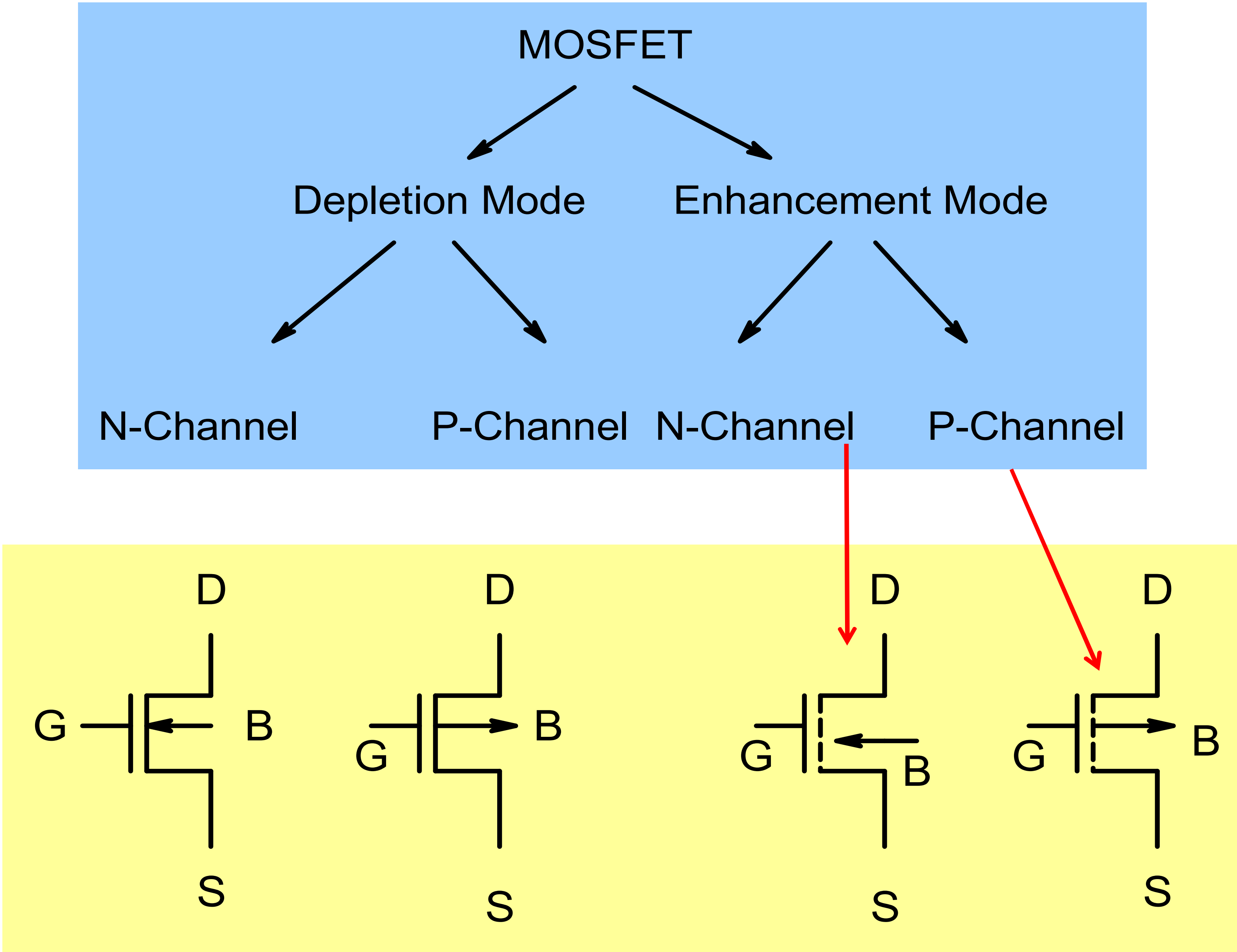
Electrons are accumulated at the surface $n_S >> N_A$

Accumulation

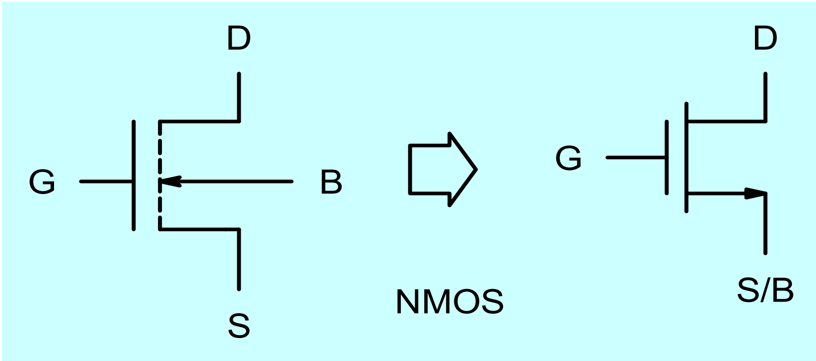


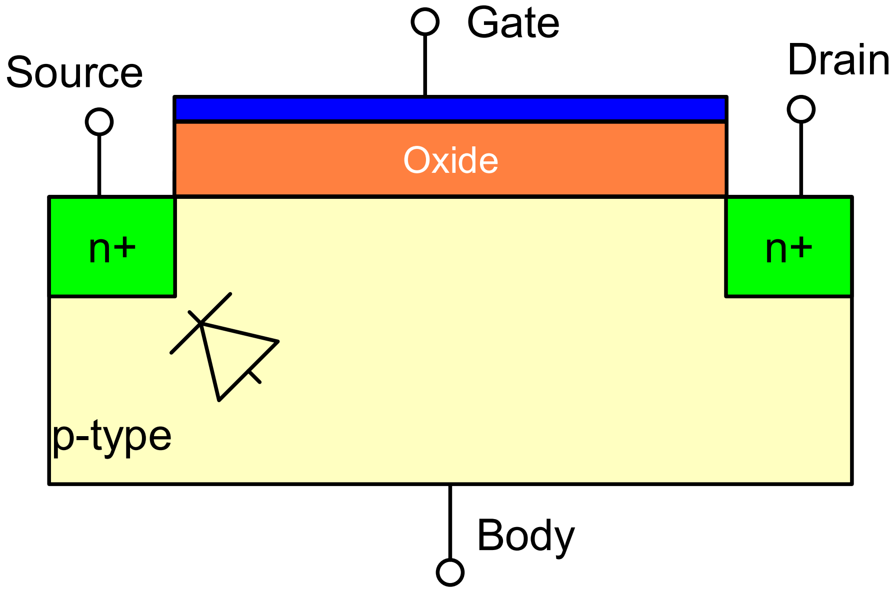
Holes are accumulated at the surface $p_S > p_B$

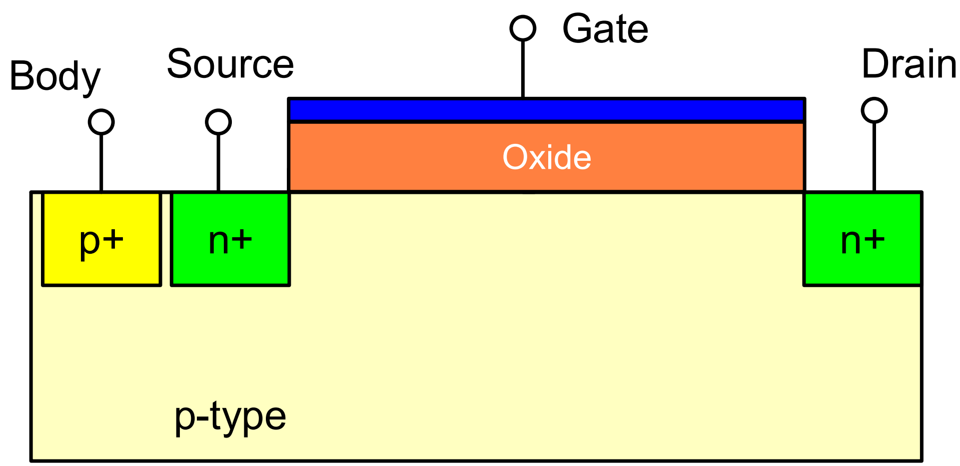
Metal Oxide Semiconductor Field Effect Transistor:



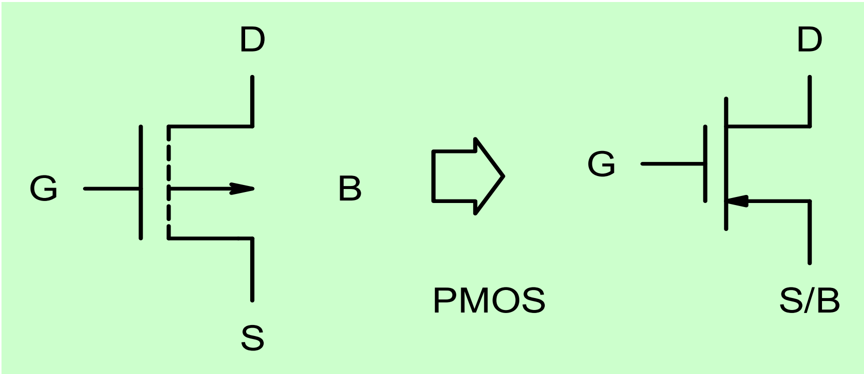
Simplified Symbols and structure

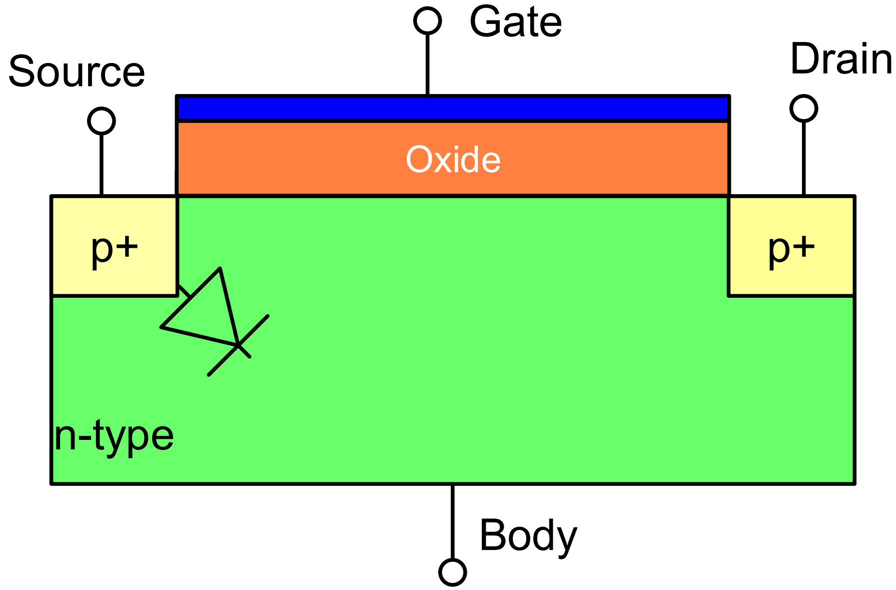


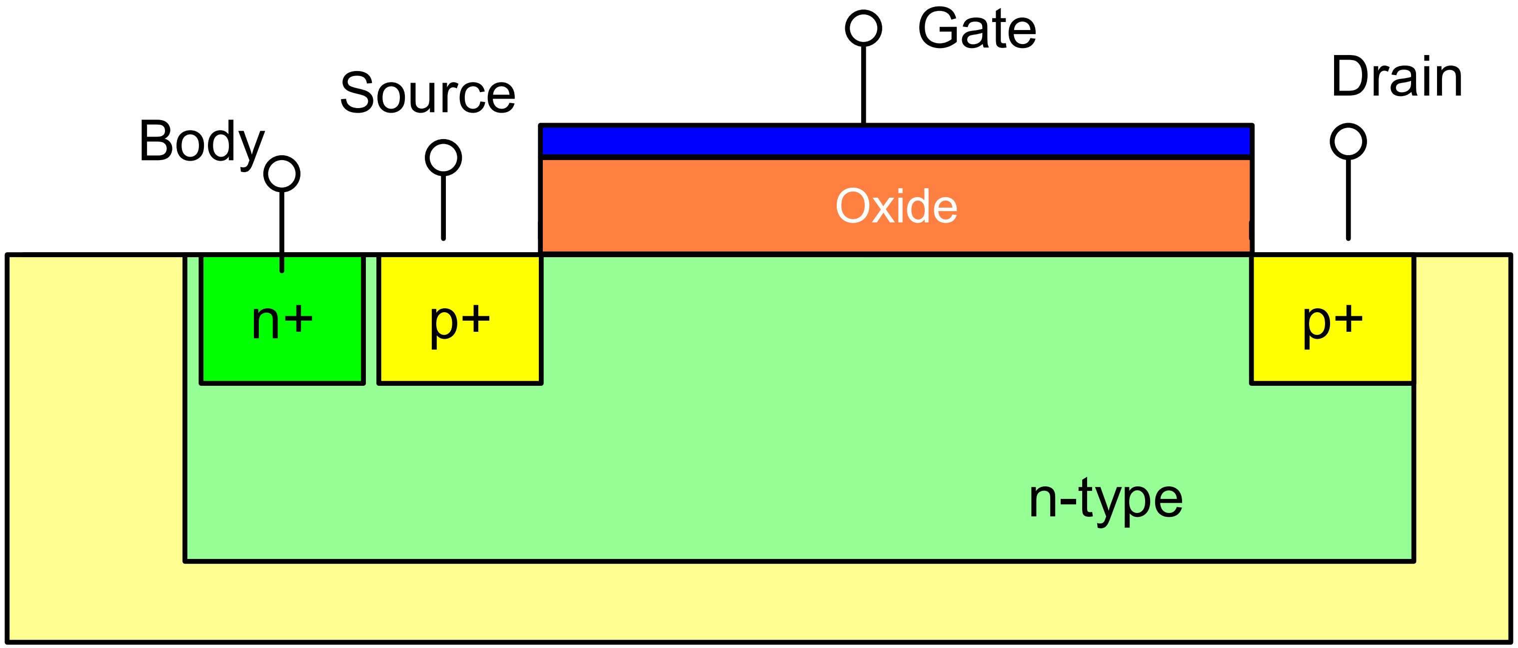


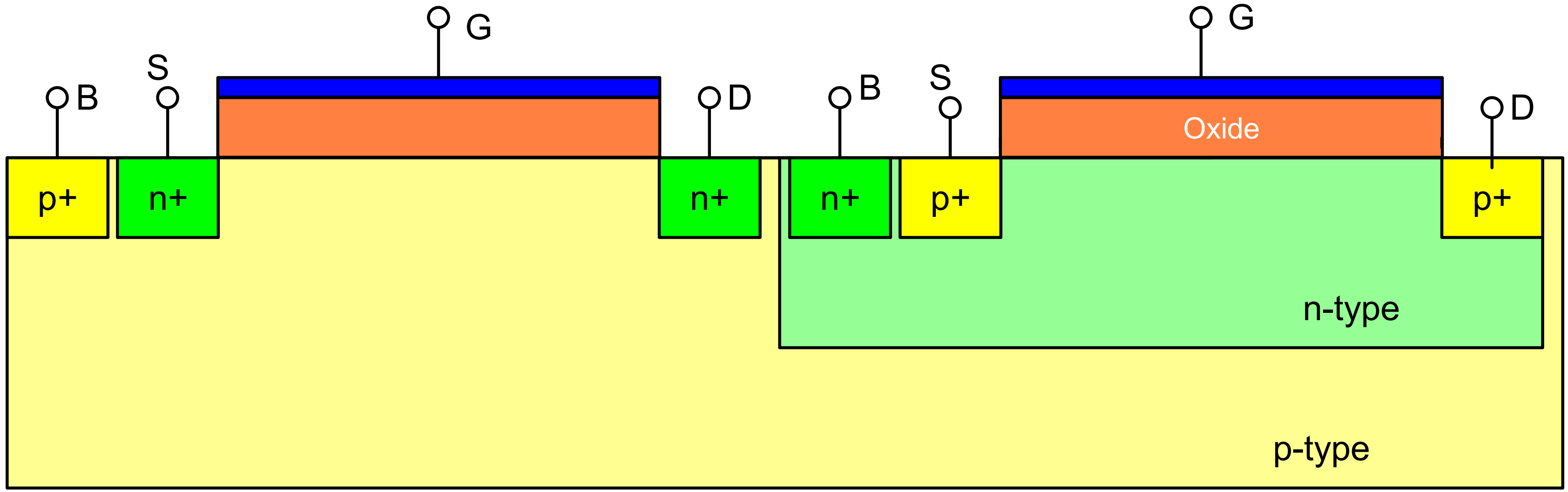


Simplified Symbols and structure



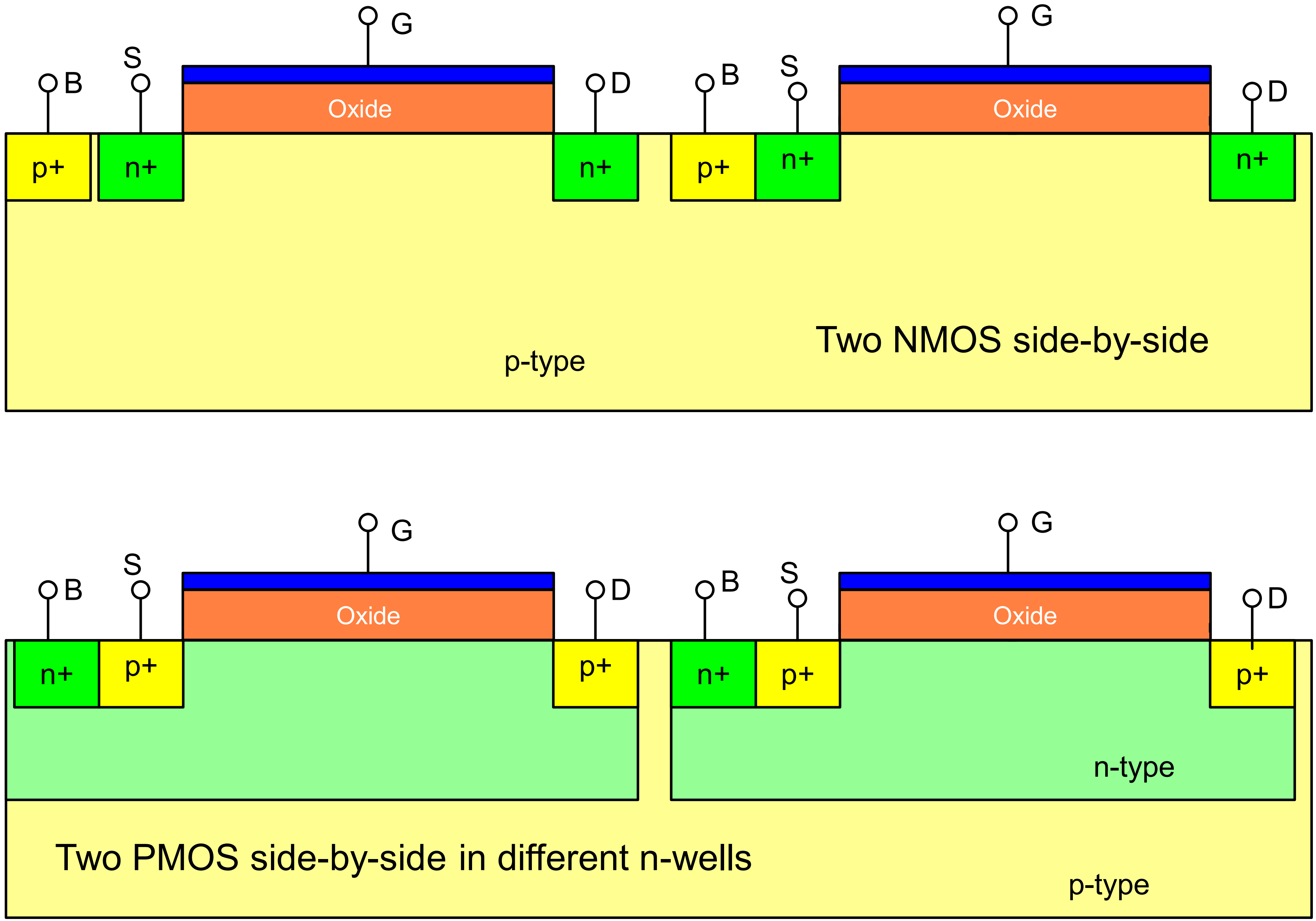






- Body potential of NMOS transistors is same and is normally connected to the most negative voltage in the circuit to ensure that VBS < 0 and thus body-source PN junction is reverse biased.

- Each PMOS can be fabricated in a separate individual N-well and thus each pmos body terminal can have a distinct voltage. Normally body and source terminals of PMOS are shorted together.


G
B
S
D
Oxide
p+
n+
n+
G
B
S
D
Oxide
p+
n+
n+
Two NMOS side-by-side
p-type
G
B
S
D
Oxide
n+
p+
p+
G
B
S
D
Oxide
n+
p+
p+
n-type
Two PMOS side-by-side in different n-wells
p-type

EE210: Microelectronics-I

Lecture-38 : MOSFET-2

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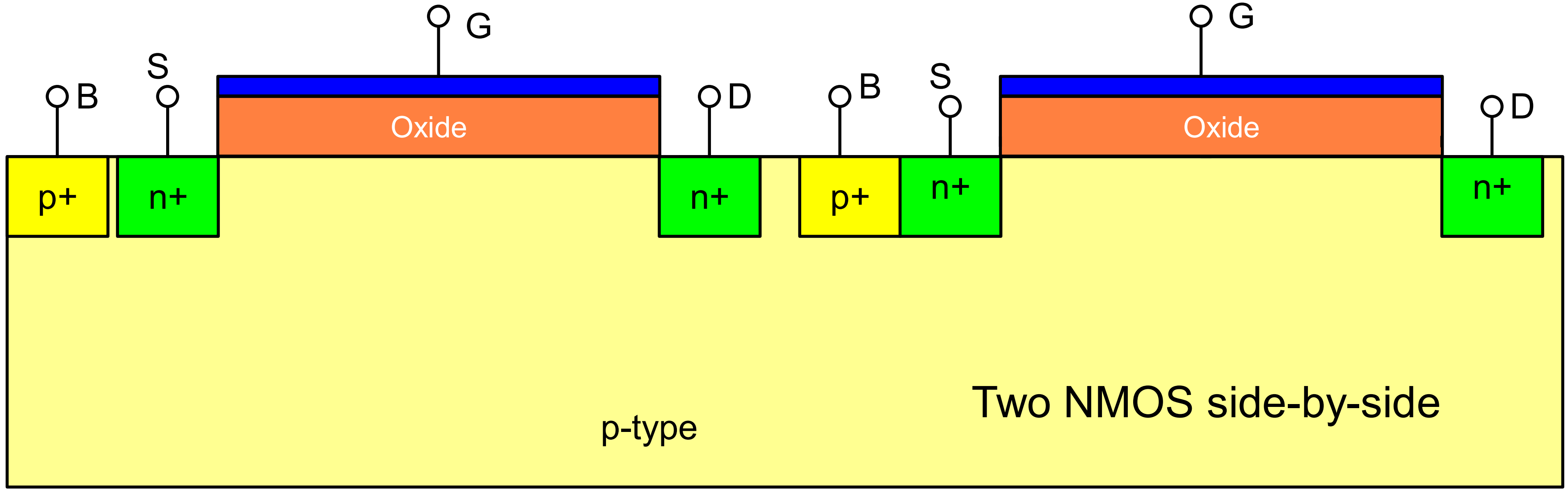
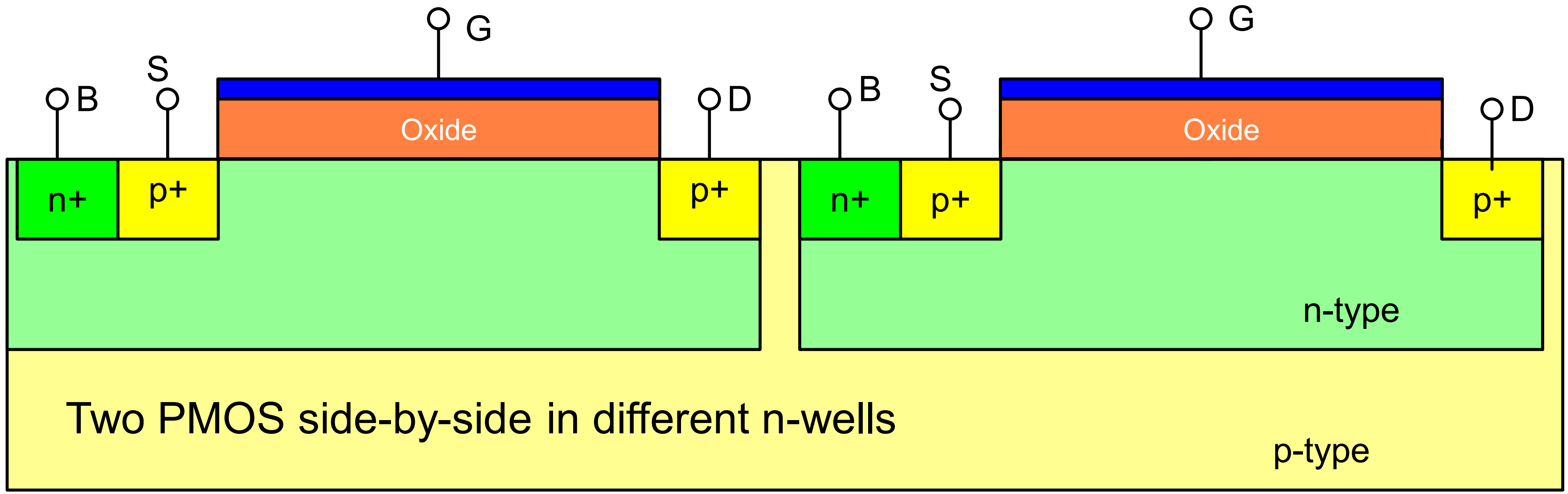
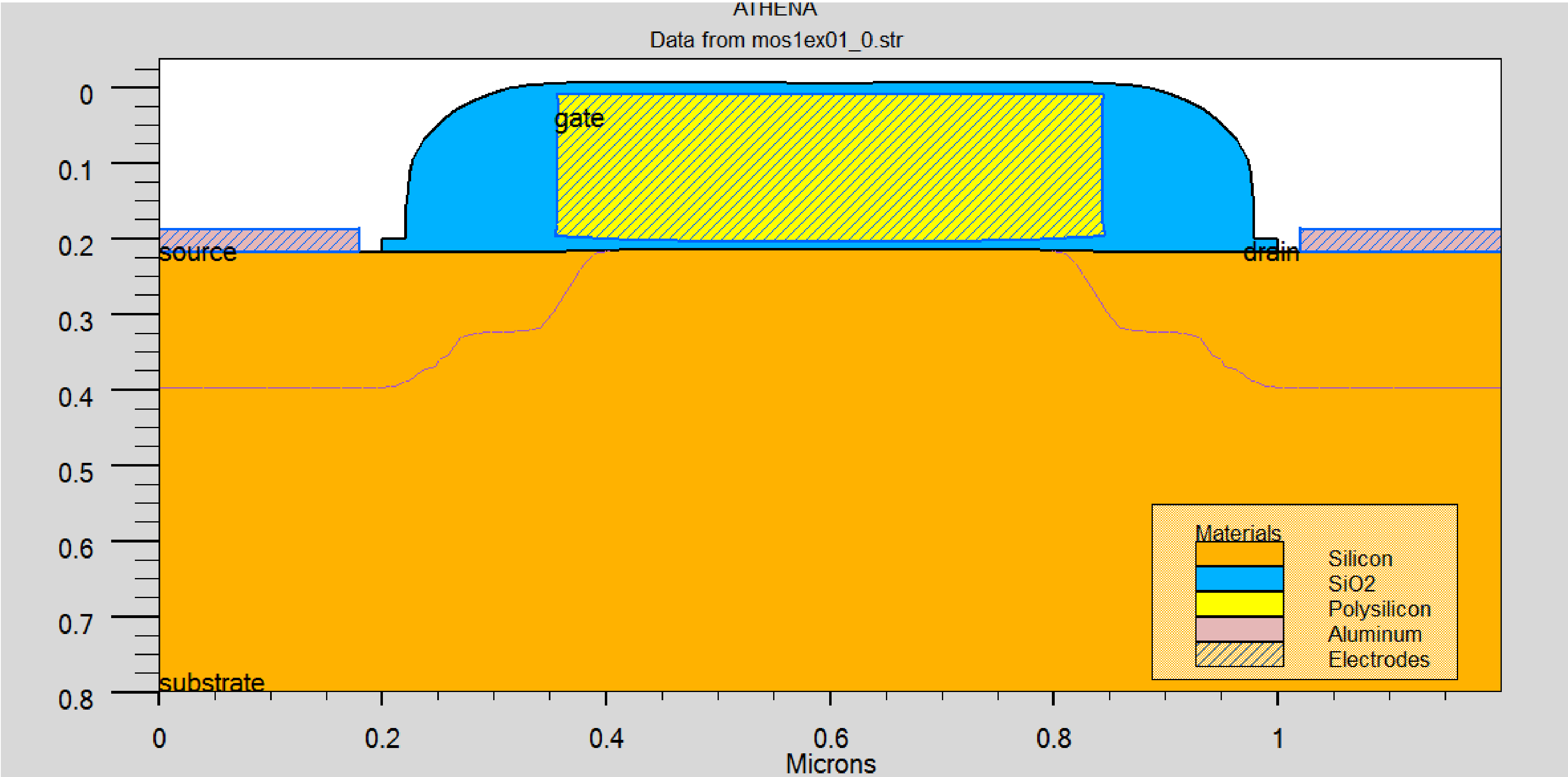
G-Number

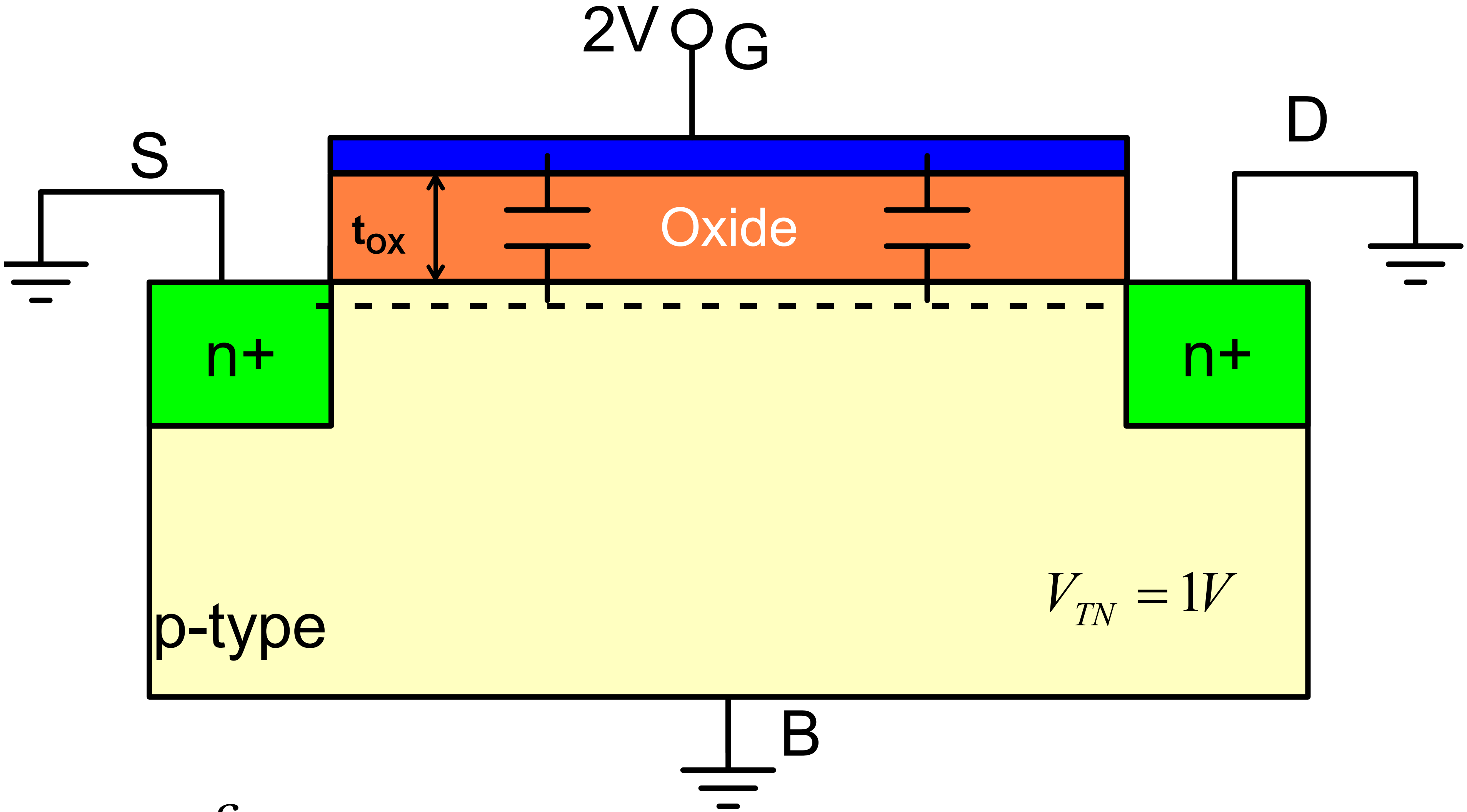

G
S
B
D
Oxide
p+
n+
n+
G
B
S
D
Oxide
p+
n+
n+
p-type
Two NMOS side-by-side


G
S
B
D
Oxide
n+
p+
p+
G
B
S
D
Oxide
n+
p+
p+
n-type
Two PMOS side-by-side in different n-wells
p-type



ATHENA
Data from mos1ex01_0.str
gate
source
drain
substrate
Materials
Silicon
SiO2
Polysilicon
Aluminum
Electrodes
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0
0.2
0.4
0.6
0.8
1
Microns

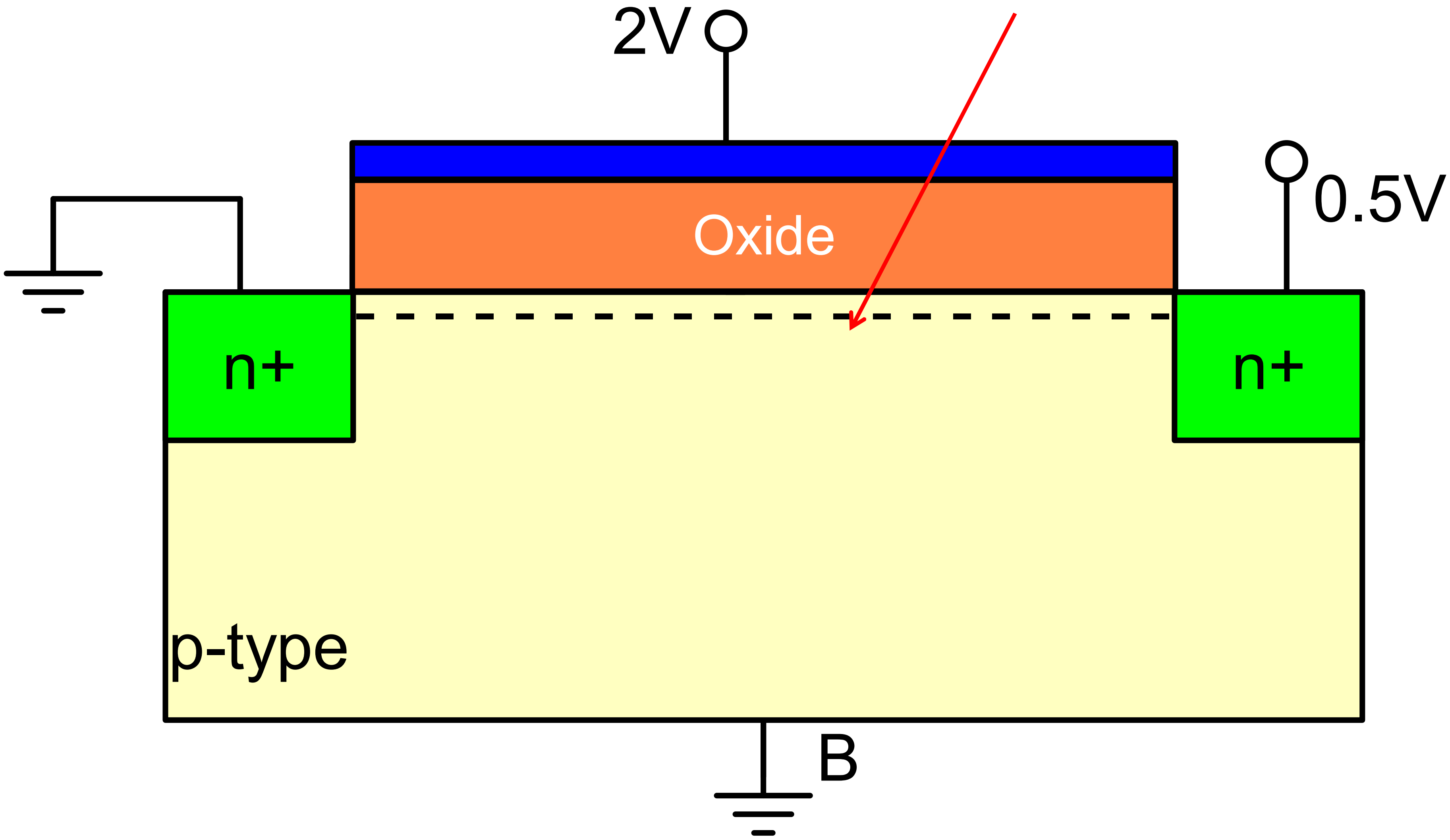
Operation of the MOSFET



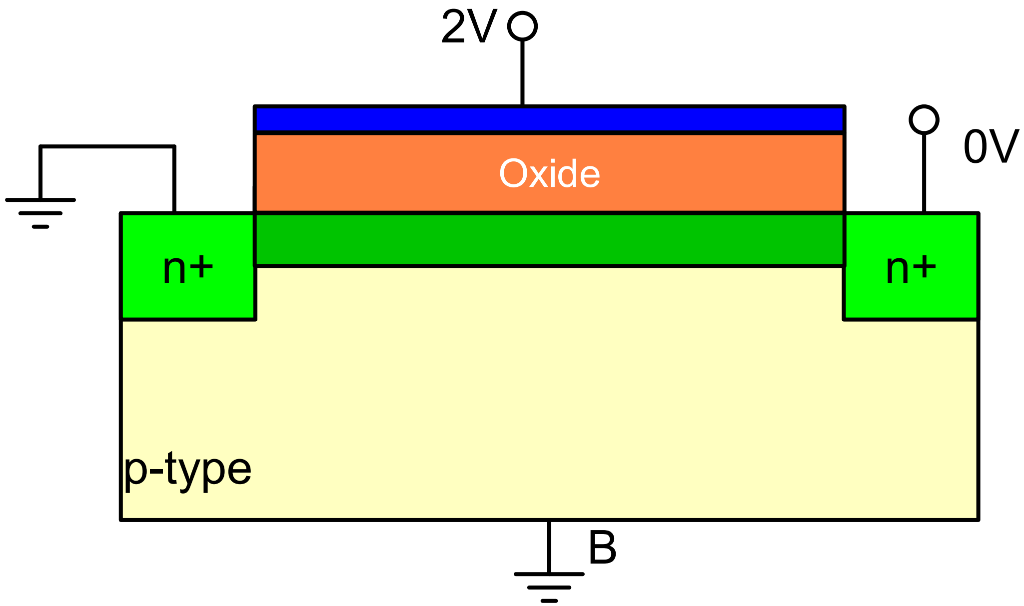
$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

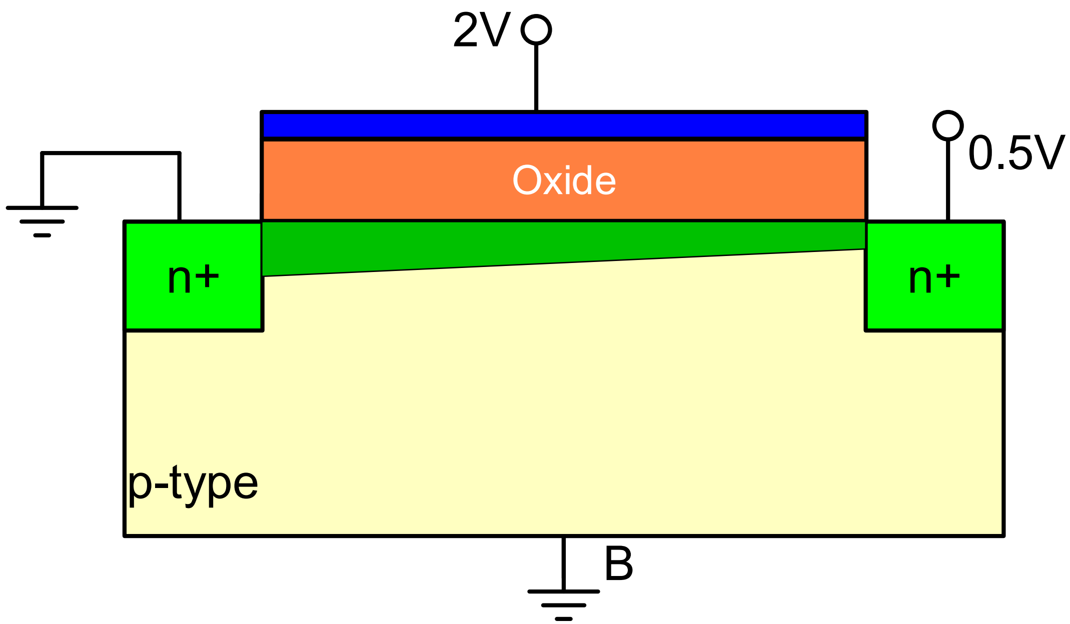
Inversion charge/area : $Q_{inv} = -C_{ox}(V_{GS} - V_{THN})$

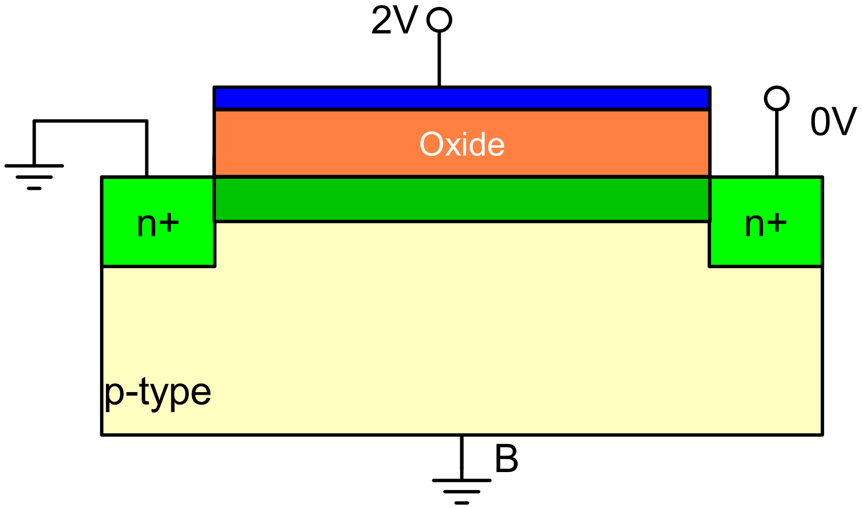
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x))$$

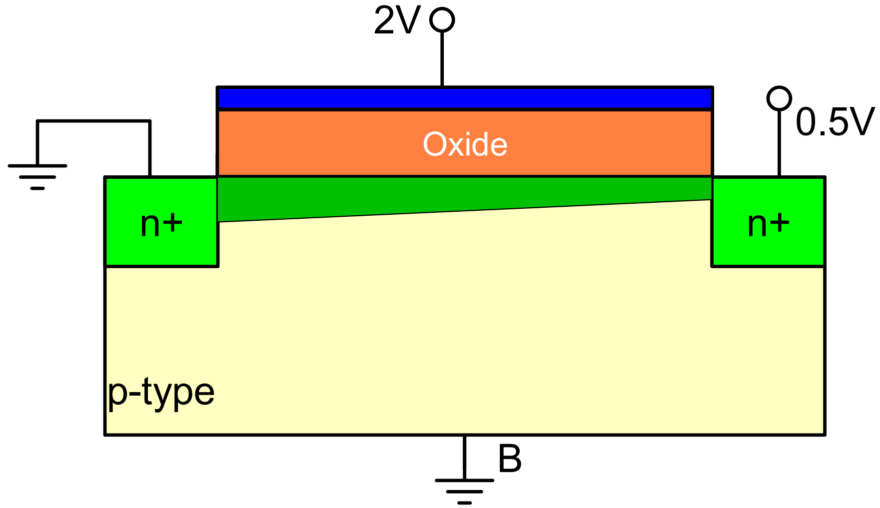


When a positive drain voltage is applied, current flows from drain to source and inversion charge density decreases from source to drain end.


2V
0V
Oxide
n+
n+
p-type
B


2V
0.5V
Oxide
n+
n+
p-type
B





$$dR_{ch} = \frac{1}{q\mu n(x)} \frac{dx}{W \times t}$$

$$R_{ch} > R_{cho}$$

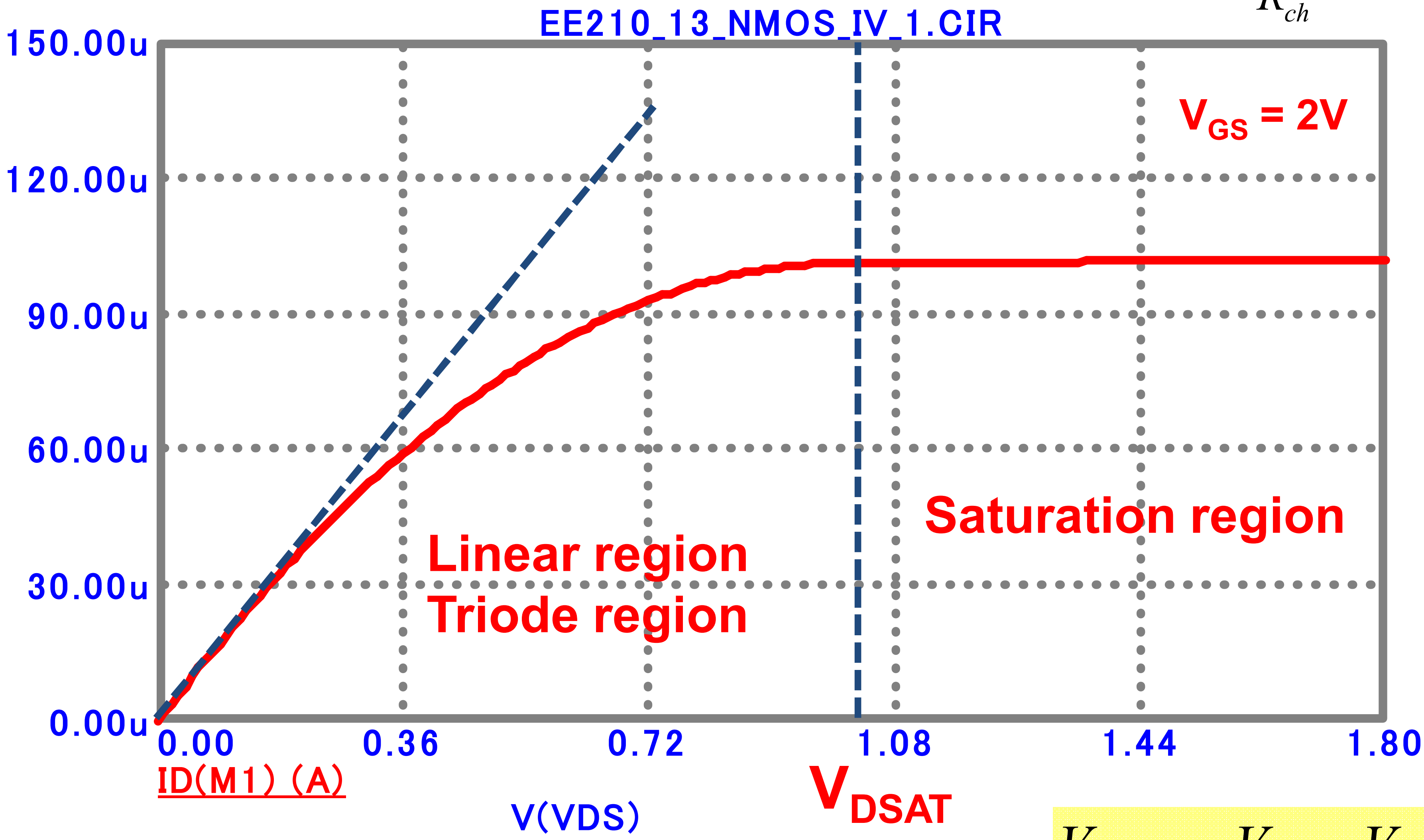
$$R_{ch} \propto \frac{1}{\int Q_{inv} dx}$$

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

$$I_{DS} = \frac{V_{DS}}{R_{cho}} = 0$$

As drain voltage increases, channel resistance also increases causing drain current to depart from linear behavior

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

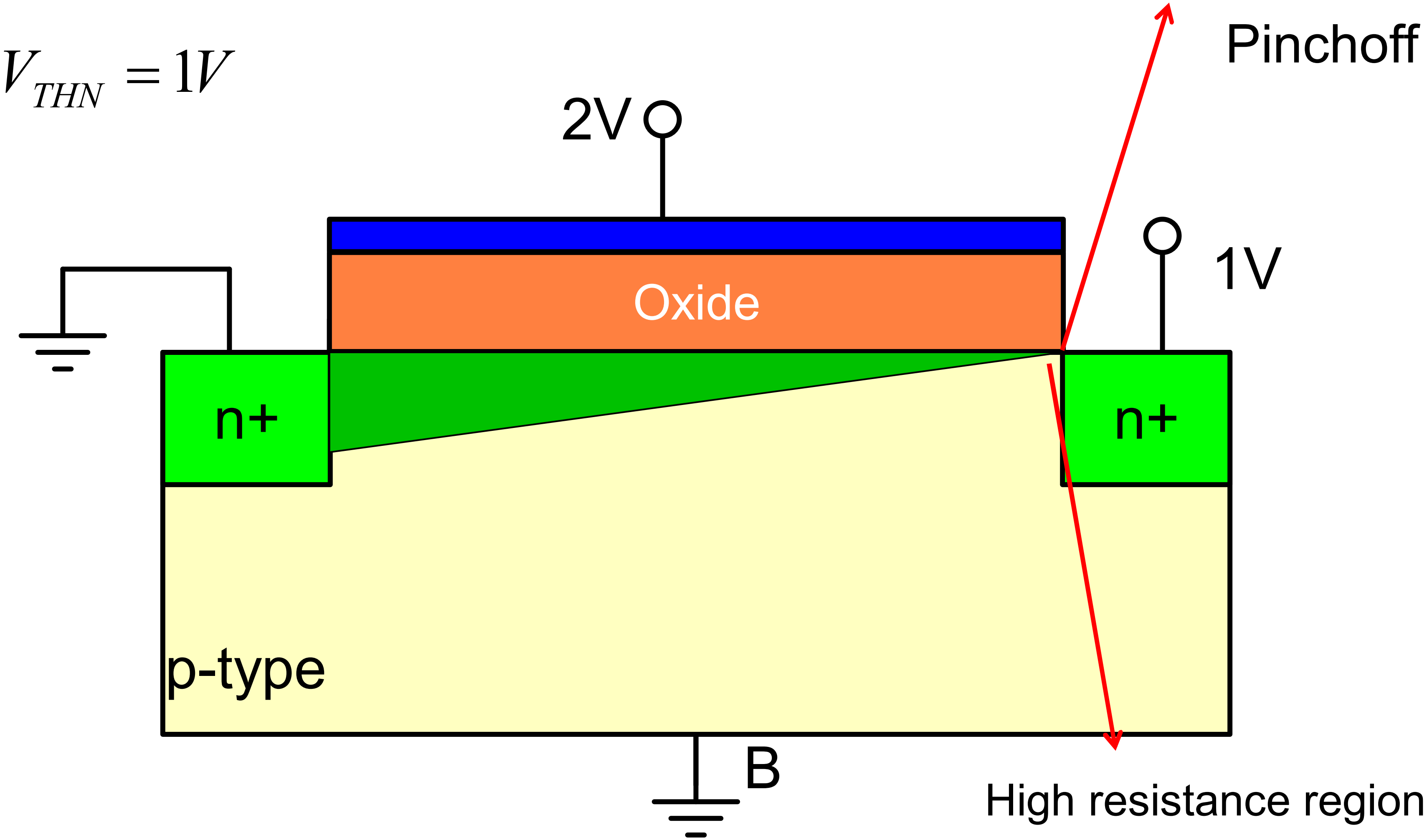


$$V_{DSAT} = V_{GS} - V_{THN}$$

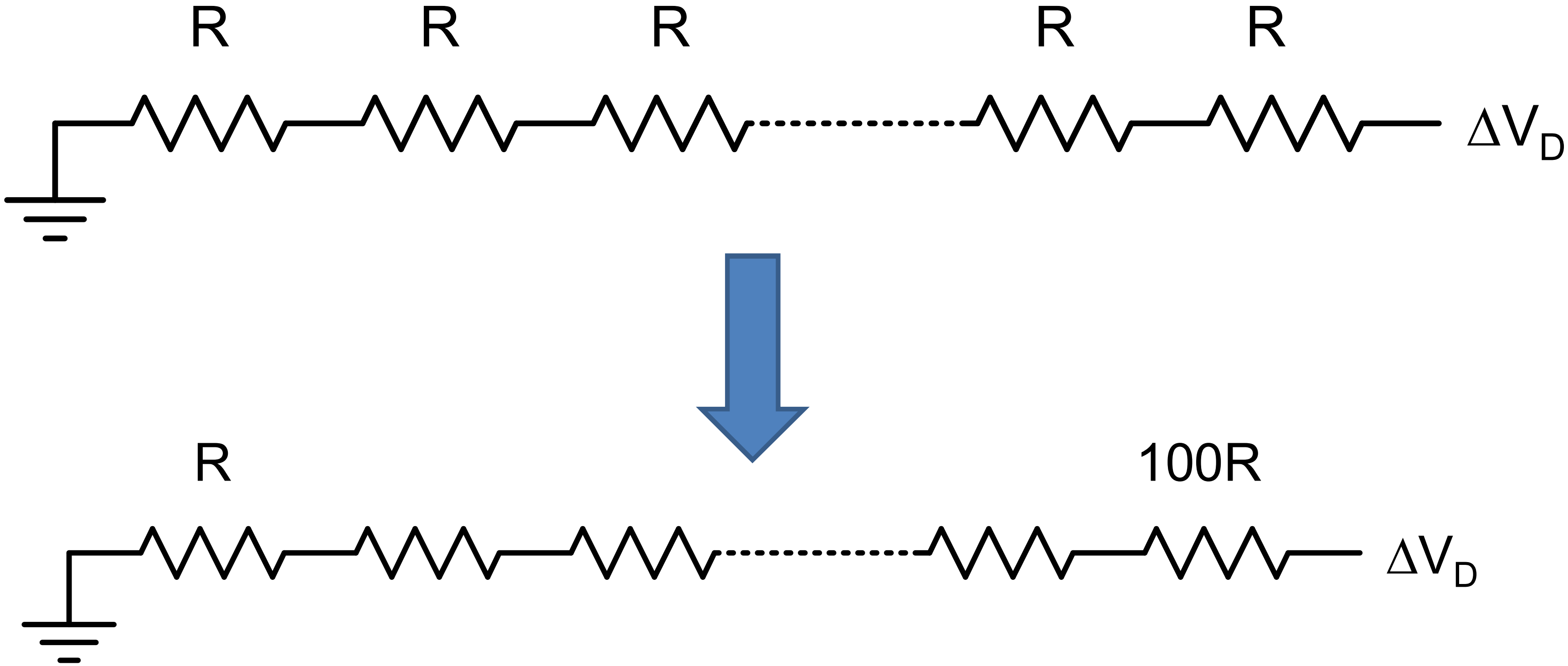
Note that **Saturation in MOSFET is analogous to forward active mode in BJT** and linear region is analogous to saturation in BJT.

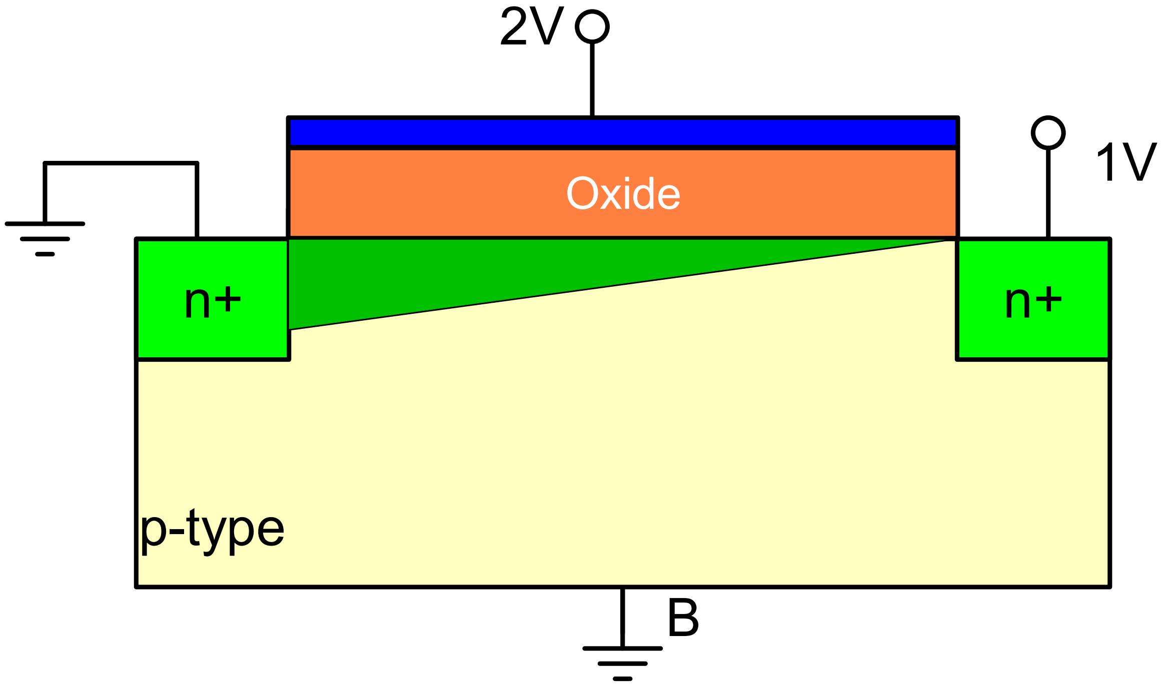
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2-1-1) = 0$$

$$V_{THN} = 1V$$



Any further increase in drain bias is absorbed in a small region next to the drain and rest of channel is not much affected and thus current becomes constant.

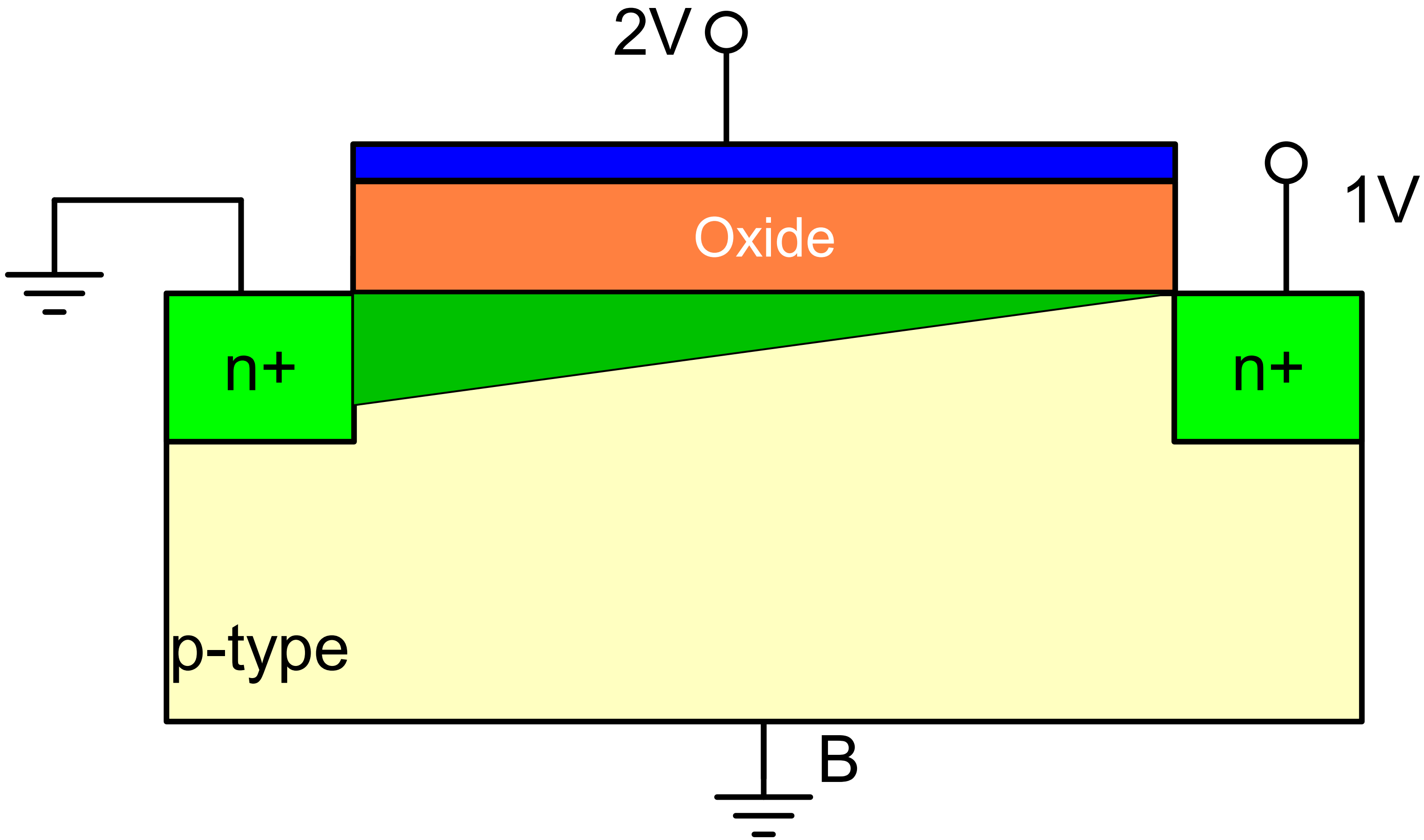

R
R
R
R
R
ΔV_D
R
100R
ΔV_D



After pinchoff or saturation, drain current does not change much with drain voltage but is still very sensitive to gate voltage. MOSFET can now **AMPLIFY** signals

$$\frac{\partial I_{DS}}{\partial V_{GS}} >> \frac{\partial I_{DS}}{\partial V_{DS}}$$

The voltage at which pinchoff occurs is the drain-saturation voltage V_{DSAT}

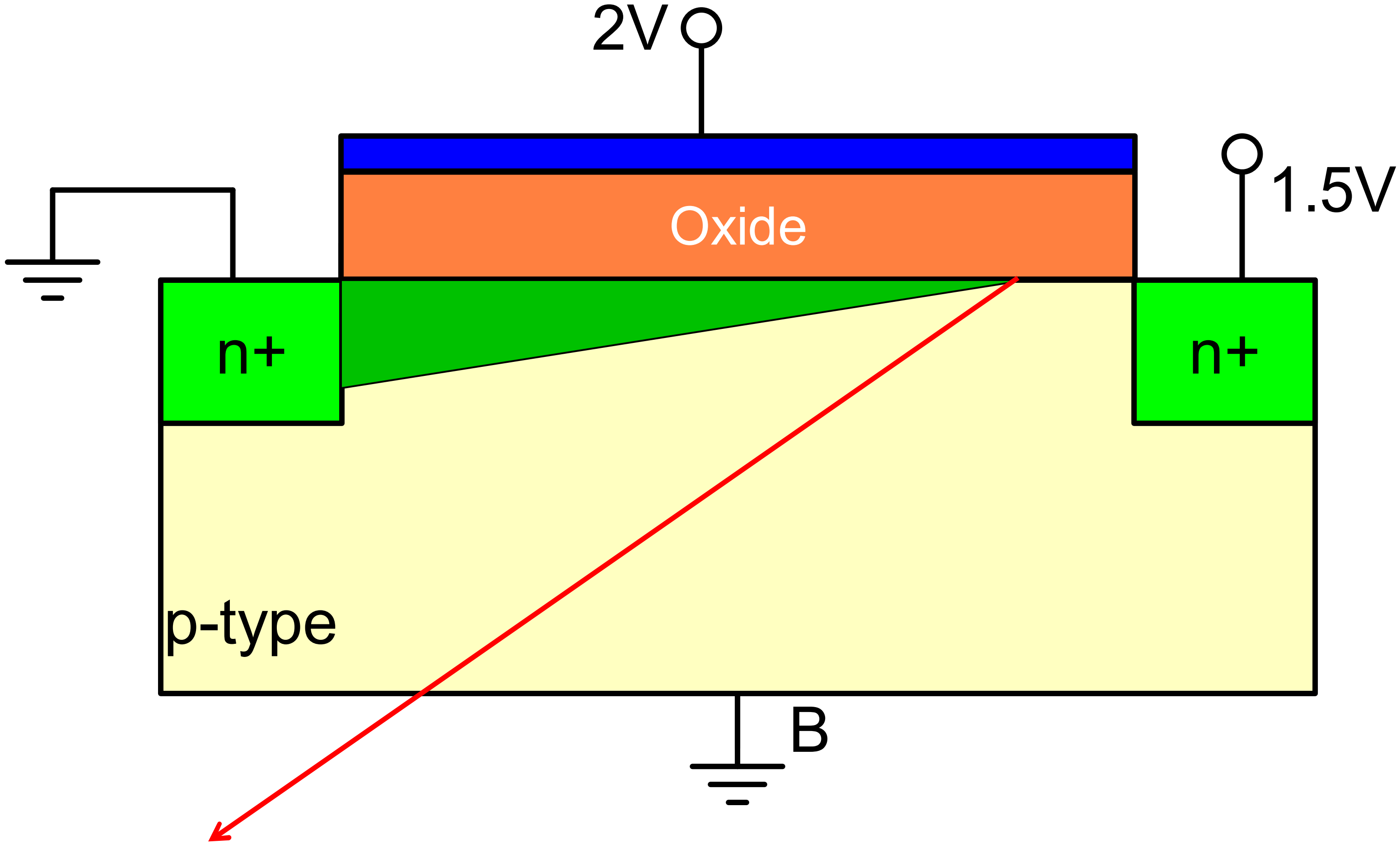


$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V_{DSAT}) \cong 0$$

$$V_{DSAT} = V_{GS} - V_{THN}$$

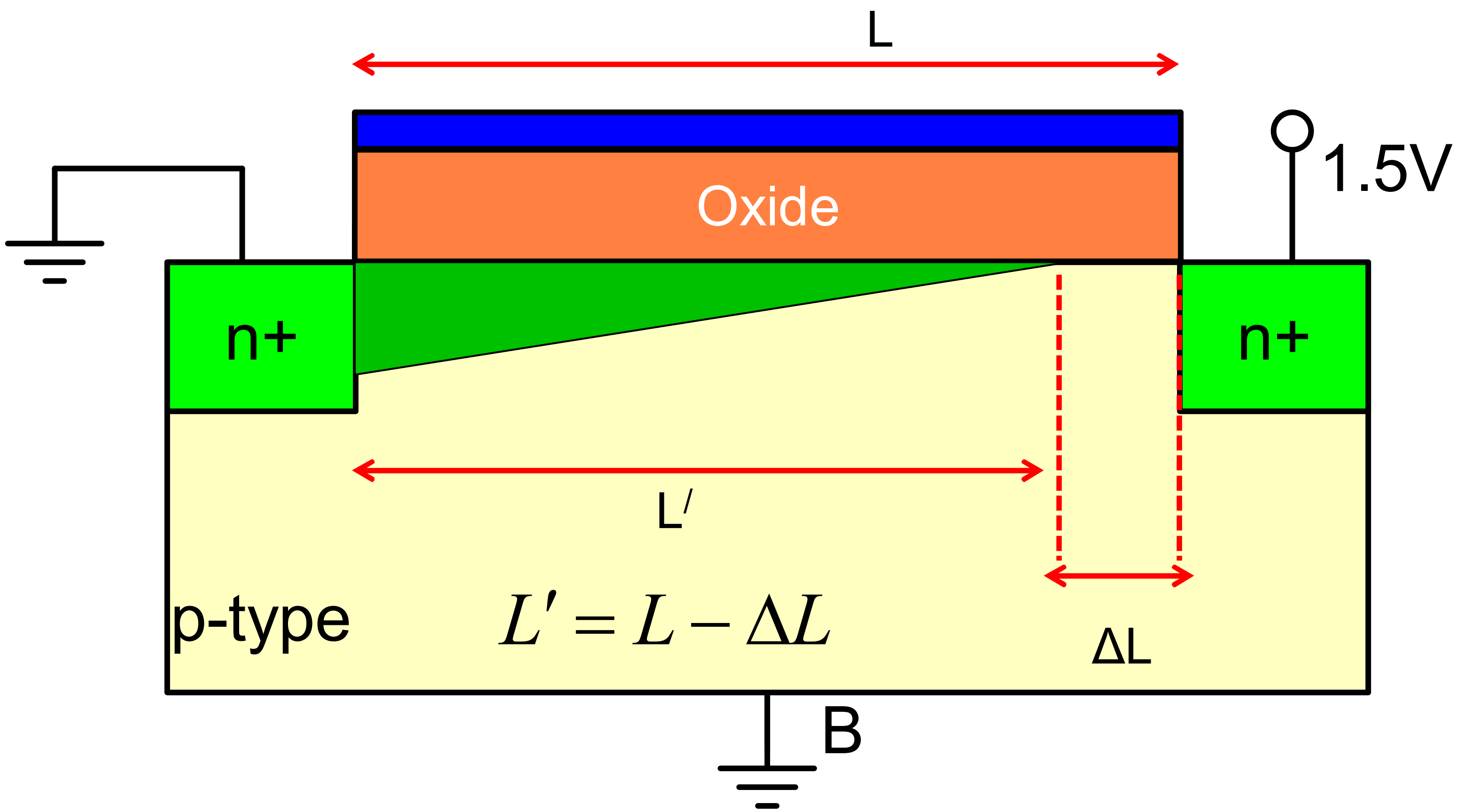
This is a very simple picture. In short channel MOSFETs especially, saturation is a more complicated phenomenon., For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2-1-1) = 0$$

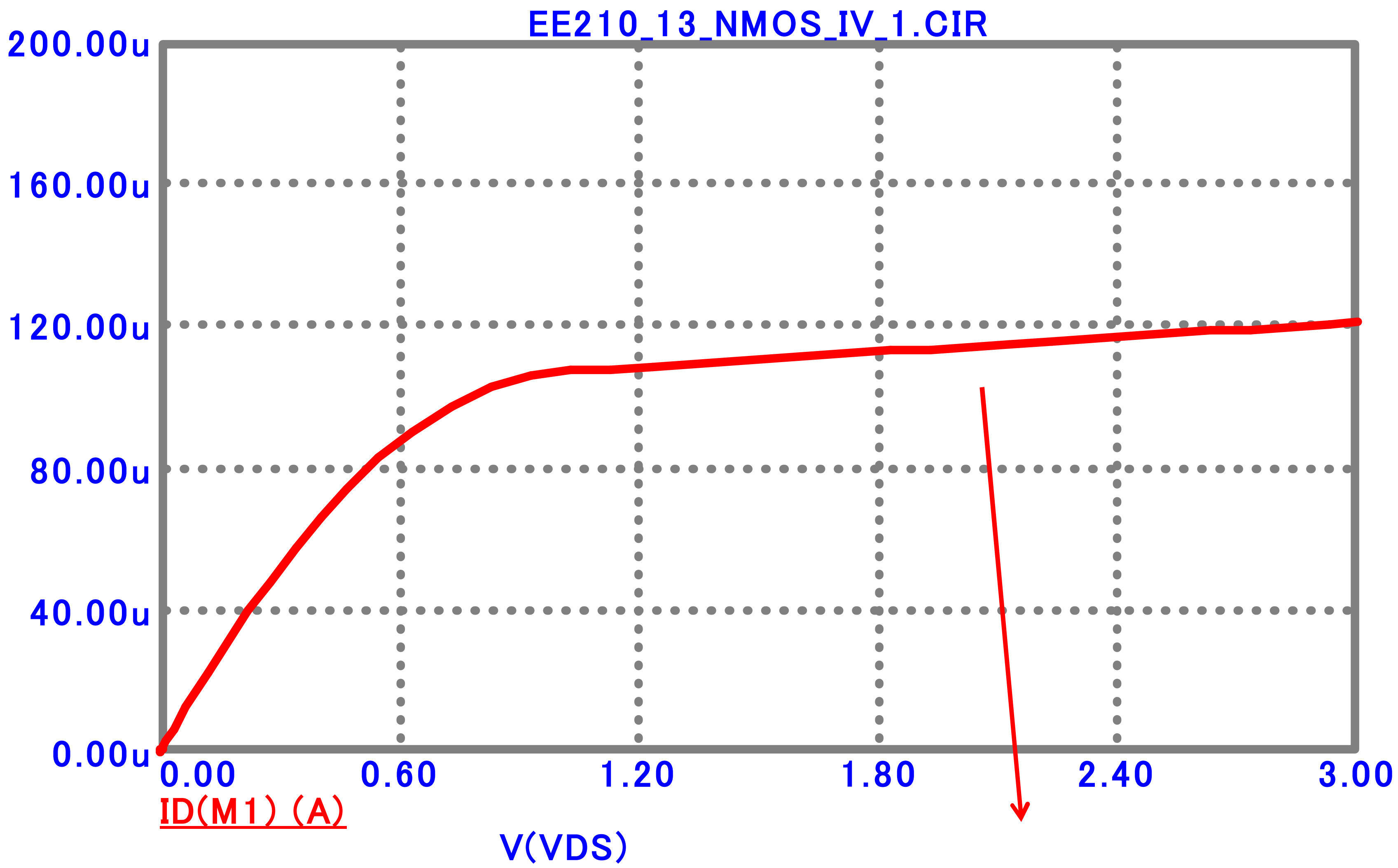


Pinchoff point moves left towards the source end. Voltage is V_{DSAT} = 1V

Channel Length Modulation



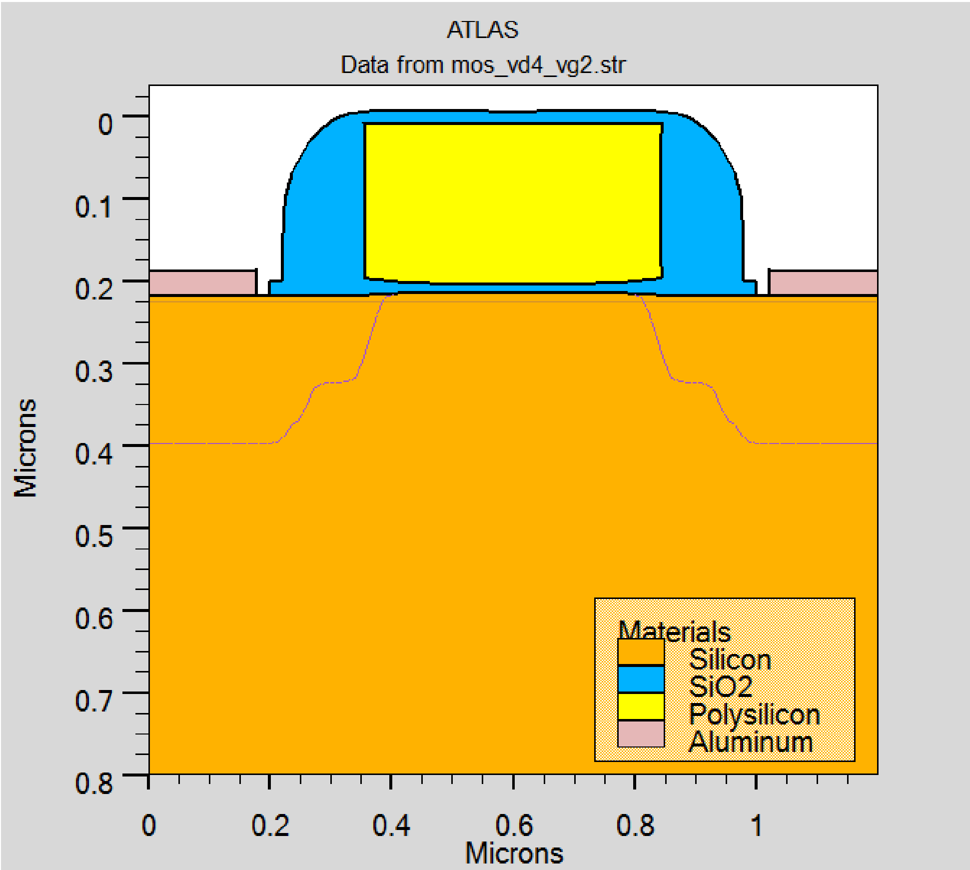
Effective channel length decreases as voltage increases beyond V_{DSAT}. As a result current increases a little with voltage

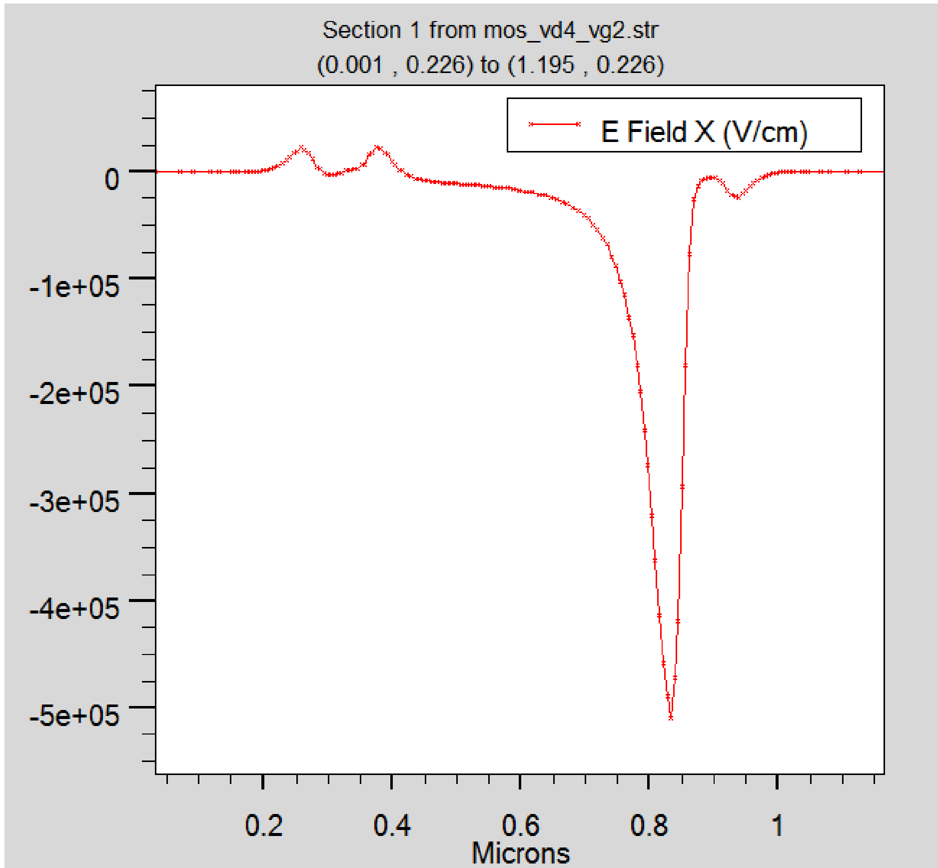


$$I_{DSAT} \times (1 + \lambda \times V_{DS})$$

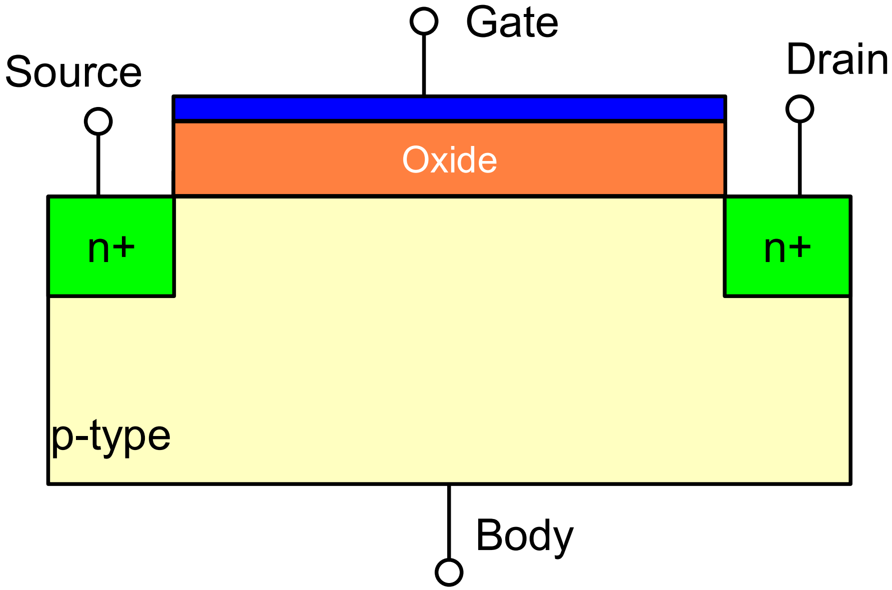
λ : channel length modulation parameter

1/ λ is analog of early voltage


ATLAS
Data from mos_vd4_vg2.str
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0
0.2
0.4
0.6
0.8
1
Microns
Materials
Silicon
SiO2
Polysilicon
Aluminum


Section 1 from mos_vd4_vg2.str
(0.001 , 0.226) to (1.195 , 0.226)
E Field X (V/cm)
0
-1e+05
-2e+05
-3e+05
-4e+05
-5e+05
0.2
0.4
0.6
0.8
1
Microns

Threshold Voltage



$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F})$$

$$V_{THNO} = 1V$$

$\gamma = body\ parameter \quad Units : \sqrt{V}$

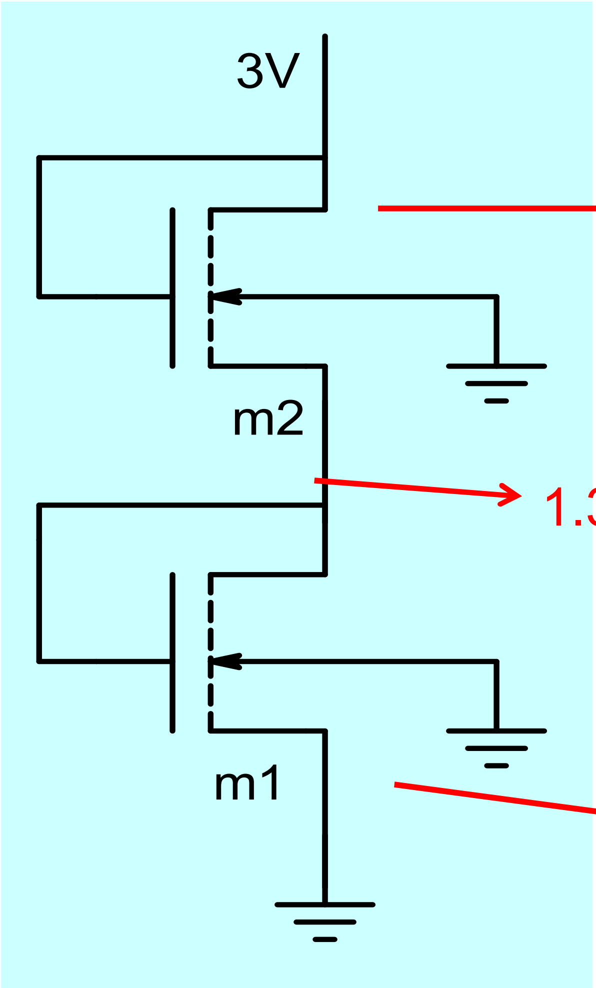
$\gamma = 0.7\ V^{1/2}$

Surface potential : $2\phi_F$

$2\phi_F = 0.7V$

$$V_{THNO} = 1V; \gamma = 0.7\ V^{1/2}; 2\phi_F = 0.7V$$

$$V_{THN} = V_{THN0} + \gamma\left(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F}\right)$$



$$V_{SB2} = 1.3V; V_{THN2} = 1.4V$$

$$V_{THN1} = V_{THN0} = 1V$$

EE210: Microelectronics-I

Lecture-39 : MOSFET-3

http://youtu.be/Y4HXLj5342s

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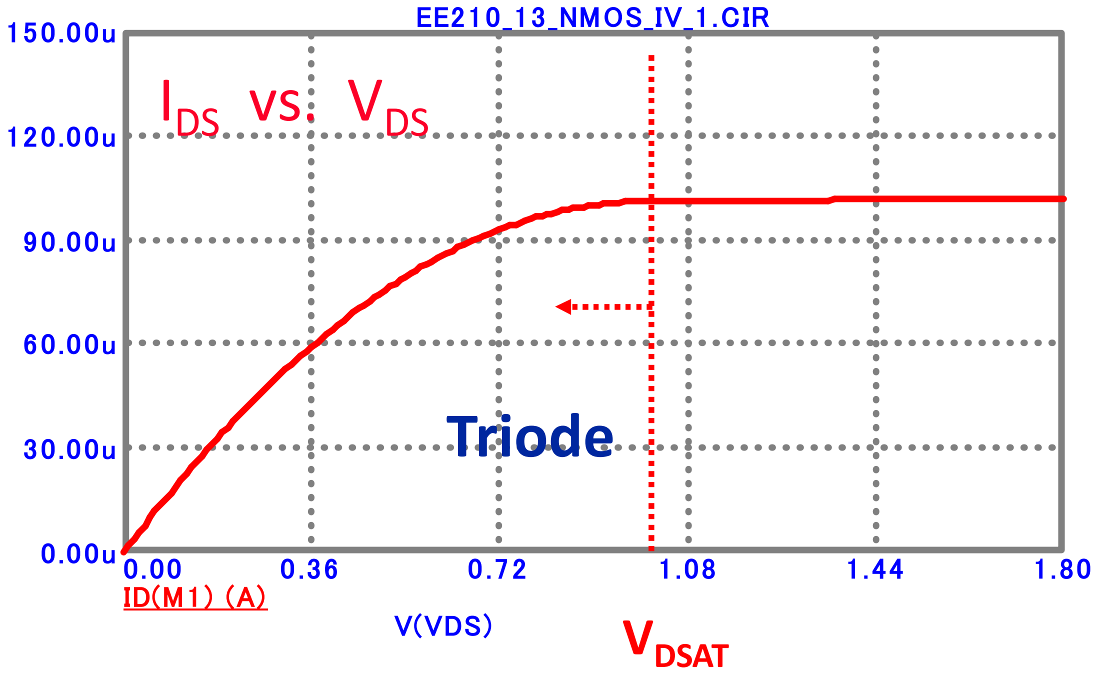
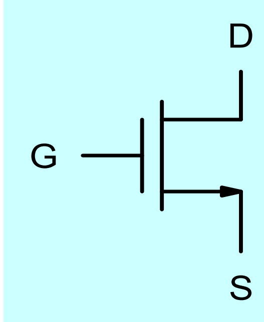
MOS Operating Regions

- **Above Threshold** ($V_{GS} > V_{TN}$)
  - **Saturation** ($V_{DS} > V_{DSAT}$)
  - **Triode** ($V_{DS} < V_{DSAT}$)
- **Subthreshold** ($V_{GS} < V_{TN}$)

dc Model: Triode (or Linear)





$$V_{GS} > V_{TN}$$

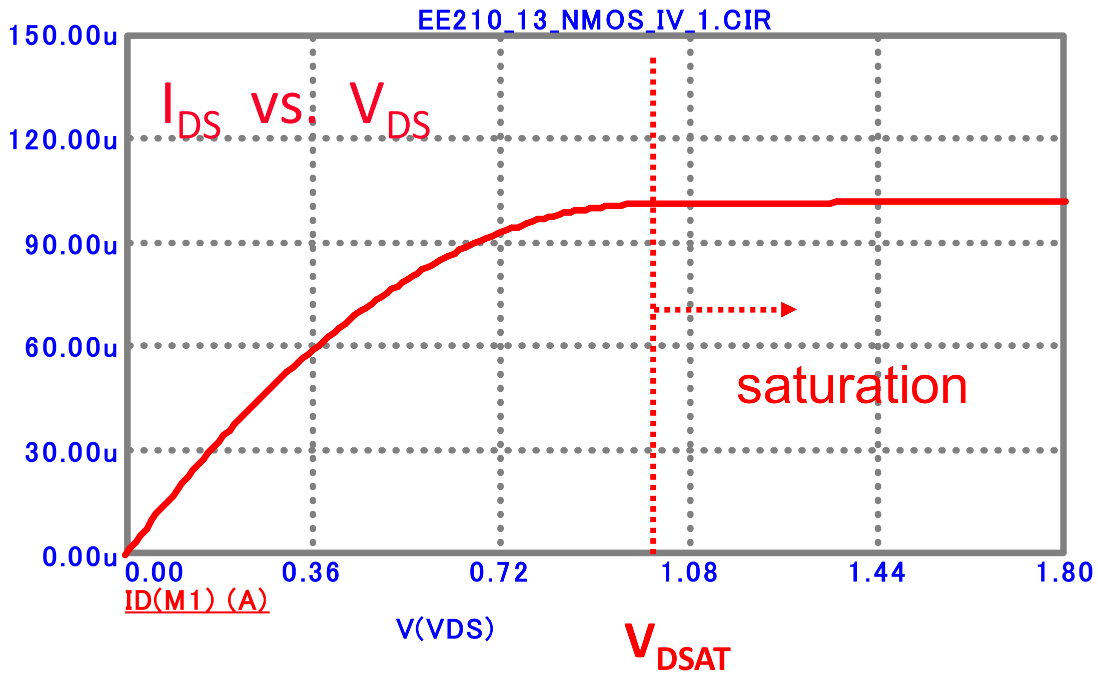
$$V_{DS} < V_{Dsat} = V_{GS} - V_{TN}$$

$$I_{DS} = \beta_N \left\{ \left(\mathrm{V}_{\mathrm{GS}} - V_{THN} \right) V_{DS} - \frac{V_{DS}{}^2}{2} \right\}$$

$$\beta_N = kP_N . \frac{W}{L}$$

$$kP_N = \mu_n C_{ox'} \; : (TransConduct\,ance\ parameter\ \frac{\mu A}{V^2})$$

DC Model: Saturation Region



$$V_{GS} > V_{THN}$$

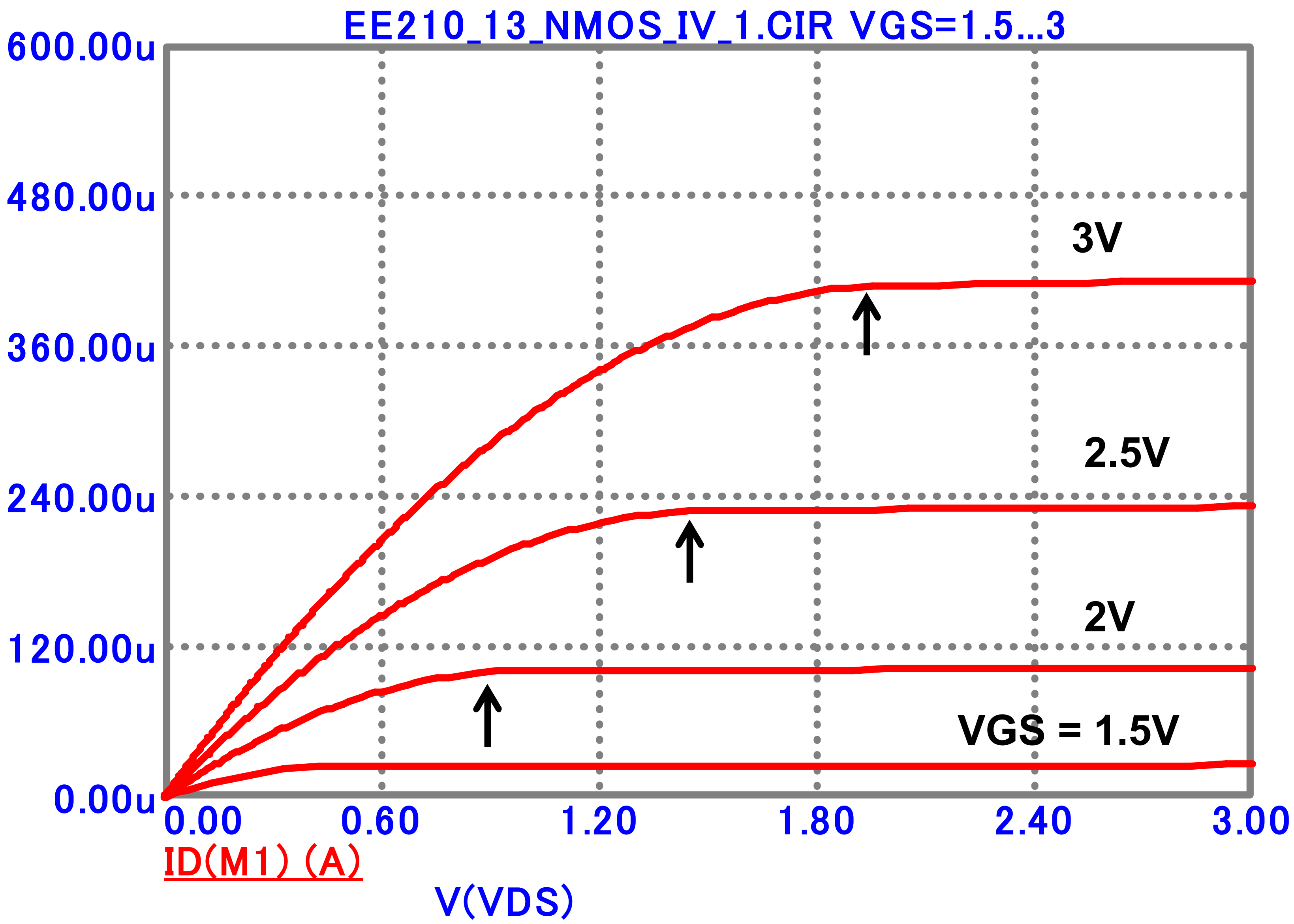
$$V_{DS} \geq V_{GS} - V_{THN}$$

$$I_{DS} = \frac{\beta_N}{2}(V_{GS} - V_{THN})^2[1 + \lambda_n V_{DS}]$$

λ_N is the channel length modulation parameter

Note that unlike BJT, VDSAT is not only larger but also dependent on applied gate-source voltage

Output Characteristics of MOSFET



dc model parameters

$$\text{Linear}: \; I_{DS} = \beta_N \left\{ (\mathrm{V_{GS}} - V_{THN}) V_{DS} - \frac{V_{DS}{}^2}{2} \right\}$$

$$\text{Saturation}: \; I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

$$\beta_N = kP_N . \frac{W}{L}$$

$$\lambda_N$$

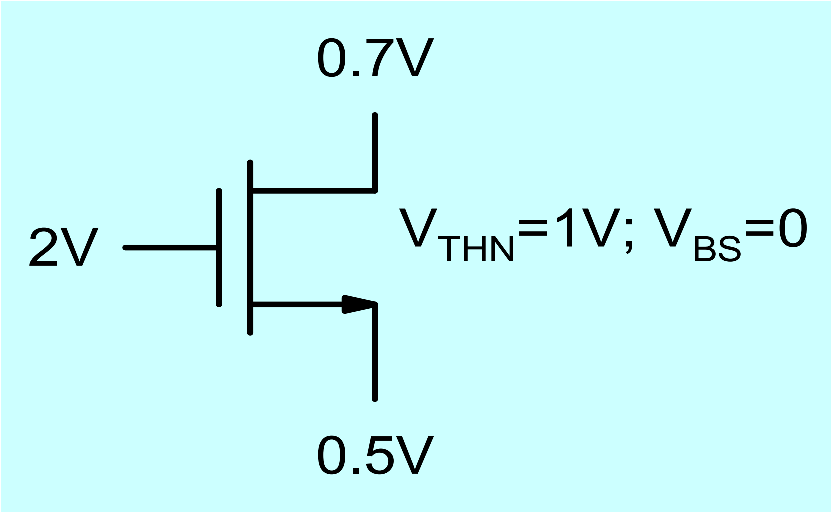
$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

$$V_{THNO} = 1V; \gamma = 0.7\ V^{1/2}; 2\phi_F = 0.7V;$$

$$KP_N = 100\mu A / V^2; L = 1\mu m; \lambda = 0.01V^{-1}$$

L is usually fixed, W is determined by designer

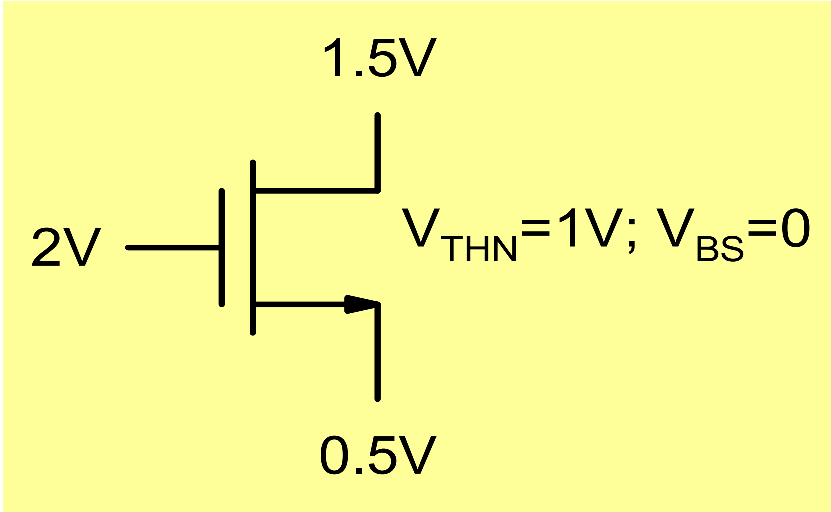
Which mode is the transistor operating in ?



$$V_{GS} = 1.5\,;\, V_{DS} = 0.2$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

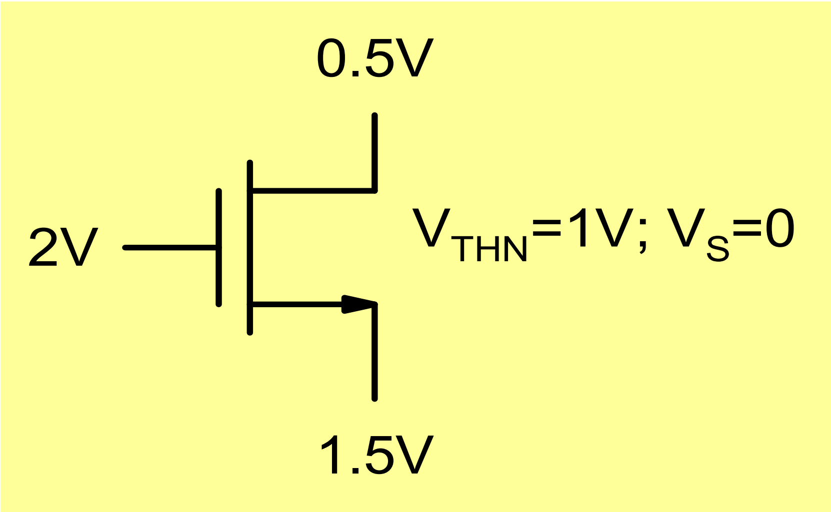
$$V_{DS} < V_{DSAT} \Rightarrow Linear$$

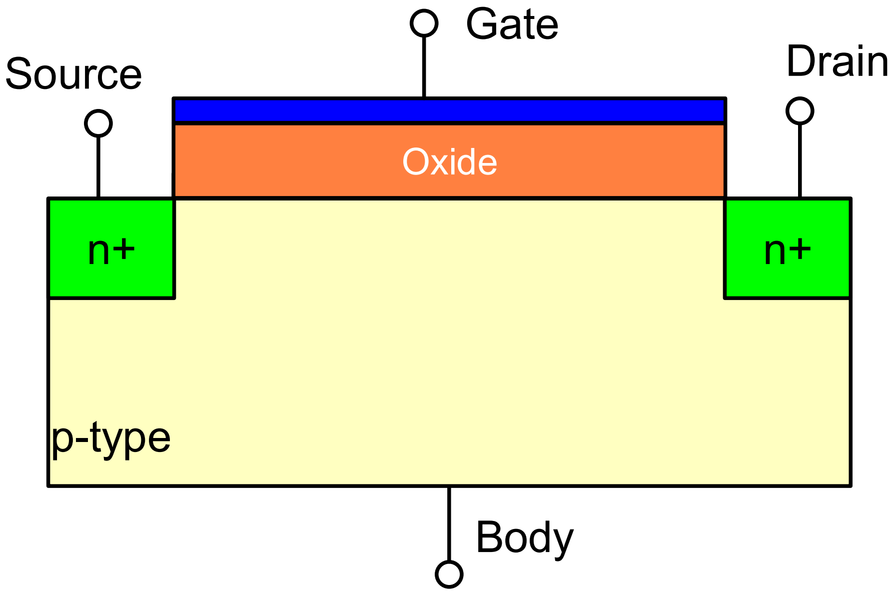


$$V_{DSAT} = 0.5\,; V_{DS} = 1V$$

Saturation

Which mode is the transistor operating in ?



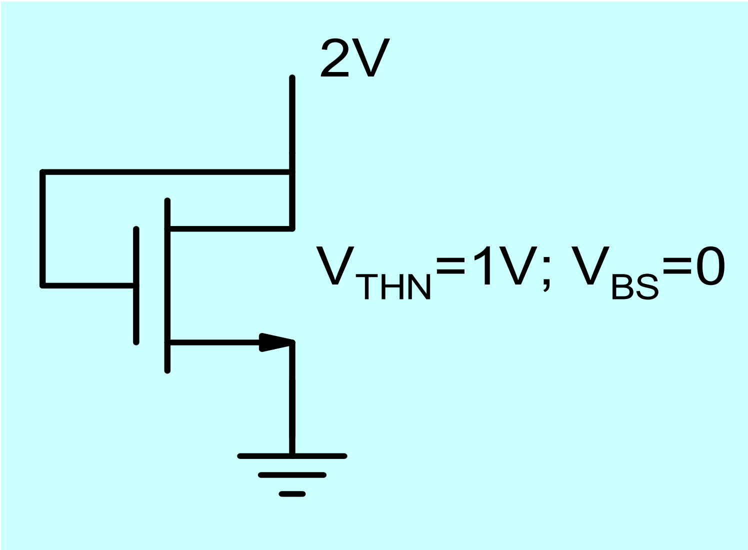


$$V_{GS} = 0.5 \; ; V_{DS} = -1V$$

$$V_{GS} = 1.5 \; ; V_{DS} = 1V$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

$$V_{DS} > V_{DSAT} \Rightarrow saturation$$



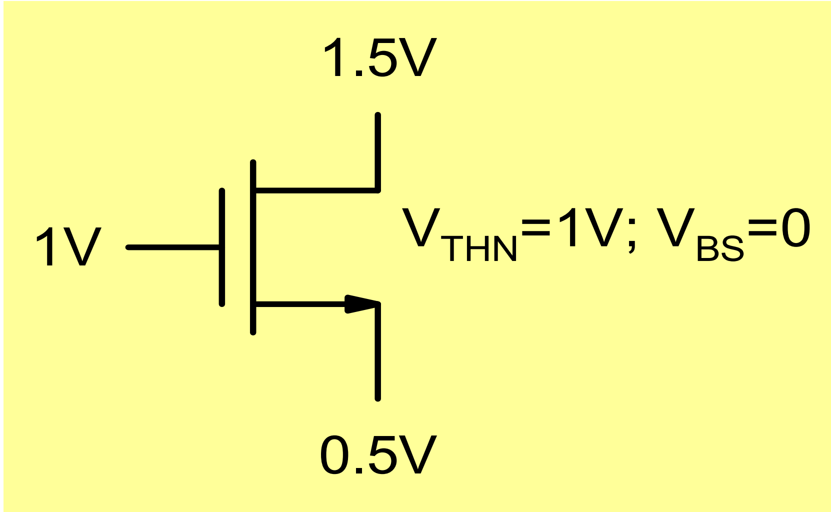
$$V_{GS} = 2\ ;\ V_{DS} = 2$$

Saturation

$$I_{DS} = \frac{\beta_N}{2}(V_{GS} - V_{THN})^2[1 + \lambda_n V_{DS}]$$

$$I_X \cong \frac{\beta_N}{2}(V_X - V_{THN})^2$$

Diode with a turn-on voltage of V_{THN}



$$V_{GS} = 0.5V < V_{THN}$$

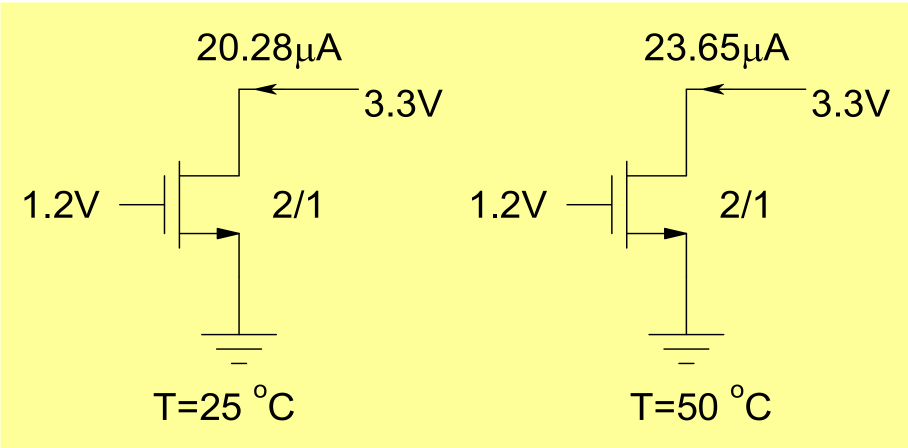
Transistor is in sub-threshold mode of operation

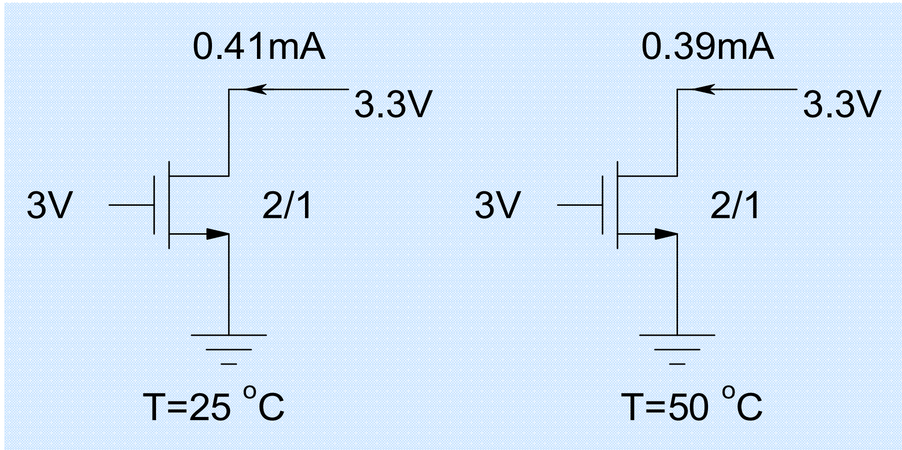
Temperature dependence

$$I_{DS} = \frac{KP_N}{2} \times \frac{W}{L} \times (V_{GS} - V_{THN})^2$$

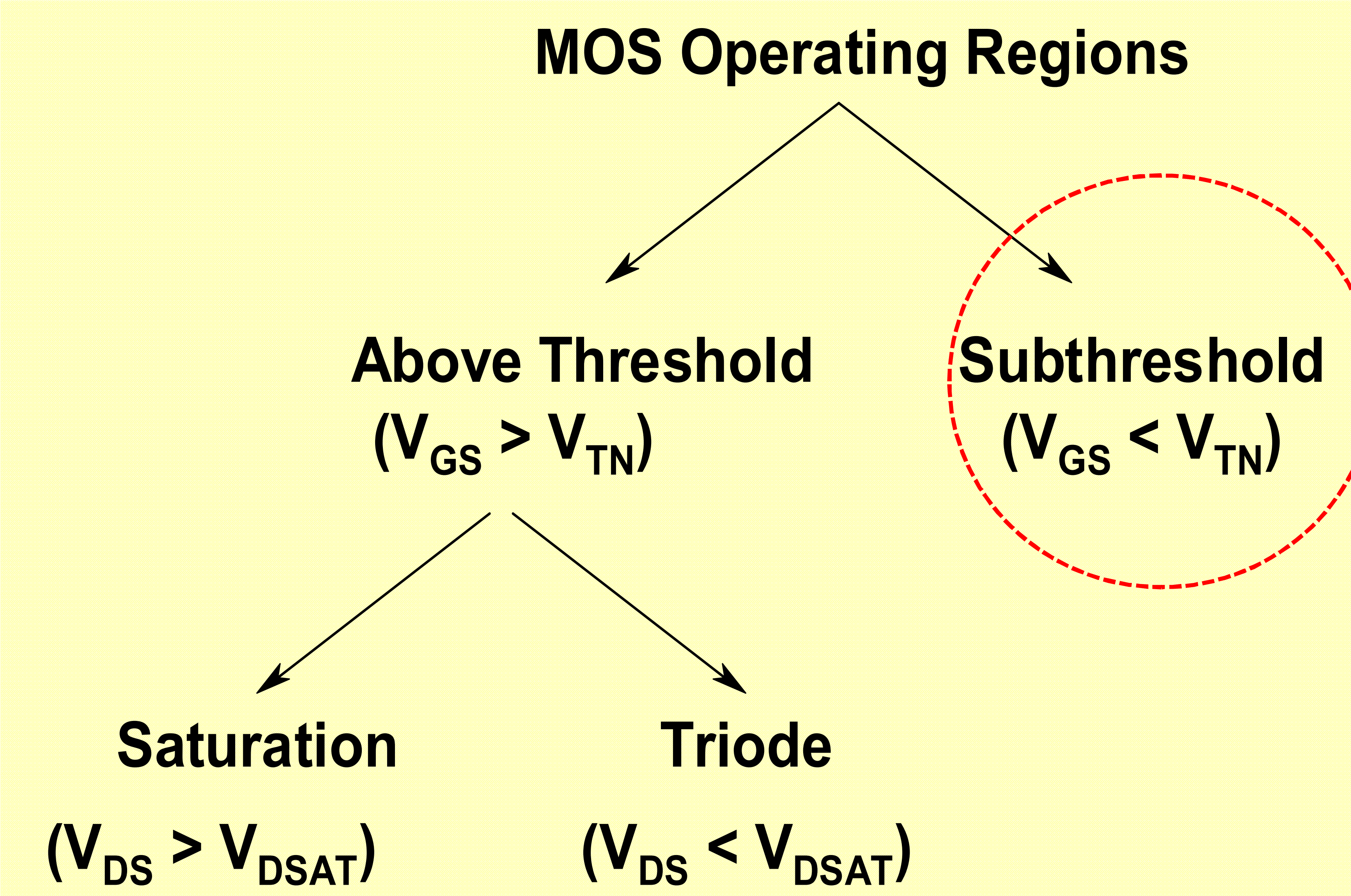
Increase in temperature causes both transconductance parameter KP_N and threshold voltage $V_{THN.}$ to decrease

Although both K_{PN} and V_{THN} and decrease with temperature, the former causes a decrease in current while the latter causes an increase in current.m



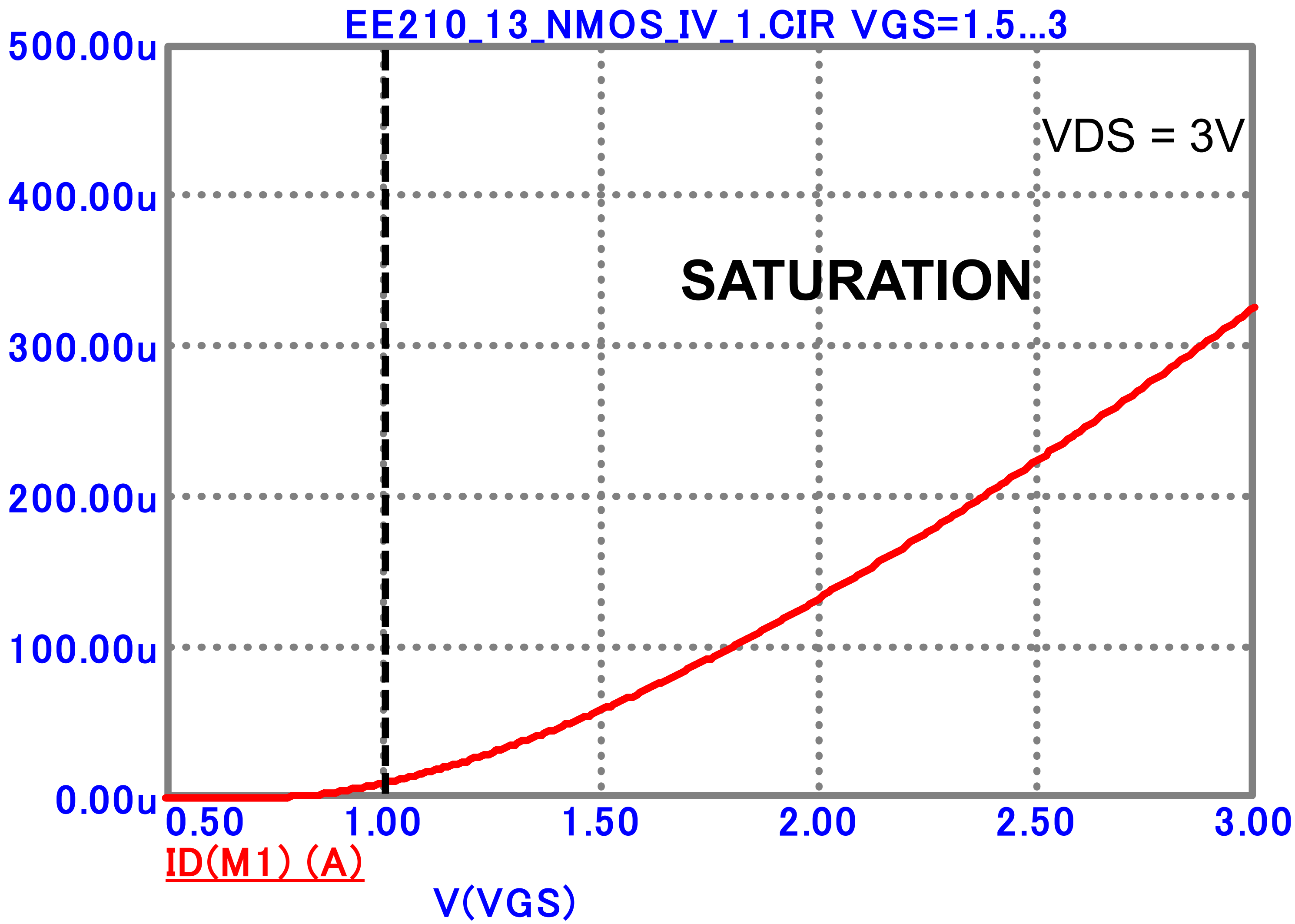


Temperature sensitivity is larger at lower gate-source voltages

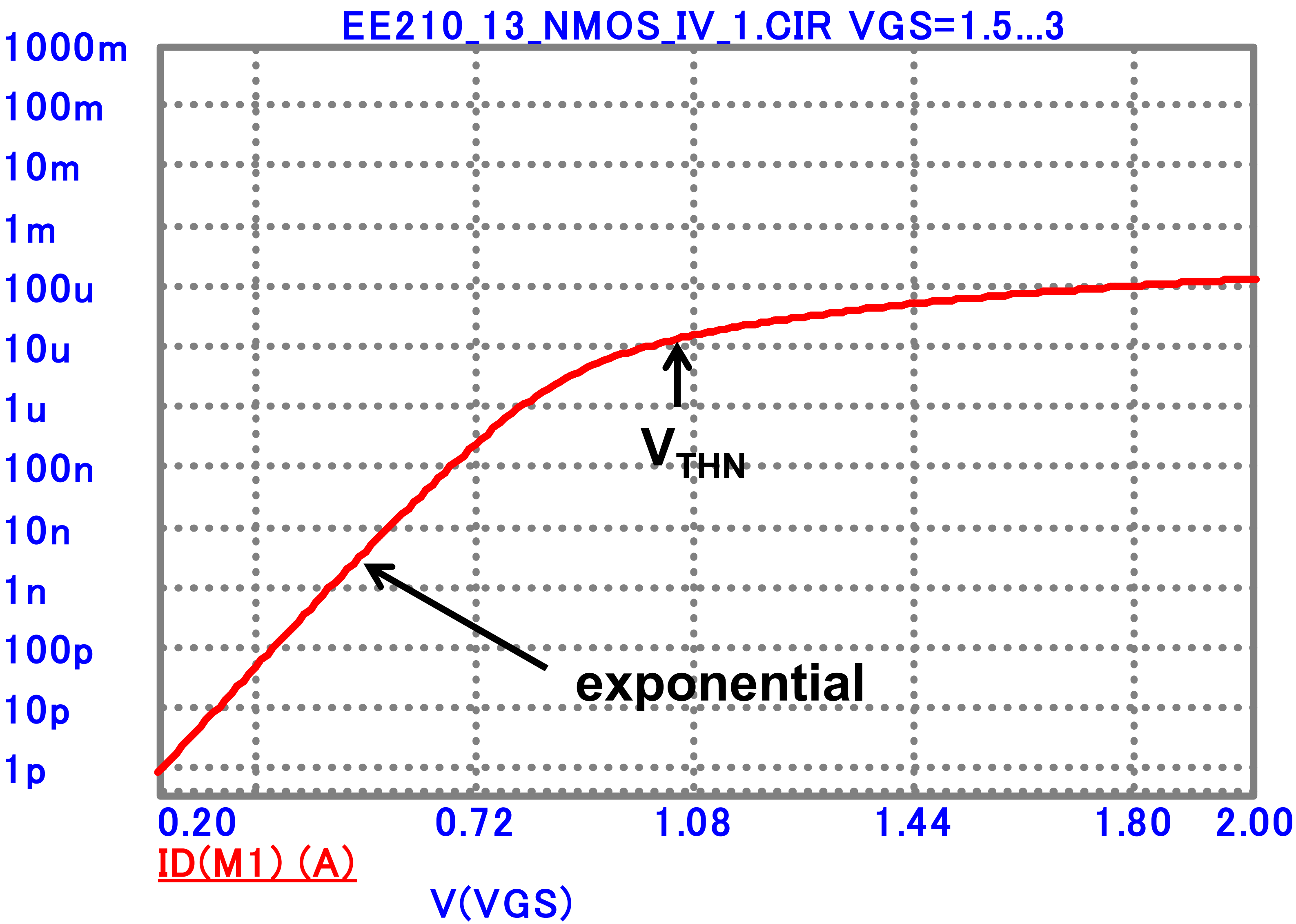


MOS Operating Regions
Above Threshold
($V_{GS} > V_{TN}$)
Subthreshold
($V_{GS} < V_{TN}$)
Saturation
($V_{DS} > V_{DSAT}$)
Triode
($V_{DS} < V_{DSAT}$)

Transfer characteristics of NMOS



Current is very small until gate-source voltage **exceeds threshold voltage V_{THN}**


EE210_13_NMOS_IV_1.CIR VGS=1.5...3
1000m
100m
10m
1m
100u
10u
1u
100n
10n
1n
100p
10p
1p
0.20
0.72
1.08
1.44
1.80
2.00
ID(M1) (A)
V(VGS)
V_{THN}
exponential

$$I_D \propto e^{\frac{qV_{GS}}{N'kT}}$$

$$g_m = \frac{\partial I_{DS}}{\partial Vgs} = \frac{I_{DS}}{nV_T}$$

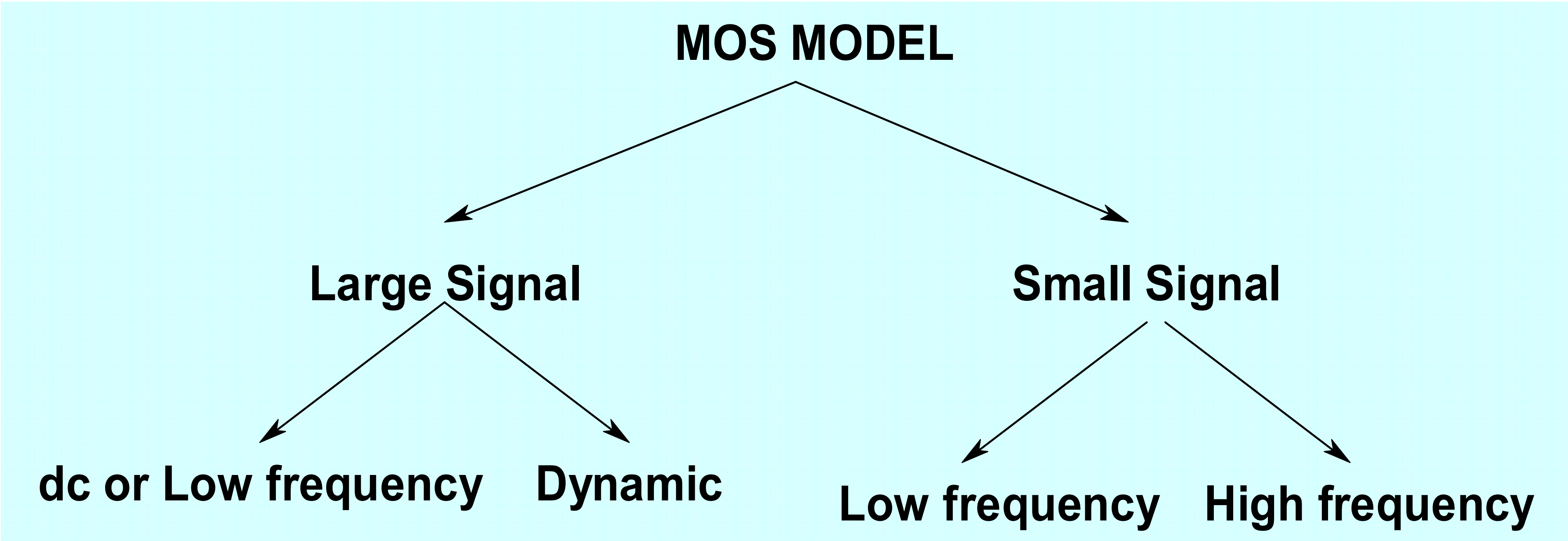
- In subthreshold region, MOS acts like a BJT

$$BJT: \qquad I_C = I_S e^{V_{BE}/V_T}$$

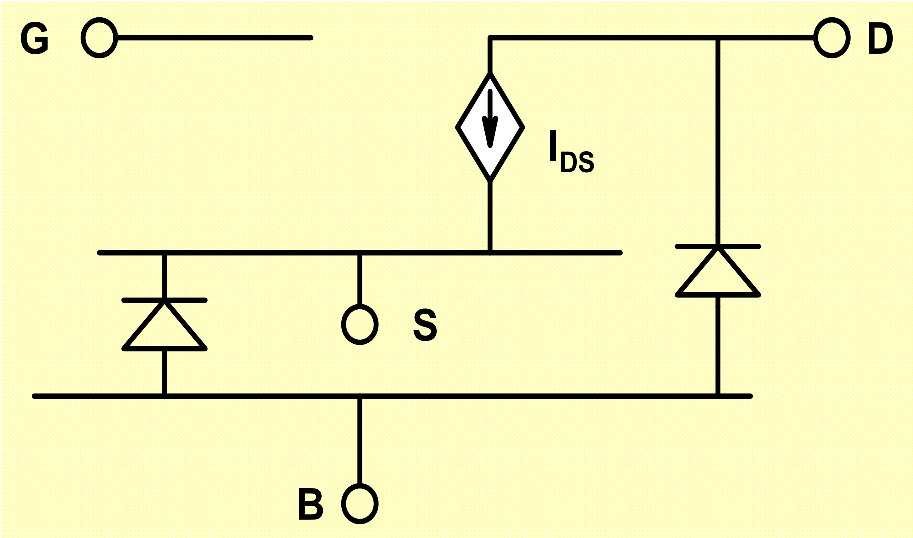
$$MOS: \quad I_{DS} = I_S e^{V_{GS}/\eta V_T}$$

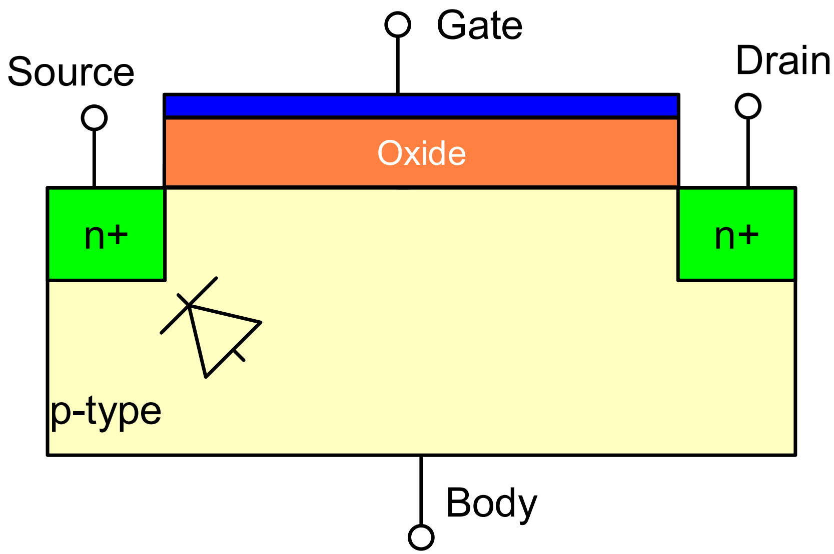
- The advantage of MOS is that it offers almost infinite input impedance. Its disadvantage is that current levels are low.

MOS models : The classification of models can be done on the basis of magnitude and frequency of applied voltages



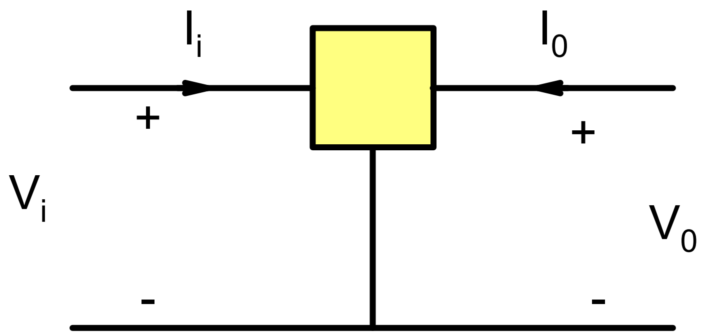
The dc model of the transistor in triode and saturation region can be represented in the form of an equivalent circuit:

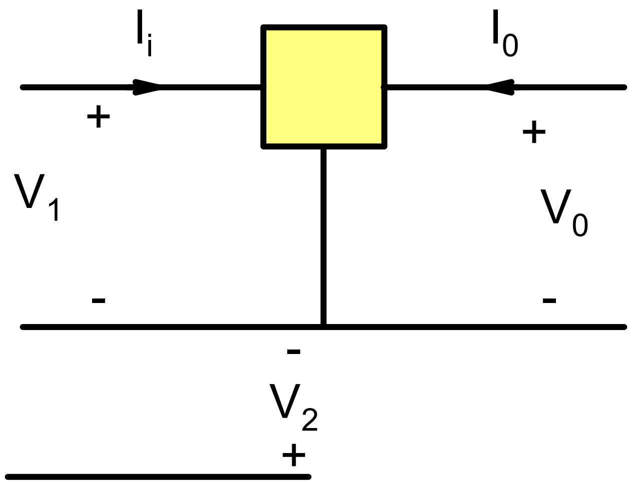


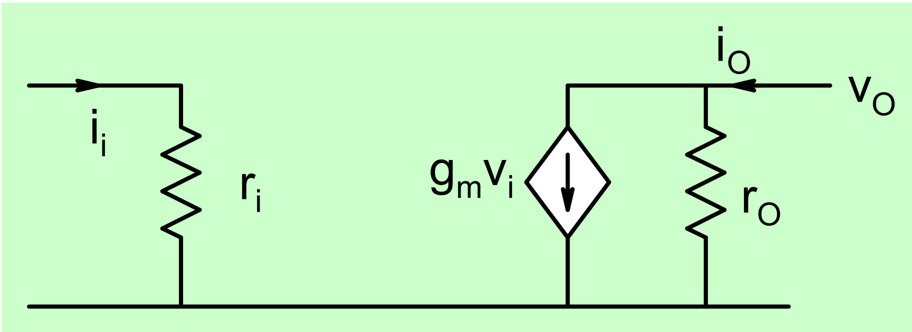


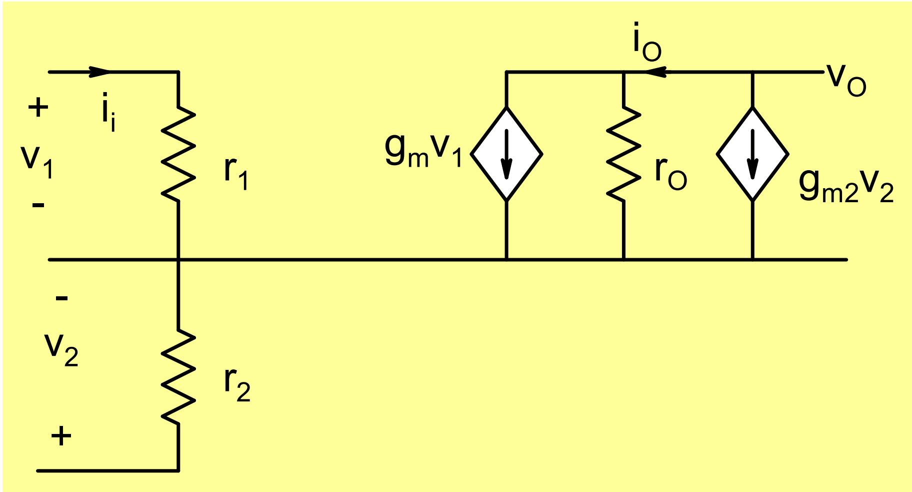
Series resistance associated with gate, source, drain and body terminals is not shown but can play an important role.

Complete small signal model (dc) for a 3-terminal unilateral device.

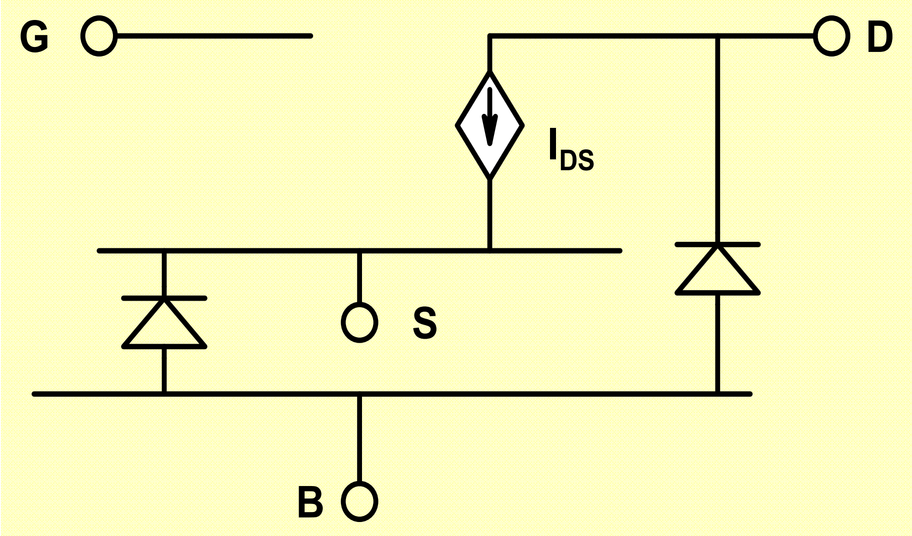








Small Signal Model (dc/low frequency)



$$I_{ds} = \frac{\beta_N}{2}\left(V_{gs} - V_{THN}\right)^2 (1 + \lambda_n V_{ds})$$

$$V_{gs} = V_{GSQ} + v_{gs}$$

$$V_{ds} = V_{DSQ} + v_{ds}$$

$$V_{sb} = V_{SBQ} + v_{sb}$$

$$I_{ds} = I_{DSQ} + i_{ds}$$

$$I_{DSQ} + i_{ds} = \frac{\beta_N}{2}\left[V_{GSQ} + v_{gs} - V_{THN}\left(V_{BSQ} + v_{bs}\right)\right]^2\left(1 + \lambda_n V_{DSQ} + \lambda_n v_{ds}\right)$$

$$i_{ds} \cong I_{DSQ}\left\{\left(\lambda_n v_{ds} + \frac{2v_{gs}}{V_{GSQ} - V_{THN}} + \frac{\gamma \times v_{bs}}{(V_{GSQ} - V_{THN}) \times \sqrt{2\varphi_F - V_{BSQ}}}\right)\right\}$$

$$i_{ds} = \frac{v_{ds}}{r_o} + g_m v_{gs} + g_{mb} v_{bs}$$

$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

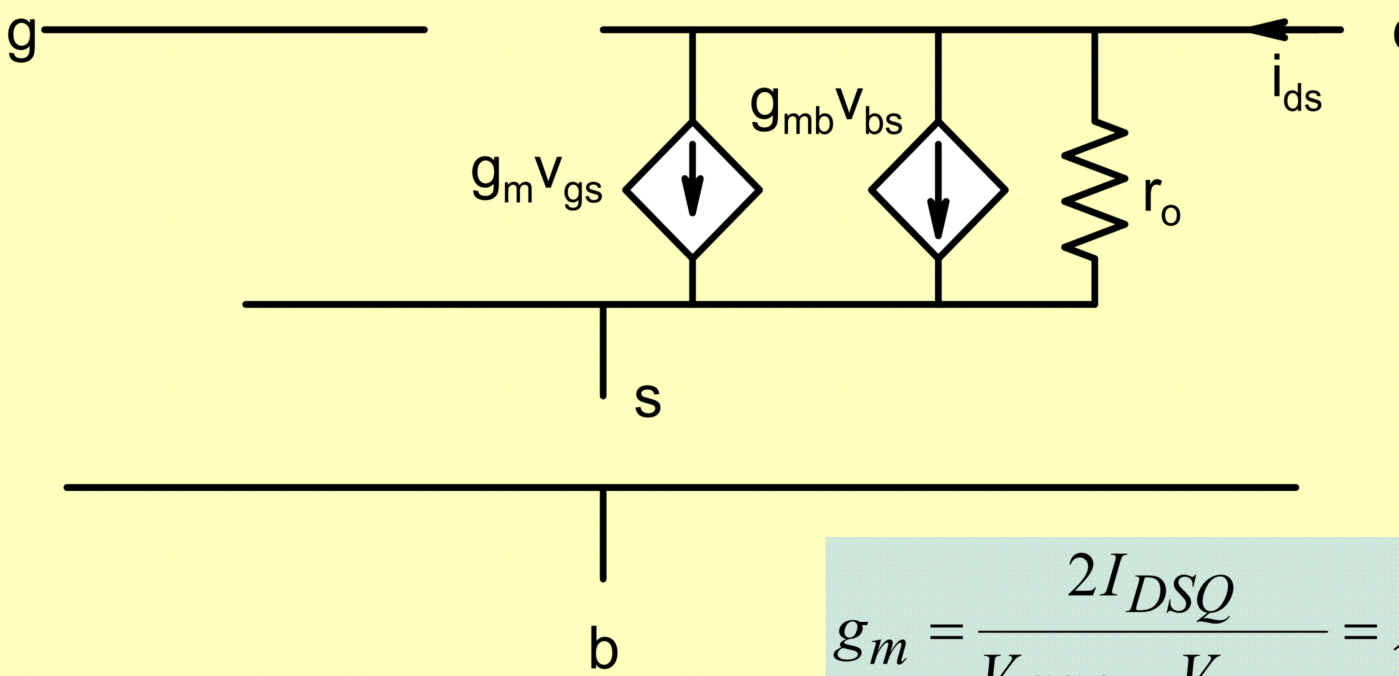
$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} = \sqrt{2I_{DSQ}\beta}$$

$$g_{mb} = g_m . \eta$$

$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SBQ}}}$$

Low frequency Small Signal model

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o}$$



$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} = \sqrt{2I_{DSQ}\beta}$$

$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

$$g_{mb} = g_m.\eta$$

$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SBQ}}}$$

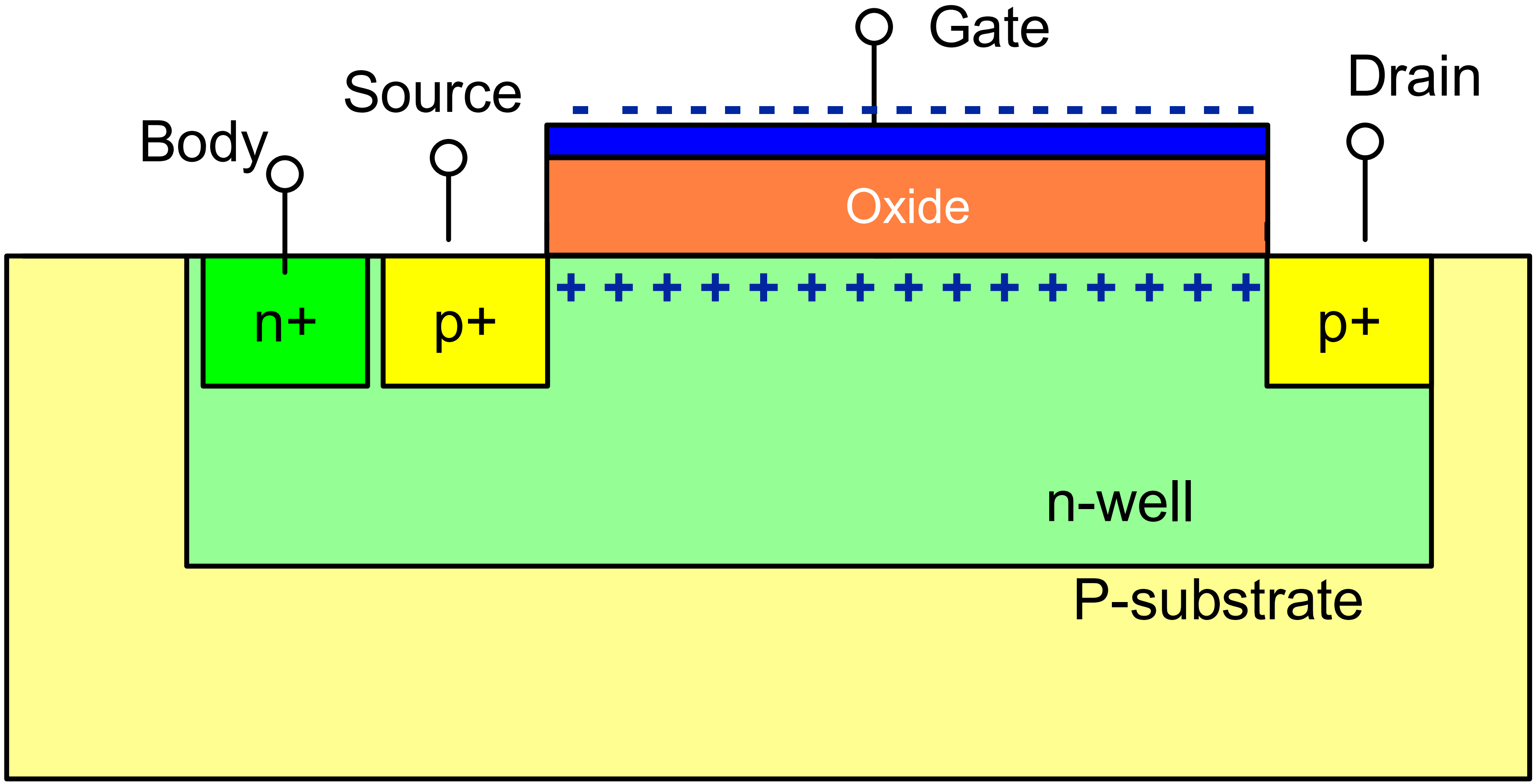
G-Number

The small signal approximation $i_{ds} = g_m v_{gs}$ is accurate when $v_{gs} << 2(V_{GS} - V_{THN})$

v_{gs}/V_{GS}-V_{THN}	**+0.1**	**-0.1**	**+0.2**	**-0.2**	**+0.5**	**-0.5**	**1**	**-1**
Error (%)	-4.7	5.26	-9.1	11.11	-20	33.33	-33.3	100

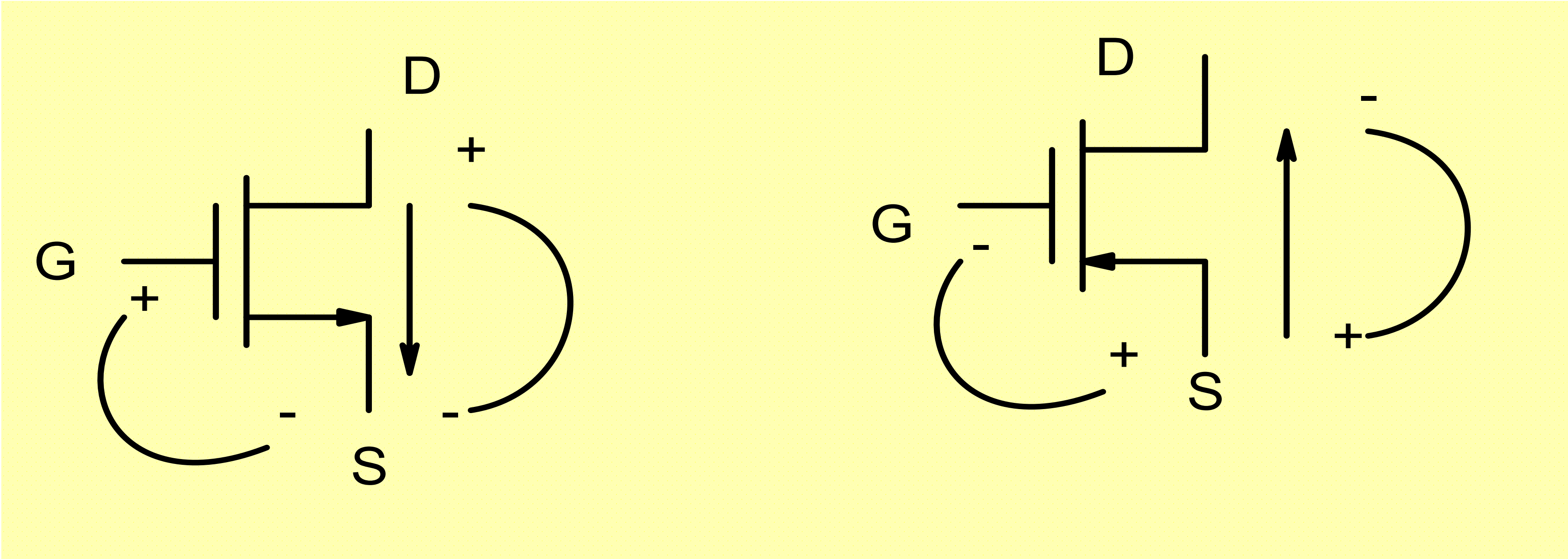
For positive values of v_{gs}, the small signal approximation results in underestimation of current while for negative values, the current is overestimated.

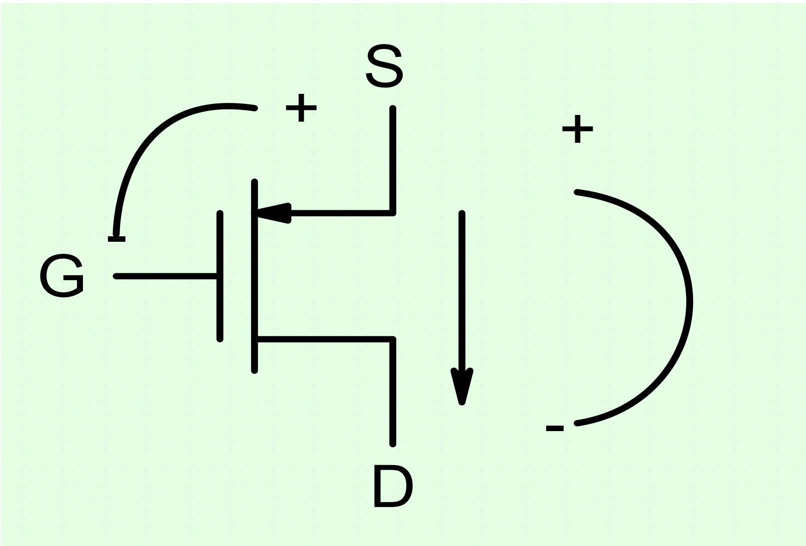
PMOS



V_{GS} is negative ; Threshold voltage V_{TP} is negative

V_{DS} is negative ; I_{DS} is negative





$$V_{GSN} \to V_{SGP}$$

$$I_{DSN} \to I_{SDP}$$

$$V_{DSN} \to V_{SDP}$$

Transformations

$$V_{GSN} \to V_{SGP} \qquad V_{DSN} \to V_{SDP} \qquad V_{BSN} \to V_{SBP}$$

$$V_{THN} \to -V_{THP} \qquad I_{DSN} \to I_{SDP}$$

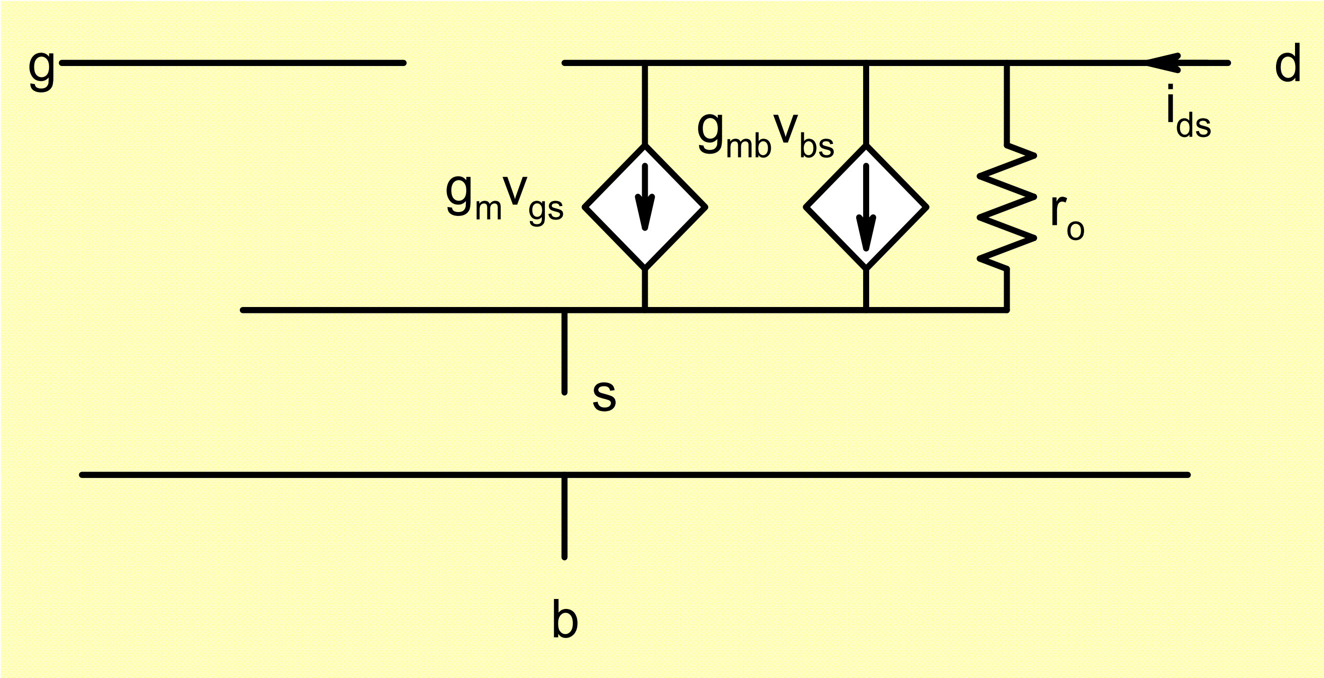
$$I_{DS} = \frac{\beta_N}{2}(V_{GS} - V_{THN})^2[1 + \lambda_n V_{DS}] \to$$

$$I_{SD} = \frac{\beta_P}{2}(V_{SG} + V_{THP})^2[1 + \lambda_p V_{SD}]$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + \frac{v_{sd}}{r_o}$$

$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \dfrac{v_{ds}}{r_o}$ same as NMOS

Small Signal Model



$$g_m = \frac{2I_{SDQ}}{V_{SGQ} + V_{THP}}$$

$$r_o = \frac{1}{\lambda_p I_{SDQ}}$$

EE210: Microelectronics-I

Lecture-40 : MOSFET-4

http://youtu.be/wyKFeaKHak8

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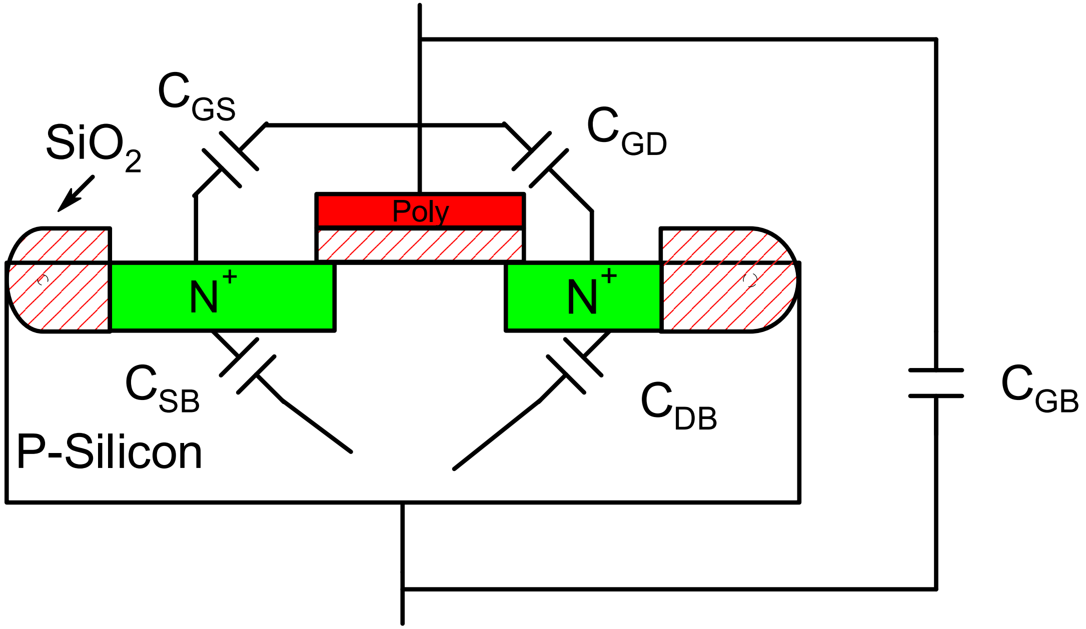
Dept. of EE, IIT Kanpur

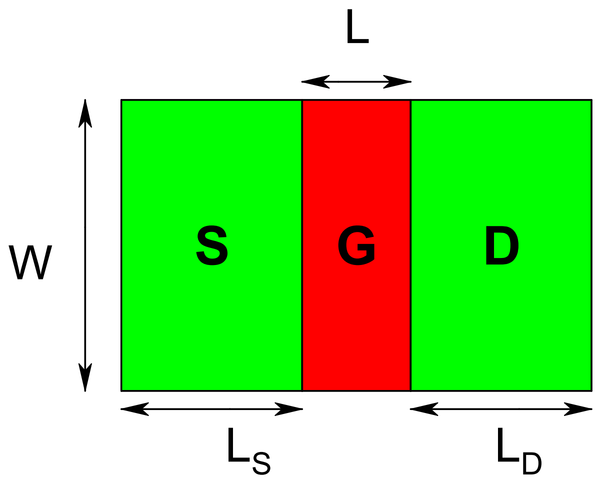
Capacitance Model Saturation

•. There are five distinct components of capacitance as illustrated below

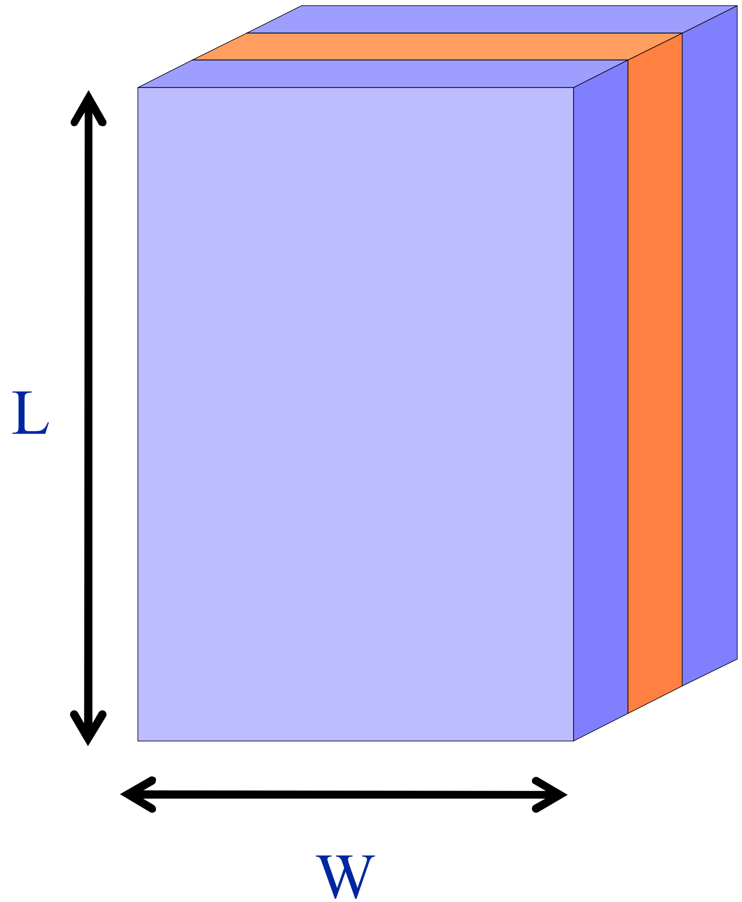


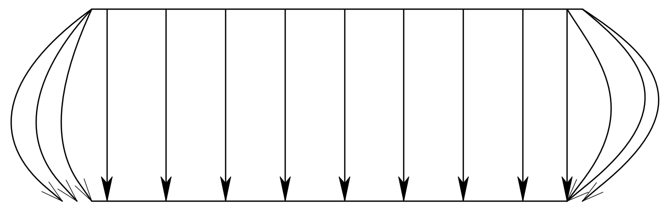
$$C_{gs} \cong \frac{2}{3} C_{ox'}.W.L + C_{gso}.W$$

$$C_{gd} = C_{GDO}.W$$

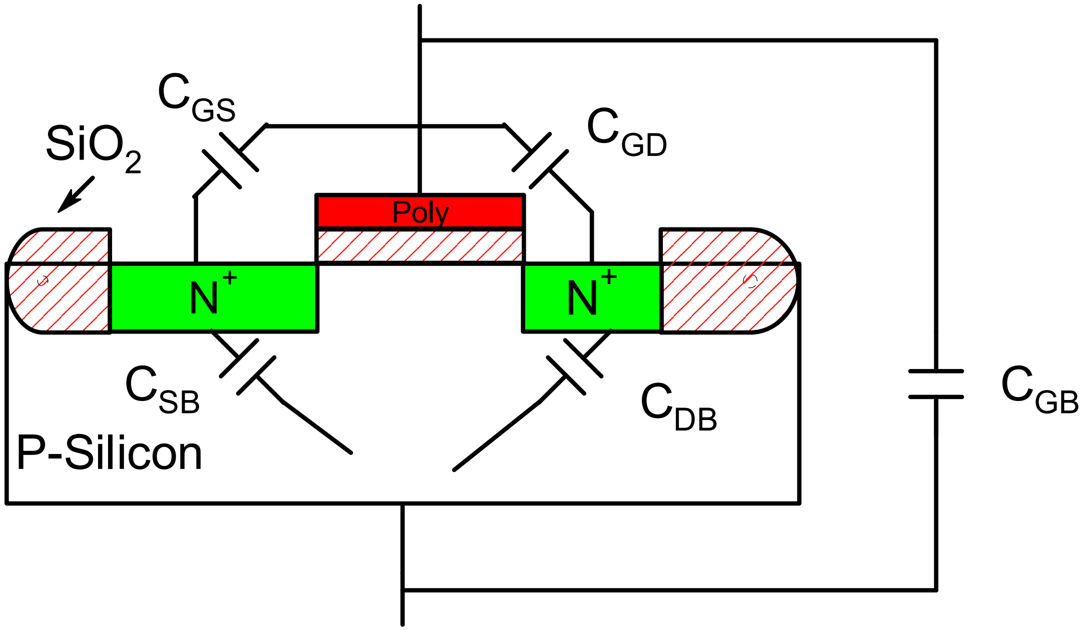


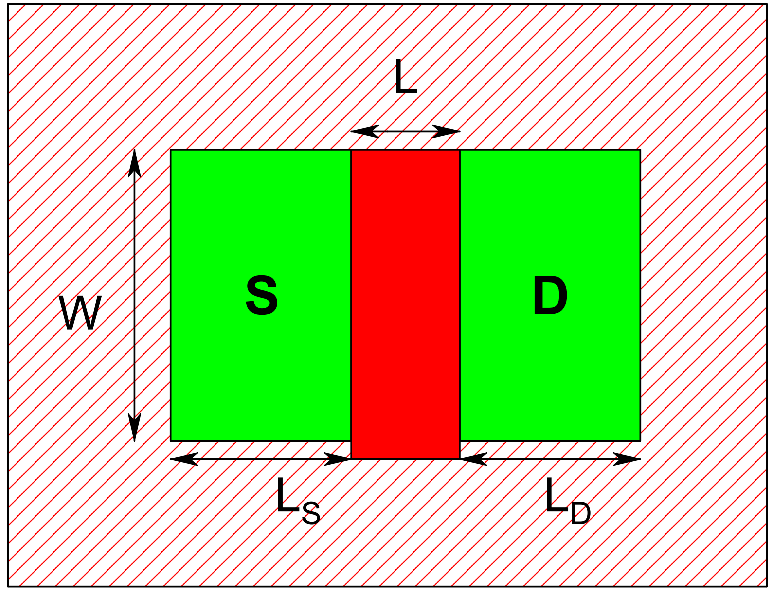
Capacitances: Area and Perimeter Components





$$C = \frac{\varepsilon}{d} \times W \times L + C_p \times (2L + 2W)$$





$$C_{sb} = \frac{C_j . A_s}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} . P_S}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W \quad , \quad A_s = W . L_S$$

A_S = *Area of Source*,

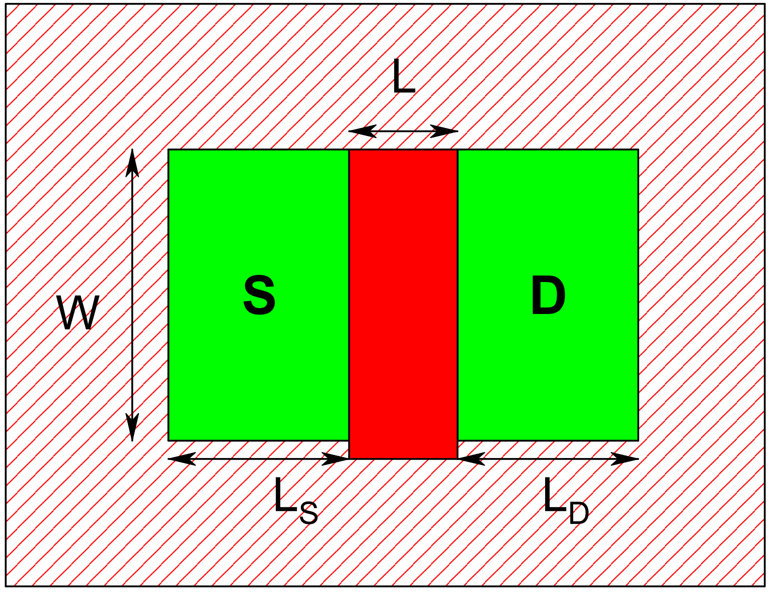
C_j = *Zero bias Capacitance*

P_B = *built-in potential*, M_j = *grading Coefficient*

G-Number

$$C_{db} = \frac{C_{jsw}.P_D}{\left(1+\frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1+\frac{V_{DB}}{P_B}\right)^{M_j}} \qquad P_D = 2L_D + W$$

$$C_{gb} = C_{GBO}.L \sim \text{often negligible}$$



Triode/Linear Region

$$C_{gs} = \frac{1}{2} C_{ox'}.W.L + C_{GSO}.W$$

$$C_{gd} = \frac{1}{2} C_{ox'}.W.L + C_{GDO}.W$$

$$C_{sb} = same\, as\, before$$

$$C_{db} = same\, as\, before$$

$$C_{gb} = same\, as\, before$$

Assuming $V_{DS} \sim 0$

Cutoff Region

$$C_{gs} = C_{GSO}.W$$

$$C_{gd} = C_{GDO}.W$$

$$C_{sb} = same\, as\, before$$

$$C_{db} = same\, as\, before$$

$$C_{gb} = C_{GBO}.L + C_{ox'}.W.L$$

Assuming Tr. is in accumulation

Summary

$$C_{gs} \cong \frac{2}{3} C_{ox'}.W.L + C_{gso}.W \qquad C_{gd} = C_{GDO}.W$$

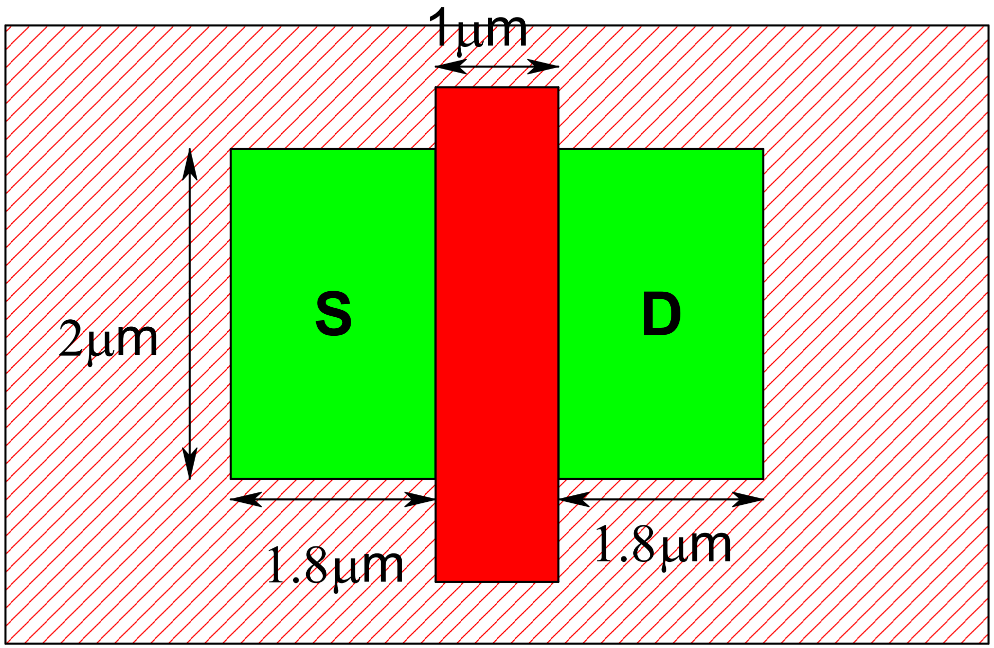
$$C_{sb,bottom} = \frac{C_j.A_s}{\left(1+\frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw}.P_S}{\left(1+\frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W \quad , \quad A_s = W.L_S$$

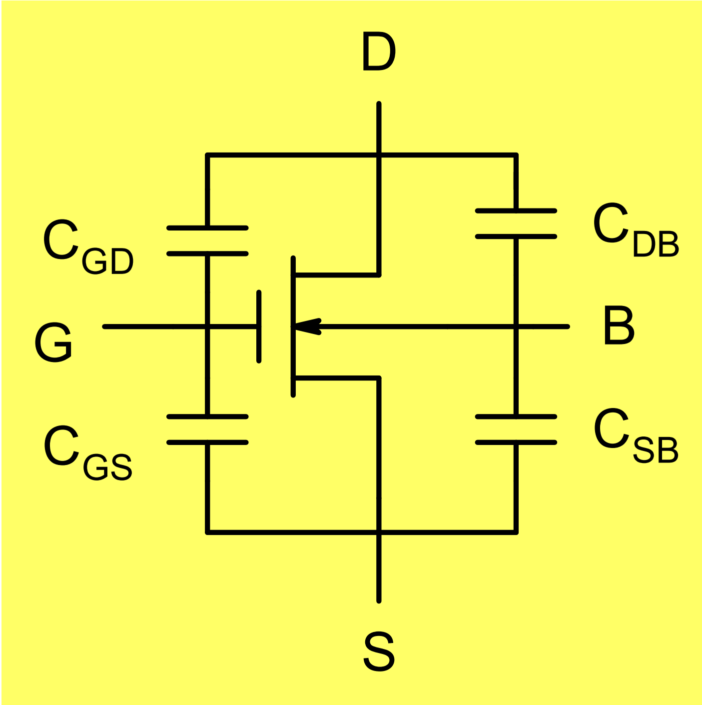
$$C_{db,sidewall} = \frac{C_{jsw}.P_D}{\left(1+\frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1+\frac{V_{DB}}{P_B}\right)^{M_j}} \quad P_D = 2L_D + W$$

The capacitance model presented herein requires 10 parameters:

$$C_{GSO}, C_{GDO}, C_{GBO}, C'_{OX}, C_J, PB, M_J, C_{JSW}, P_{BSW}, M_{JSW}$$

Typical Values of Capacitances

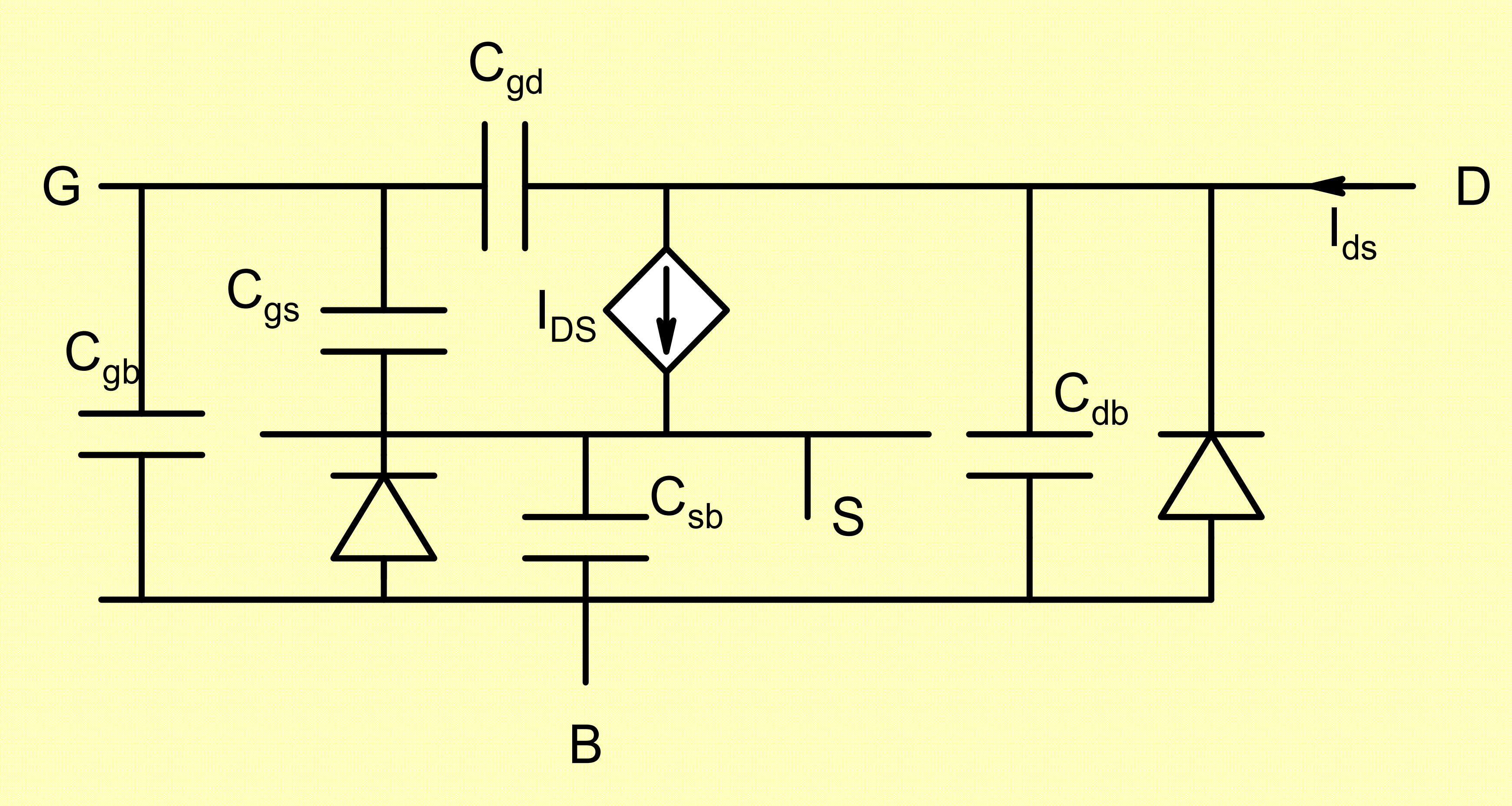




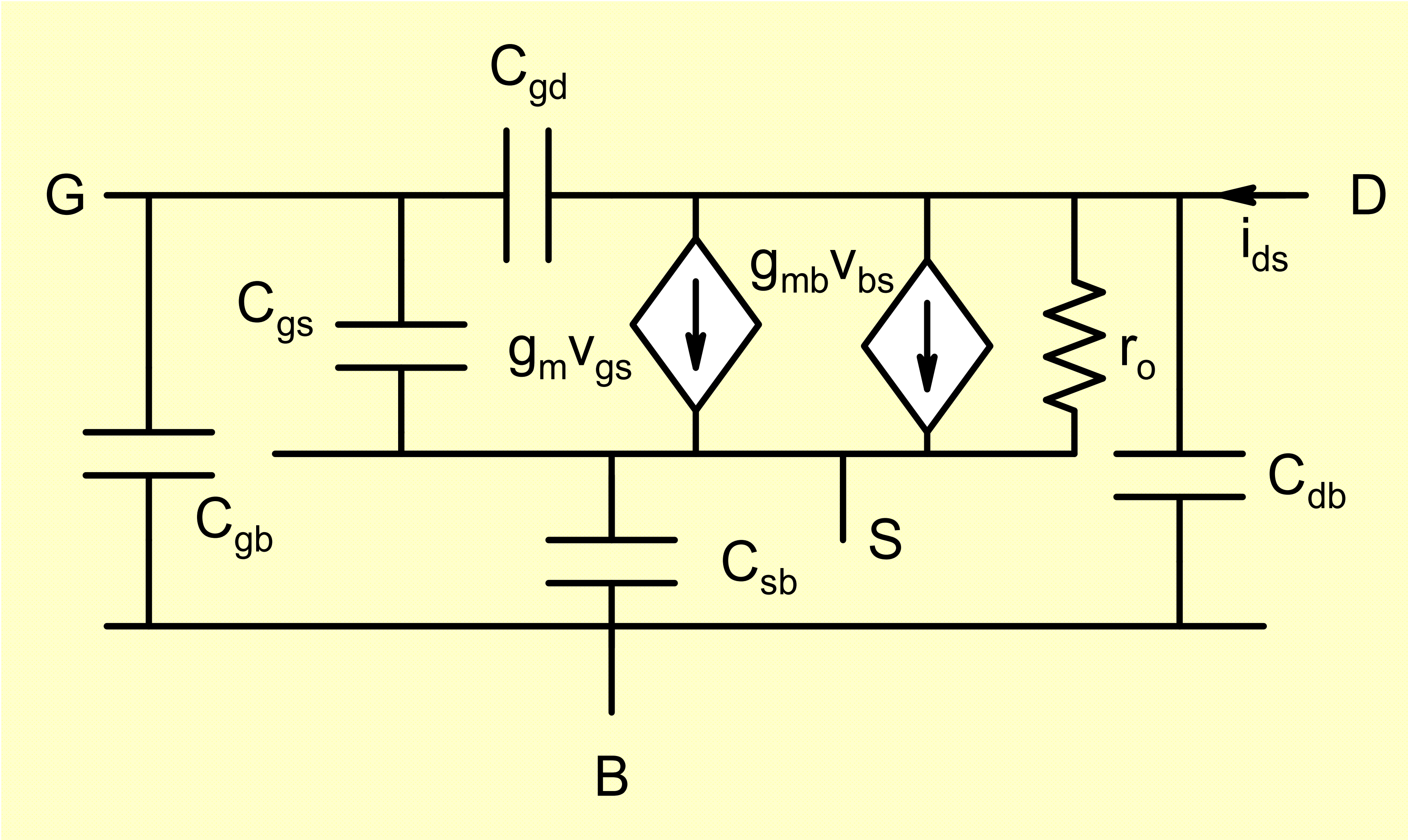
$$C_{gs} = 4.1\,fF\,;\;\; C_{gd} = 0.43\,fF$$
$$C_{sb} = 4.47\,fF$$
$$C_{db} = 2.75\,fF$$

$V_{SB} = 0; \quad V_{DS} = 2V$

Complete Large Signal Model



High Frequency Small Signal Model



- We have so far discussed simple MOS models which are suitable for 'hand-analysis' of circuits. For more accurate prediction of circuit characteristics using circuit simulation more accurate MOS models are required.

- SPICE and its various variants are the most popular circuit simulation tool. In SPICE, there are a number of MOS models that are available including Level-1, level-2, Level-3, BSIM1, BSIM2, BSIM3, BSIM4 etc.

- Level-1 model is the simplest and is basically similar to the large signal model that we have described earlier. A popular model for submicron devices is BSIM3 model.

BSIM3 : Berkeley Short Channel IGFET (Insulated gate Field Effect) Model

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2v_t)}\right) V_{dseff}}{L_{eff}[1 + V_{dseff} / (E_{sat} L_{eff})]}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

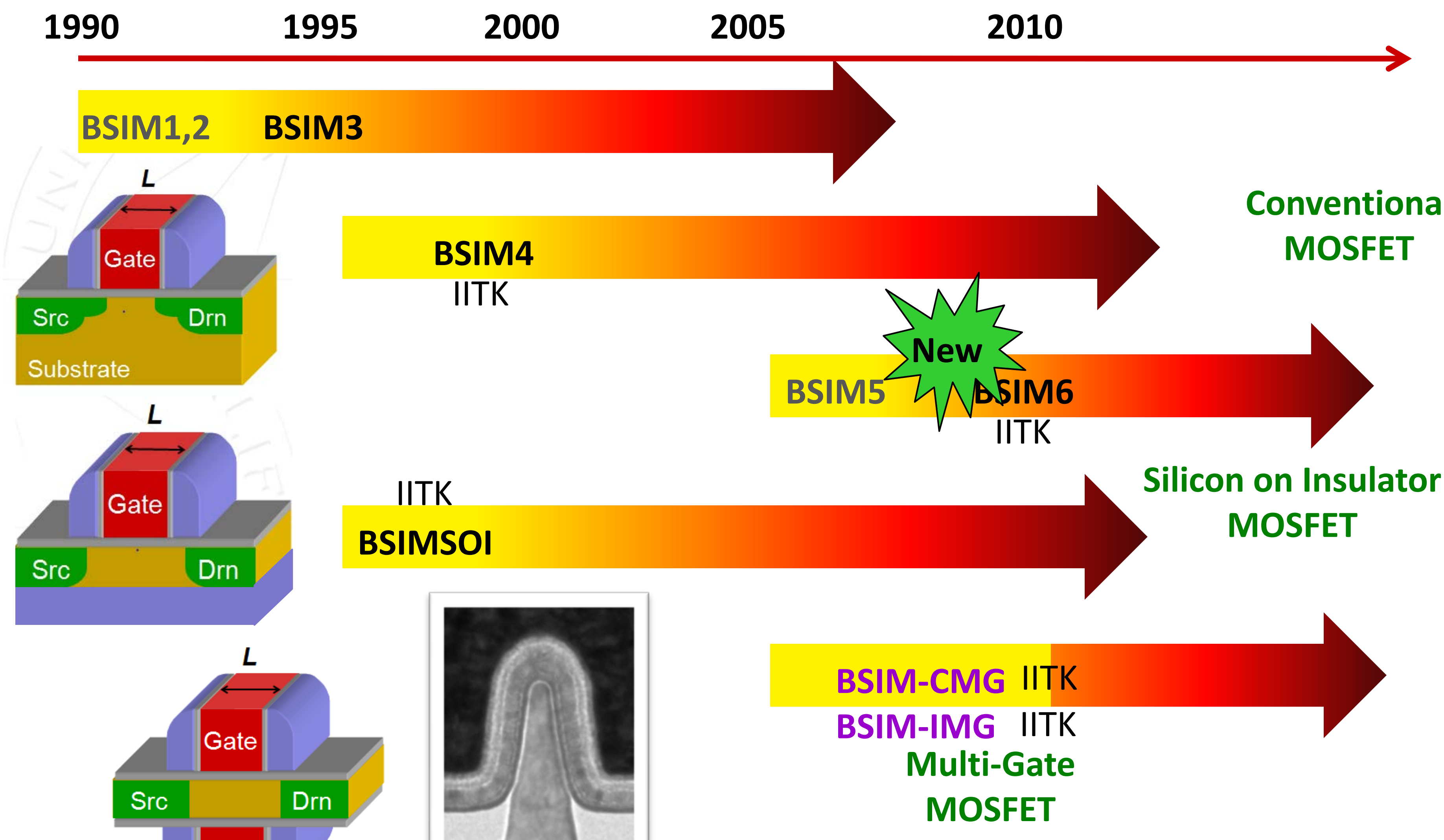
$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat}\, litl} (V_{ds} - V_{dseff})$$

```
MODEL CMOSN NMOS (                                   LEVEL    = 49
+VERSION = 3.1            TNOM     = 27               TOX      = 9.6E-9
+XJ      = 1.5E-7         NCH      = 1.7E17           VTH0     = 0.627652
+K1      = 0.793853       K2       = -0.0306761       K3       = 78.5045537
+K3B     = 0.1300339      W0       = 1E-5             NLX      = 3.89825E-8
+DVT0W   = 0              DVT1W    = 0                DVT2W    = 0
+DVT0    = 6.7330734      DVT1     = 0.8341494        DVT2     = -0.1360511
+U0      = 423.6054862    UA       = 1E-12            UB       = 1.365092E-18
+UC      = 1.078475E-11   VSAT     = 1.236292E5       A0       = 0.9417794
+AGS     = 0.1494531      B0       = 1.565313E-6      B1       = 5E-6
+KETA    = 2.243159E-3    A1       = 0                A2       = 1
+RDSW    = 1.153603E3     PRWG     = 0.0653342        PRWB     = -0.0681133
+WR      = 1              WINT     = 2.329652E-7      LINT     = 1.00611E-7
+XL      = -1E-7          XW       = 0                DWG      = -4.464259E-9
+DWB     = 1.245396E-8    VOFF     = -0.0580692       NFACTOR  = 1.4823566
+CIT     = 0              CDSC     = 2.4E-4           CDSCD    = 0
+CDSCB   = 0              ETA0     = 0.043042         ETAB     = -5.942602E-3
+DSUB    = 0.4388988      PCLM     = 0.6404859        PDIBLC1  = 1.514861E-7
+PDIBLC2 = 3.246207E-3    PDIBLCB  = -0.197801        DROUT    = 1.551814E-3
+PSCBE1  = 5.680232E9     PSCBE2   = 1.369852E-9      PVAG     = 0.0306927
+DELTA   = 0.01           RSH      = 2.8              MOBMOD   = 1
+PRT     = 0              UTE      = -1.5             KT1      = -0.11
+KT1L    = 0              KT2      = 0.022            UA1      = 4.31E-9
+UB1     = -7.61E-18      UC1      = -5.6E-11         AT       = 3.3E4
+WL      = 0              WLN      = 1                WW       = 0
+WWN     = 1              WWL      = 0                LL       = 0
+LLN     = 1              LW       = 0                LWN      = 1
+LWL     = 0              CAPMOD   = 2                XPART    = 0.5
+CGDO    = 2.81E-10       CGSO     = 2.81E-10         CGBO     = 1E-9
+CJ      = 5.04643E-4     PB       = 0.99             MJ       = 0.8099425
+CJSW    = 4.814417E-10   PBSW     = 0.99             MJSW     = 0.1
+CJSWG   = 2.2346E-10     PBSWG    = 0.99             MJSWG    = 0.1
+CF      = 0              PVTH0    = 9.036446E-3      PRDSW    = -22.8038789
+PK2     = 0.0105156      WKETA    = -3.709225E-3     LKETA    = -8.524366E-3
+PAGS    = 0.0968          )
```

```
MODEL CMOSP PMOS (                                LEVEL    = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 9.6E-9
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.8351513
+K1      = 0.3832927      K2      = 0.0182059      K3      = 93.9598487
+K3B     = -5             W0      = 1E-5           NLX     = 2.041534E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 3.7095566      DVT1    = 0.5091225      DVT2    = -0.0368146
+U0      = 181.6646706    UA      = 1.338606E-9    UB      = 1.002605E-18
+UC      = -5.64742E-11   VSAT    = 2.234764E5     A0      = 0.9423567
+AGS     = 0.2743733      B0      = 4.198245E-6    B1      = 5E-6
+KETA    = 3.411785E-3    A1      = 0              A2      = 1
+RDSW    = 3.5E3          PRWG    = -0.0704989     PRWB    = 5.293994E-3
+WR      = 1              WINT    = 2.285806E-7    LINT    = 6.239413E-8
+XL      = -1E-7          XW      = 0              DWG     = -1.628171E-8
+DWB     = 9.20495E-9     VOFF    = -0.0914053     NFACTOR = 0.9483204
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.0364279      ETAB    = 3.484825E-3
+DSUB    = 0.2648828      PCLM    = 4.0562705      PDIBLC1 = 1.366583E-6
+PDIBLC2 = 6.468762E-3    PDIBLCB = -0.0188204     DROUT   = 0
+PSCBE1  = 5.65221E9      PSCBE2  = 5.685284E-10   PVAG    = 13.2742869
+DELTA   = 0.01           RSH     = 2.3            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.52E-10       CGSO    = 2.52E-10       CGBO    = 1E-9
+CJ      = 9.379142E-4    PB      = 0.9348647      MJ      = 0.4765513
+CJSW    = 1.279151E-10   PBSW    = 0.99           MJSW    = 0.1303972
+CJSWG   = 4.256E-11      PBSWG   = 0.99           MJSWG   = 0.1303972
+CF      = 0              PVTH0   = -1.076201E-3   PRDSW   = 282.4948778
+PK2     = 3.181465E-3    WKETA   = 7.931059E-3    LKETA   = -9.663719E-3
+PAGS    = 0.09532         )
```

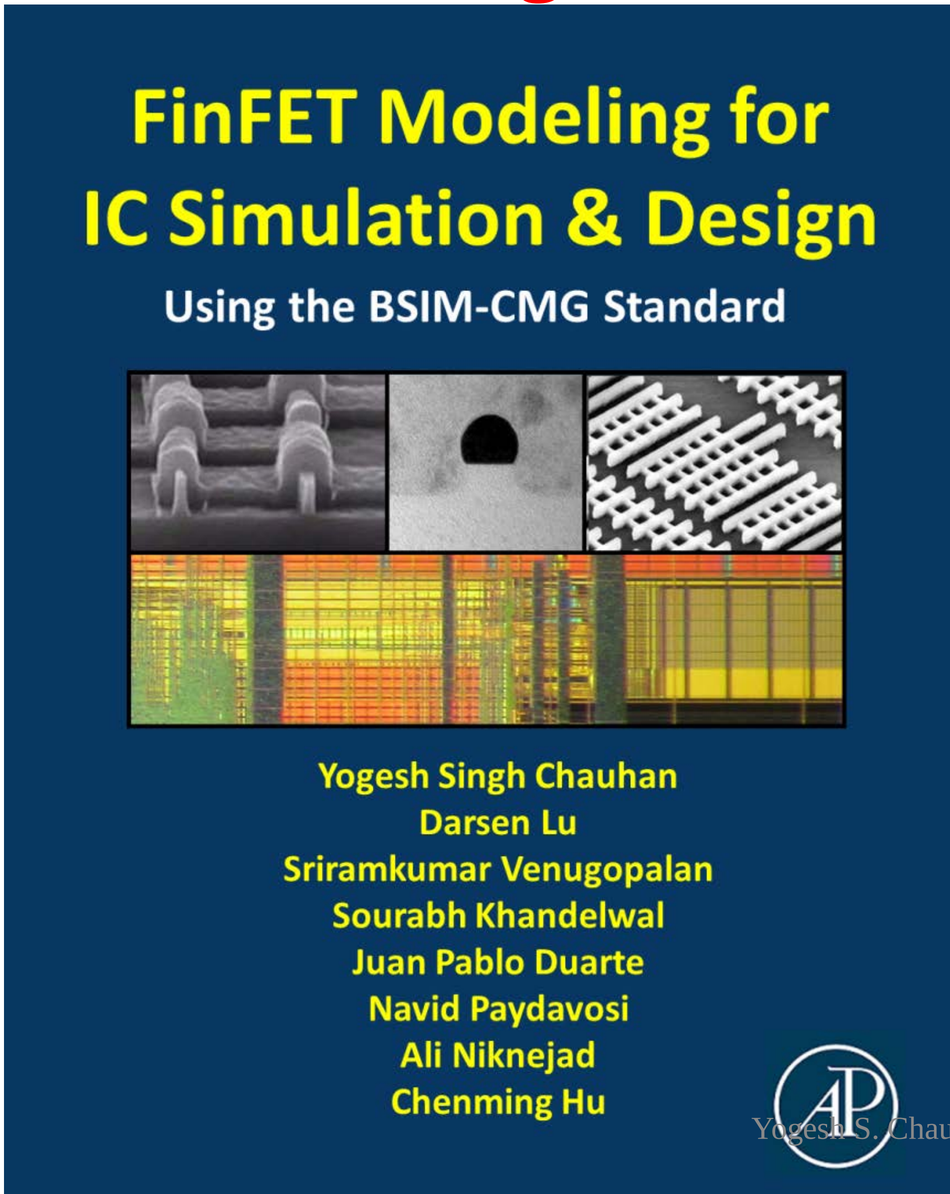
G-Number

BSIM Family of Compact Device Models



BSIM: Berkeley Short-channel IGFET Model

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

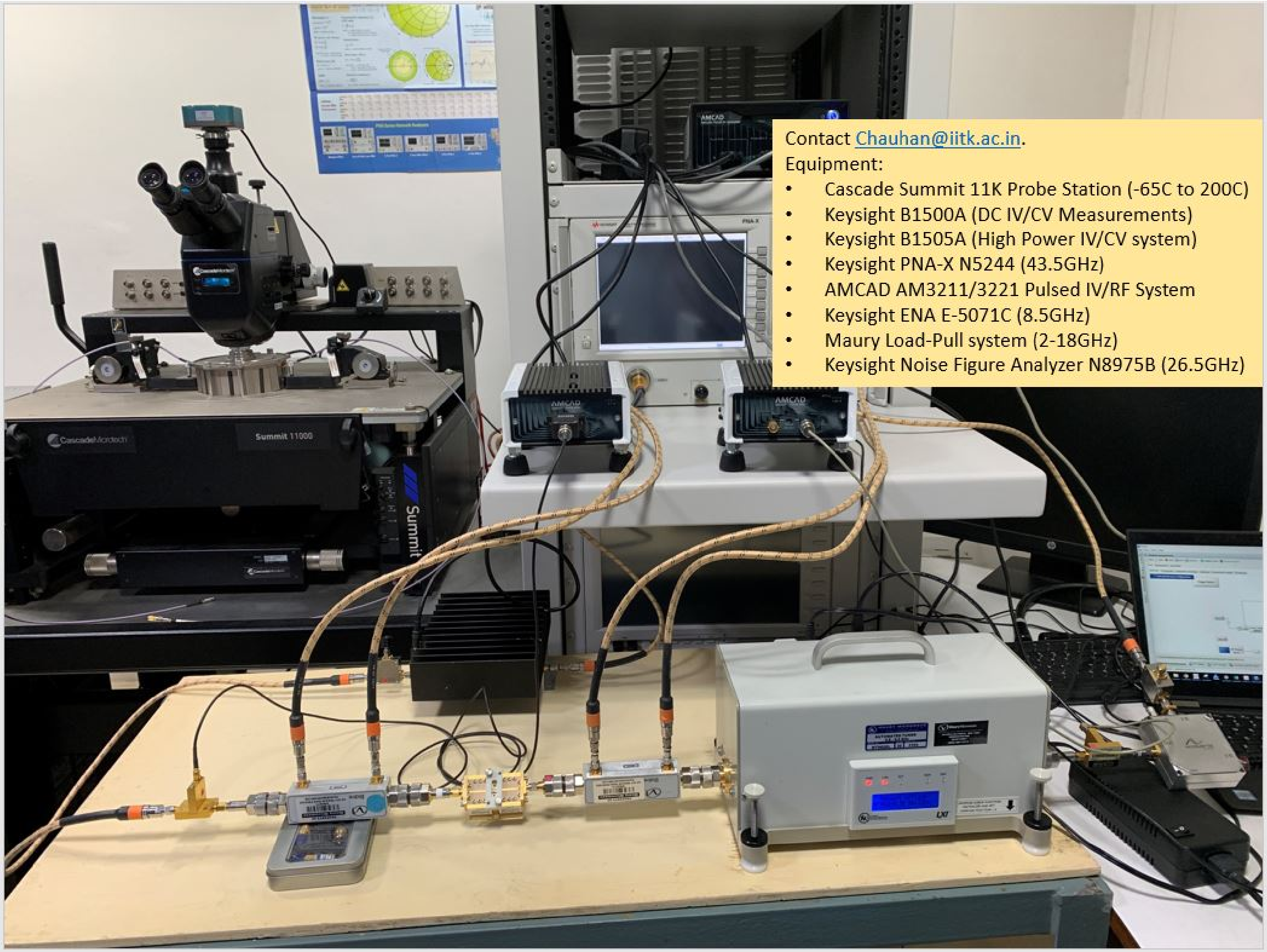


Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

IIT Kanpur's Nanolab

Developing Industry Standard SPICE Models for Semiconductor Industry

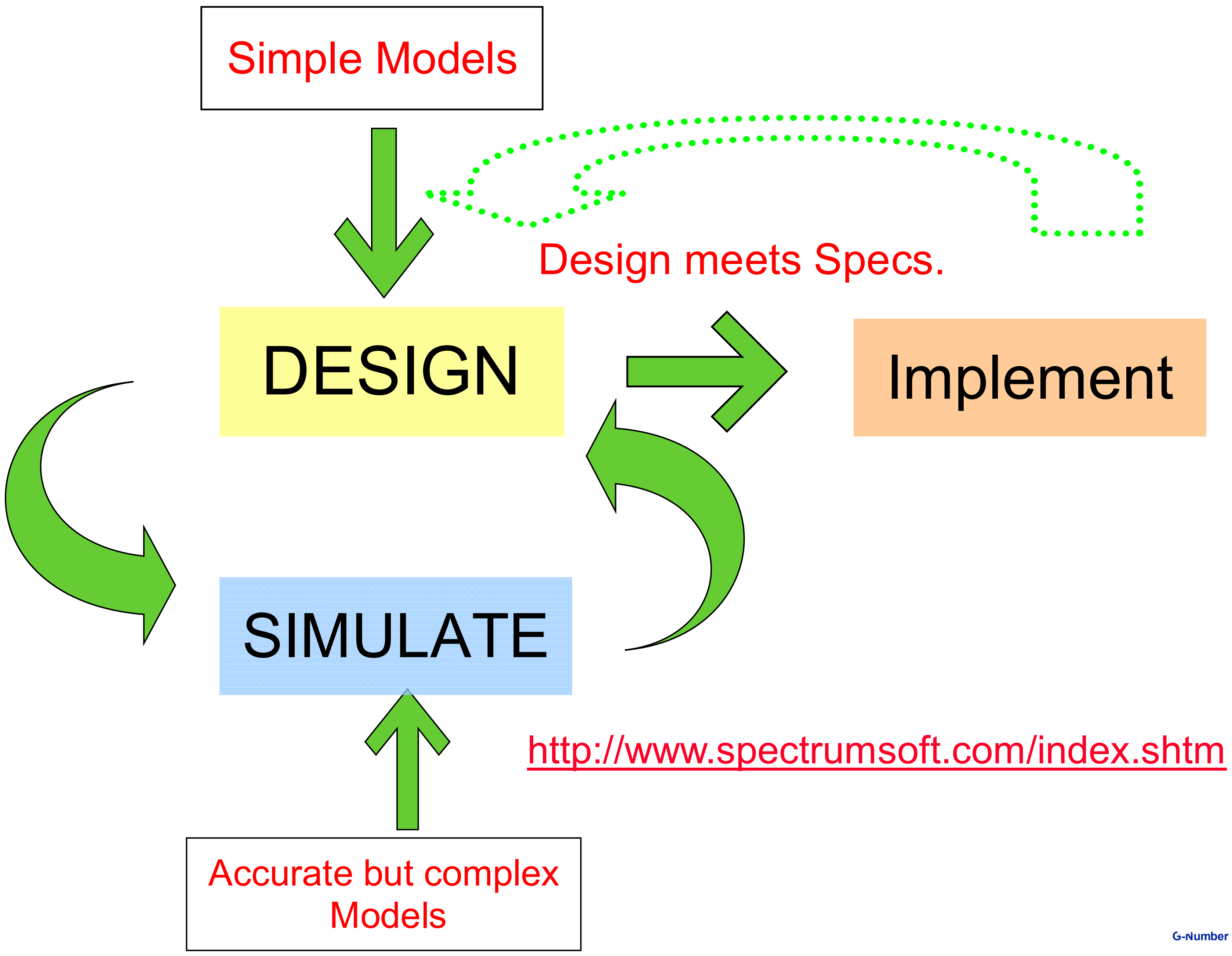


Contact Chauhan@iitk.ac.in.

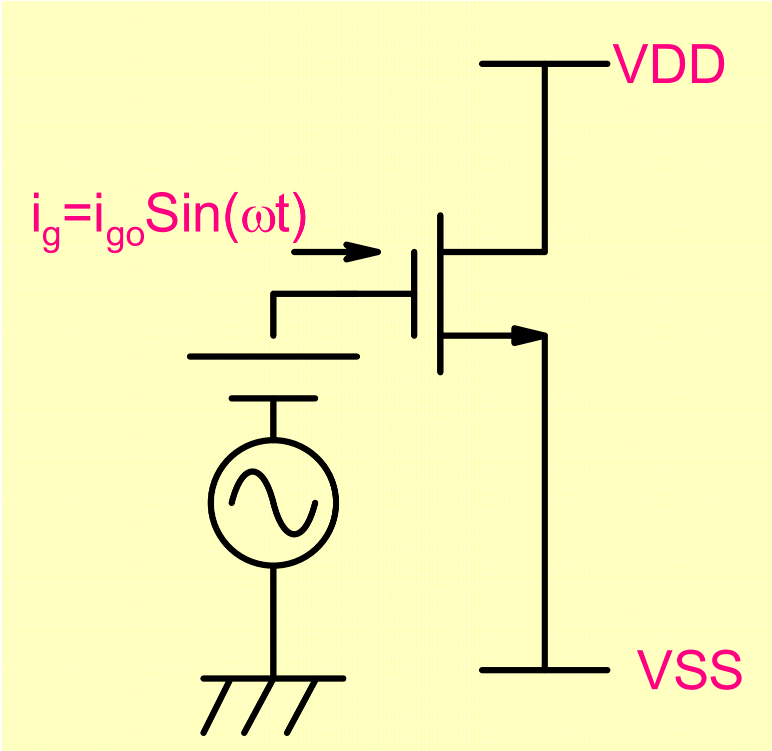
Equipment:

- Cascade Summit 11K Probe Station (-65C to 200C)
- Keysight B1500A (DC IV/CV Measurements)
- Keysight B1505A (High Power IV/CV system)
- Keysight PNA-X N5244 (43.5GHz)
- AMCAD AM3211/3221 Pulsed IV/RF System
- Keysight ENA E-5071C (8.5GHz)
- Maury Load-Pull system (2-18GHz)
- Keysight Noise Figure Analyzer N8975B (26.5GHz)

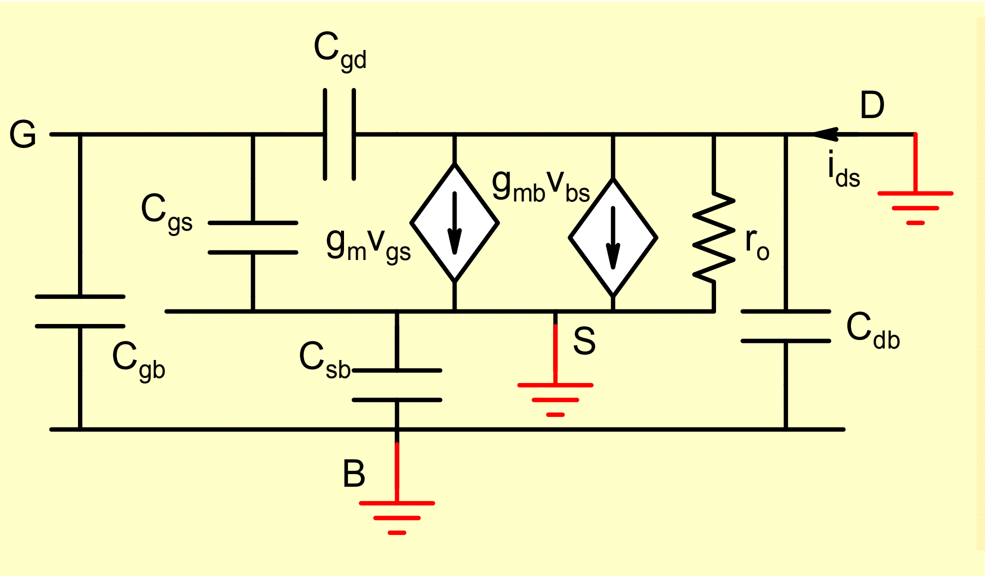
Role of simple model in design cycle

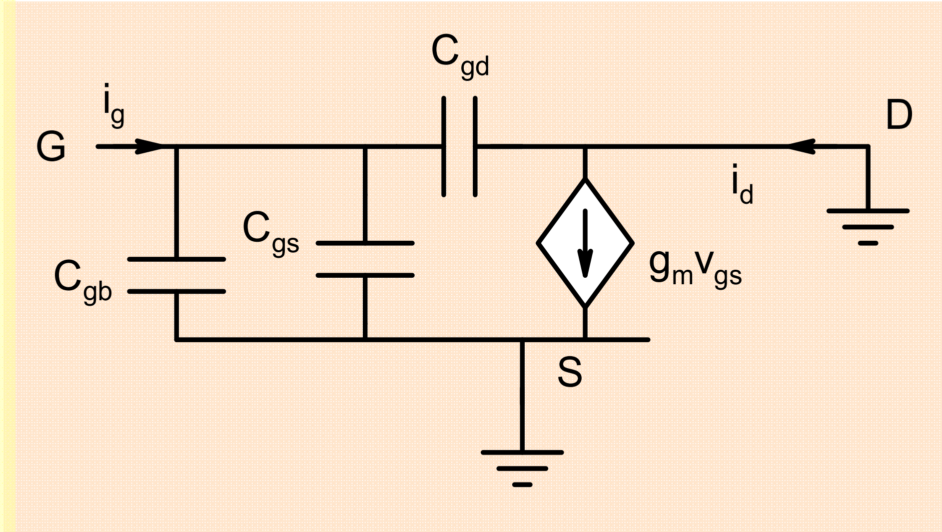


Unity Gain Frequency



Frequency at which current gain $\left.\dfrac{i_d}{i_g}\right|_{v_{sb}=0;v_{ds}=0} = 1$





$$i_g = j\omega(C_{gs} + C_{gd} + C_{gb})v_g$$

$$i_d \cong g_m v_{gs}$$

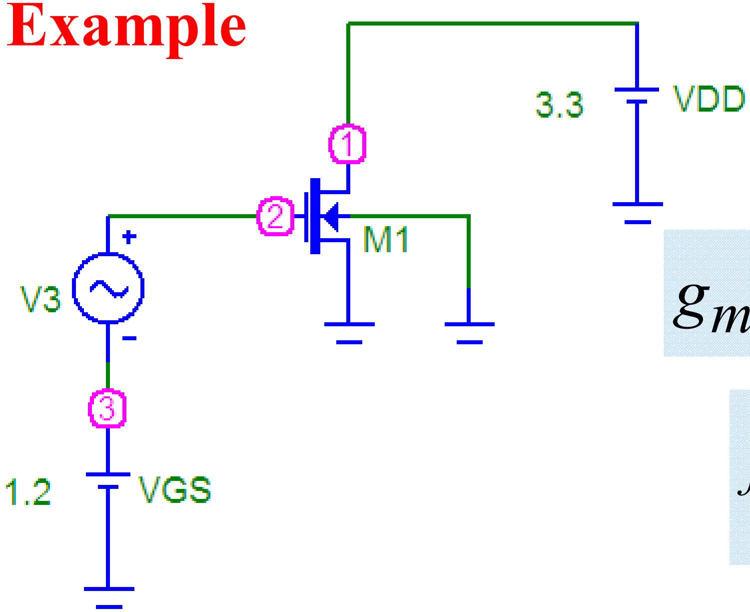
$$\frac{i_d}{i_g} = \frac{g_m}{j\omega(C_{gs} + C_{gd} + C_{gb})}$$

$$\frac{g_m}{\omega_T(C_{gs} + C_{gd} + C_{gb})} = 1$$

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd} + C_{gb}}$$

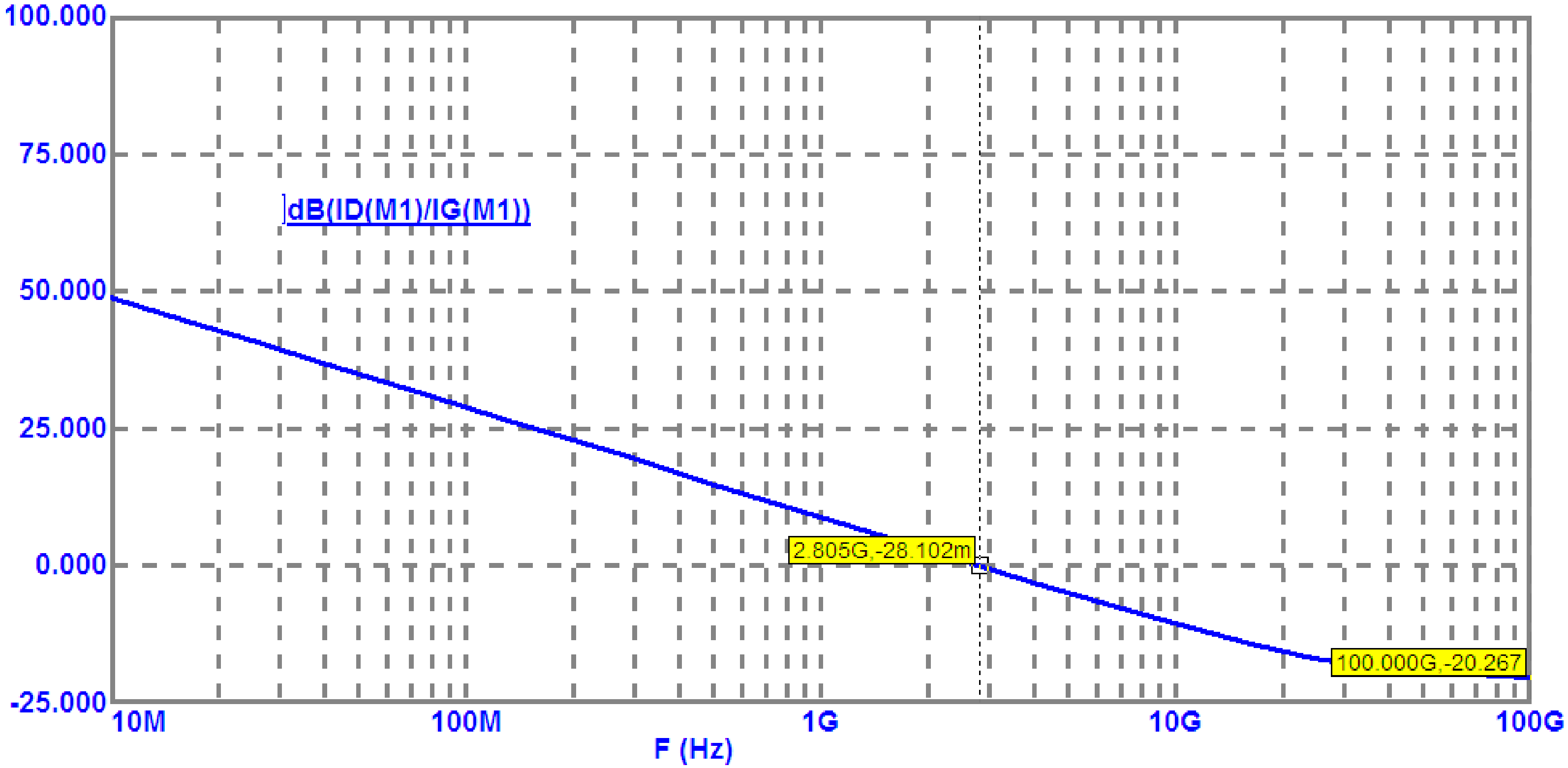
$$f_T \cong \frac{g_m}{2\pi C_{gs}} = \frac{1}{2\pi} \times \frac{\mu_N}{L^2} \times (V_{GSQ} - V_{THN})$$

Example



$$g_m = 8.1\times10^{-5}\,\square\ ; C_{gs} = 4.1\,fF;\ C_{gd} = 0.43\,fF$$

$$f_T = \frac{1}{2\pi}\times\frac{g_m}{C_{gs}+C_{gd}+C_{gb}} = 2.8GHz$$



G-Number