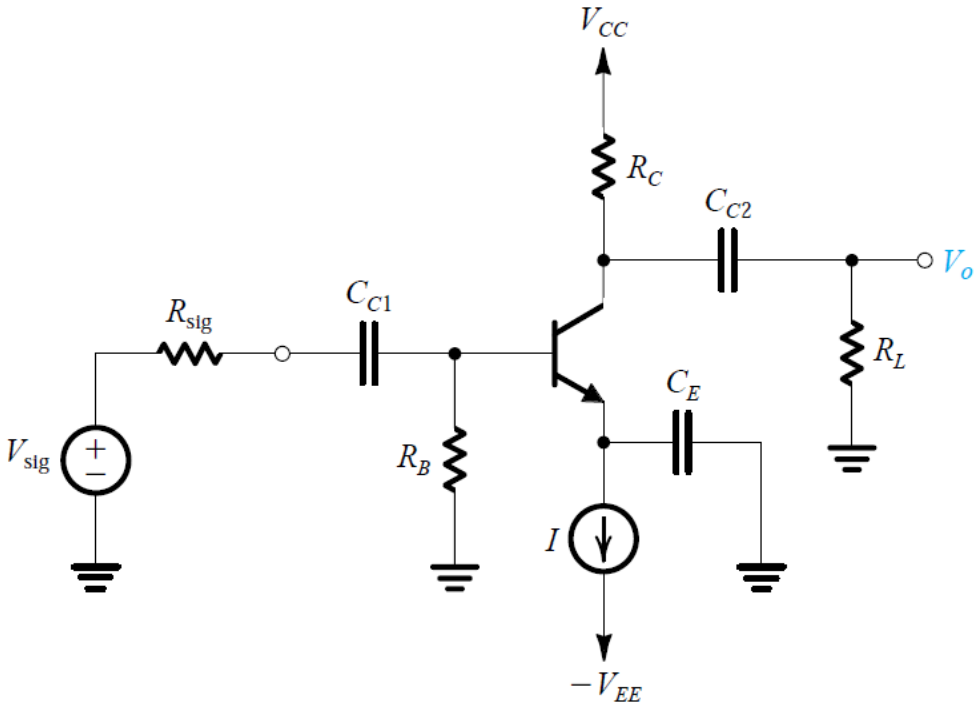
EE210: HW-7 Extra Problems

Date: 14.02.2019

Q.1 Determine appropriate capacitance values for C_{C1}, C_{C2}, and C_E for the common-emitter amplifier to have f_L = 100 Hz. Given: R_B = 100 kΩ, R_C = 8 kΩ, R_L = 5 kΩ, R_{sig} = 5 kΩ, β = 100, g_m = 40 mA/V, and r_π = 2.5 kΩ. [From Sedra & Smith]



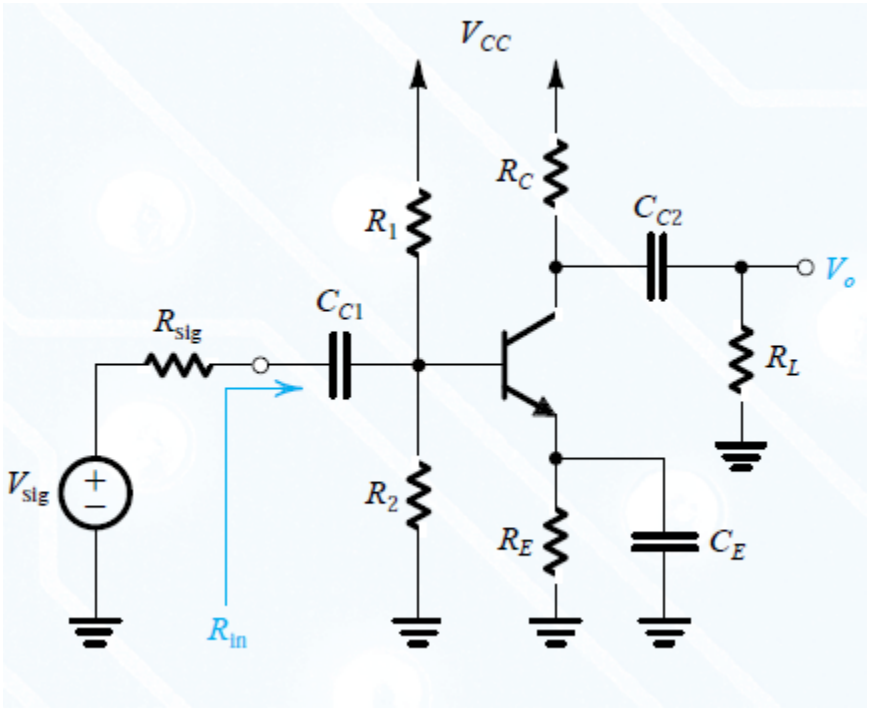
Q.2 A common-emitter amplifier shown above has C_{C1} = C_E = C_{C2} = 1 μF, R_B = 100 kΩ, R_{sig} = 5 kΩ, g_m = 40 mA/V, r_π = 2.5 kΩ, R_C = 8 kΩ, and R_L = 5 kΩ. Determine cutoff frequency from each capacitor and then estimate f_L. [From Sedra & Smith]

Q.3 Repeat Q.2 for the situation in which C_E = 50 μF and C_{C1} = C_{C2} = 2μF. Find the three break frequencies and estimate f_L. [From Sedra & Smith]

Q.4 Repeat Q.1 for a related CE amplifier whose supply voltages and bias current are each reduced to half of their original value but R_B, R_C, R_{sig}, and R_L are left unchanged. Find C_{C1}, C_{C2}, C_E and for f_L = 100 Hz. Minimize the total capacitance used, under the following conditions. Arrange that the contributions of C_E, C_{C1}, and C_{C2} are 80%, 10%, and 10%, respectively. Specify capacitors to two significant digits, choosing the next highest value (in general, for a conservative design), but realizing that for C_E, this may represent a larger capacitance increment. Check the value of f_L that results. [From Sedra & Smith]

[Note: An attractive approach can be to select on the small side, allowing it to contribute more than 80% to f_L, while making C_{C1} and C_{C2} larger, since they must contribute less to f_L.)

Q.5 Consider the common-emitter amplifier shown below under the following conditions: R_{sig} = 5 kΩ, R_1 = 33 kΩ, R_2 = 22 kΩ, R_E = 3.9 kΩ, R_C = 4.7 kΩ, R_L = 5.6 kΩ, V_{CC} = 5 V. The dc emitter current can be shown to be $I_E \cong 0.3$ mA, at which β = 120. Find the input resistance R_{in} and the mid-band voltage gain. If $C_{C1} = C_{C2}$ = 1 μF and C_E = 20 μF, find the three cutoff frequencies f_{P1}, f_{P2}, and f_{P3} and an estimate for f_L.



Q.6 For the amplifier described in Q.5, design the coupling and bypass capacitors for a lower 3-dB frequency of 100 Hz. Design so that the contribution of each of C_{C1} and C_{C2} to determining f_L is only 5%.