EE210: Microelectronics-I

Lecture-21 :CE Amplifier-9

Design Perspective

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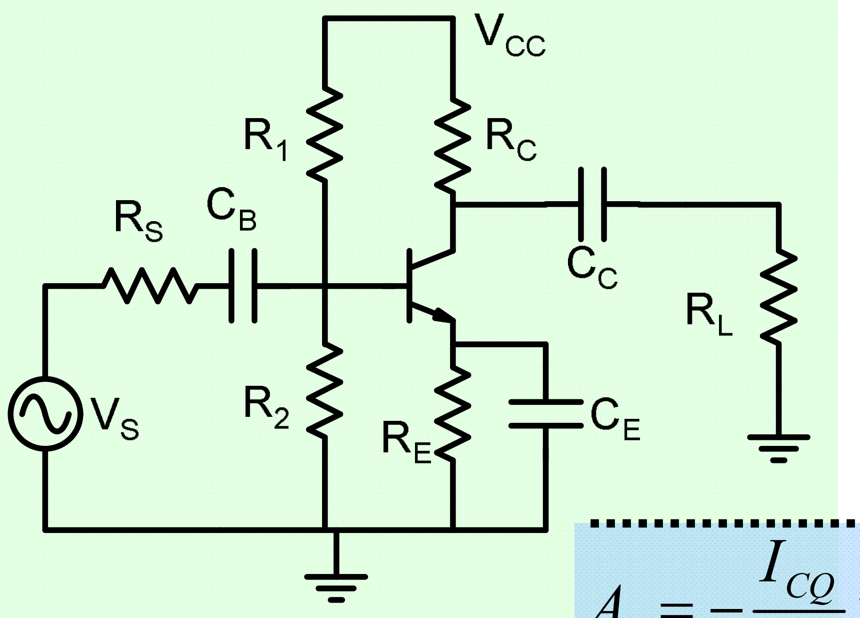
CE Amplifier

Summary



$$I_{CQ} = \frac{V_{CC}\dfrac{R_2}{R_1+R_2} - V_{BE}(on)}{\dfrac{R_B}{\beta} + R_E}; R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{CC} = V_{CEQ} + I_{CQ}(R_C + R_E)$$

$$S = \frac{\Delta I_{CQ}/I_{CQ}}{\Delta\beta/\beta} = \frac{1}{1+\dfrac{\beta R_E}{R_B}}; \quad x_b = \frac{R_B}{r_\pi}$$

$$A_V = -\frac{I_{CQ}}{V_T} \times R_C \| R_L$$

$$R_{in} = r_\pi \| R_B$$

$$R_o = R_C$$

$$\omega_L = \frac{1}{C_E \times \left(R_E \left\| \dfrac{(R_S \| R_B) + r_\pi}{\beta}\right.\right)}$$

$$V_{om} = Min.\left\{(V_{CEQ} - V_{CEsat.}), \frac{H_{D2}}{25} \times I_{CQ} R_C \| R_L\right\}$$

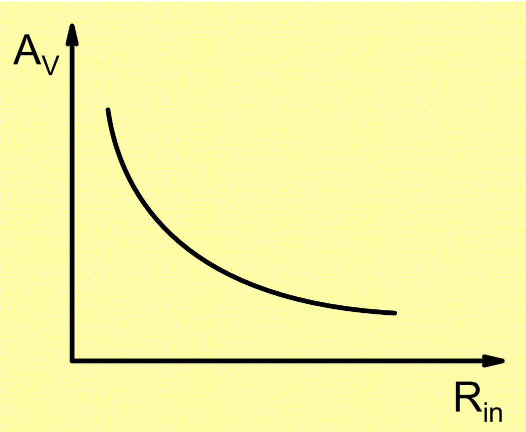
$$\omega_H \cong \frac{1}{\left(\left(R_S \| R_B\right) + r_{bb}\right) \| r_\pi \{C_\pi + C_\mu(1 + g_m R_C \| R_L)\} + C_\mu R_C \| R_L}$$

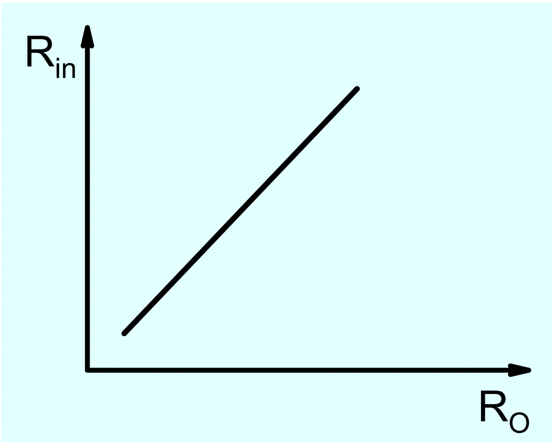
Tradeoff between Voltage Gain, Input Resistance and Output Resistance

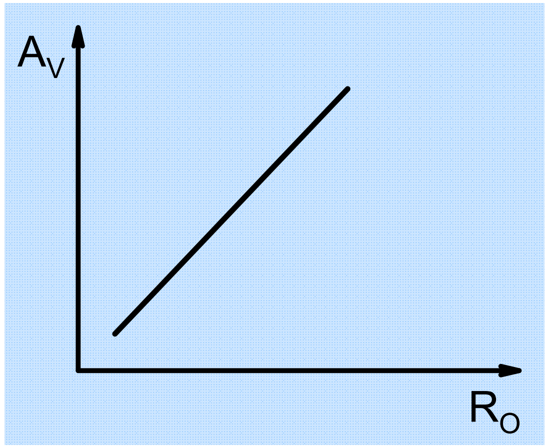
$$A_V = -\frac{I_{CQ}}{V_T} \times R_C \| R_L$$

$$R_{in} = r_\pi \| R_B$$

$$R_o = R_C$$



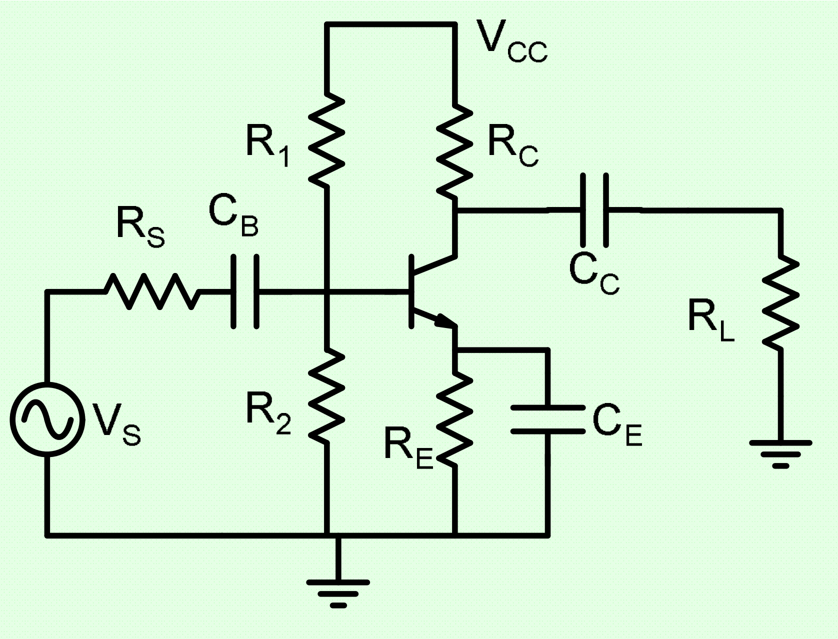


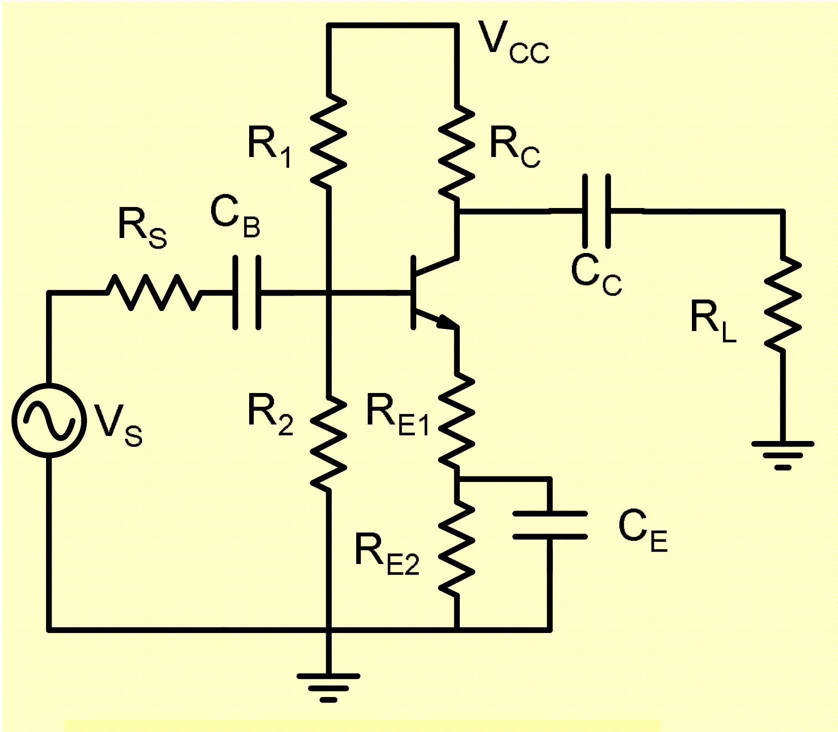


$$\frac{A_V \times R_{in}}{R_O} = \beta \times \frac{1}{1 + \frac{R_o}{R_L}} \times \frac{1}{1 + \frac{r_\pi}{R_B}}$$

$$\frac{A_V \times R_{in}}{R_O} \leq \beta$$

Gain-Input resistance Tradeoff



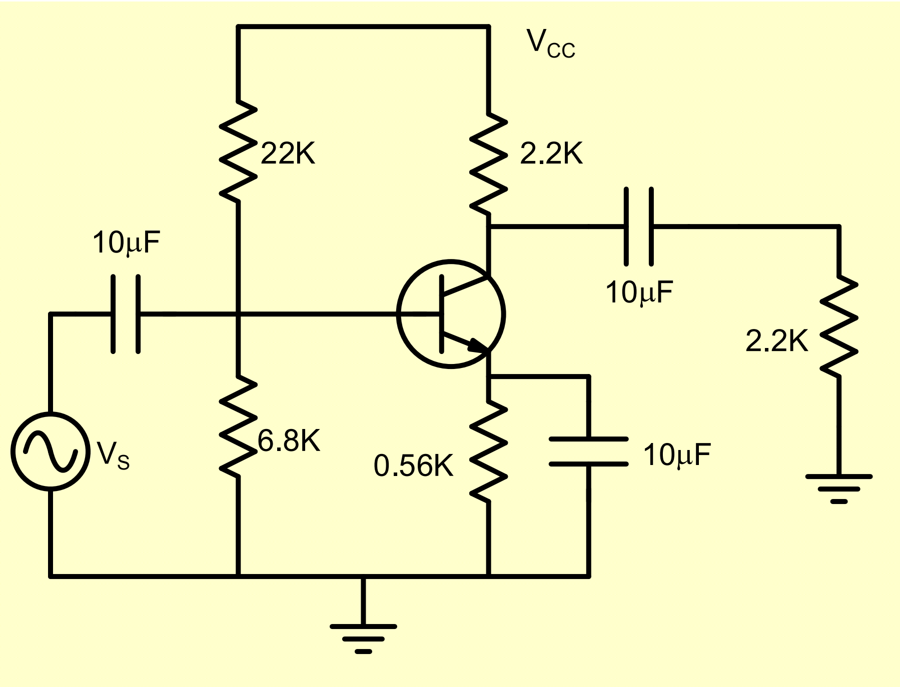


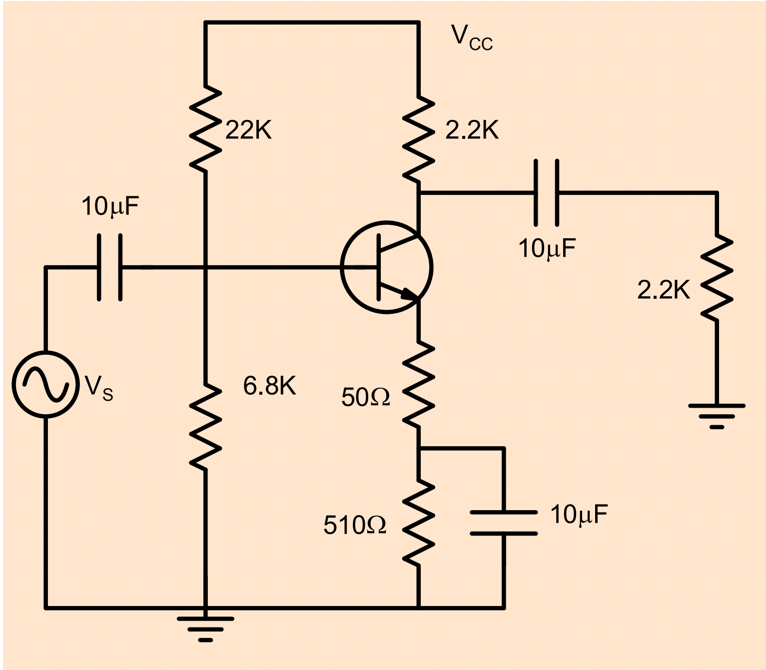
$$A_V = -g_m \times R_C \| R_L$$

$$R_{in} = r_\pi \| R_B$$

$$A_V = -\frac{g_m}{1 + g_m R_{E1}} \times R_C \| R_L$$

$$R_{in} = r_\pi \times (1 + g_m R_{E1}) \| R_B$$





$$\beta = 100; V_{CC} = 12V$$

$$I_{CQ} = 3.4mA; V_{CEQ} = 2.57V$$

$$A_V = 110.7; R_{in} = 0.82K \; ; R_O = 2.2K$$

$$v_{om} = 0.39V \,@\, THD = 1.9\%$$

$$f_L = 1.67kHz; f_H = 5.8MHz$$

$$\beta = 100$$

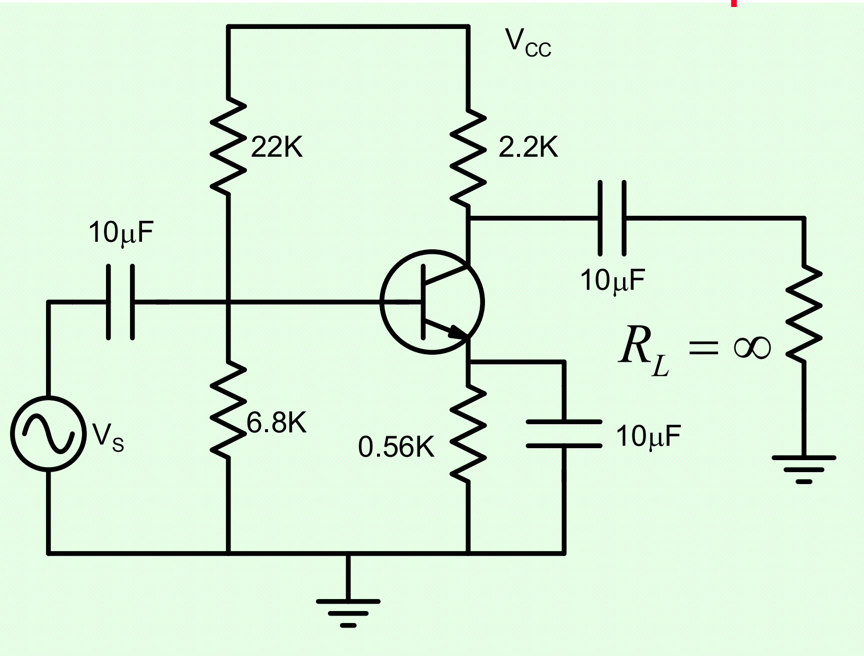
$$I_{CQ} = 3.4mA; V_{CEQ} = 2.57V$$

$$A_V = 18.2; R_{in} = 2.76K \; ; R_O = 2.2K$$

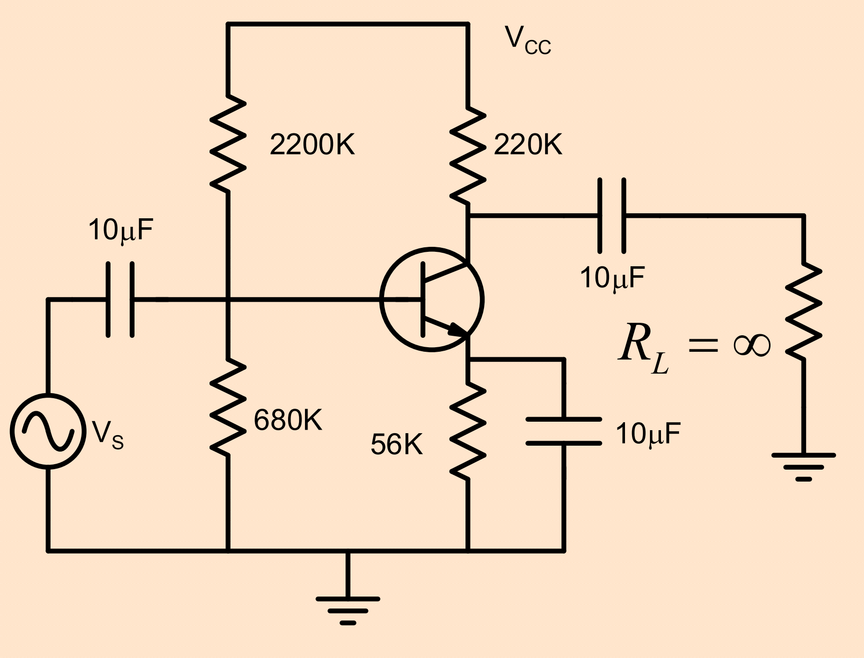
$$v_{om} = 2V \,@\, THD = 1.8\%$$

$$f_L = 0.3kHz; f_H = 26.46MHz$$

Characteristics of CE amplifier



$$A_V = 232; R_{in} = 0.8K \ ; R_O = 2.2K$$



$$A_V = 283.5; R_{in} = 64K \ ; R_O = 220K$$

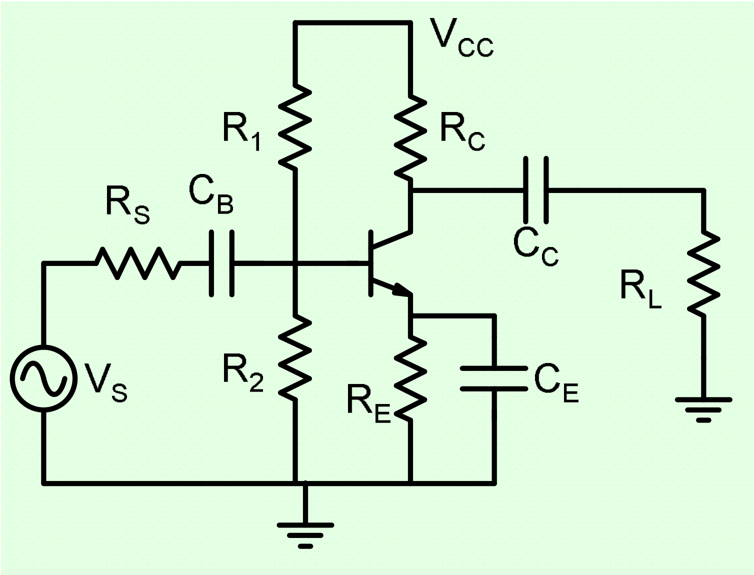
Parameter	Voltage Gain	Input Resistance	Output Resistance
Value	High	Medium	Medium

Parameter	Voltage Gain	Input Resistance	Output Resistance
Value	High	High	High

$$\frac{A_V \times R_{in}}{R_O} \leq \beta$$

G-Number

Gain-Swing Tradeoff



$$A_V = -\frac{I_{CQ}}{V_T} \times R_C \| R_L$$

$$V_{om} = Min.\left\{ (V_{CEQ} - V_{CEsat.}), \frac{H_{D2}}{25} \times I_{CQ} R_C \| R_L \right\}$$

$$V_{om} = Min.\left\{ (V_{CEQ} - V_{CEsat.}), \frac{H_{D2}}{25} \times |A_V| \times V_T \right\}$$

$$v_{om} = 0.5V \Rightarrow V_{CEQ} \geq 0.7V$$

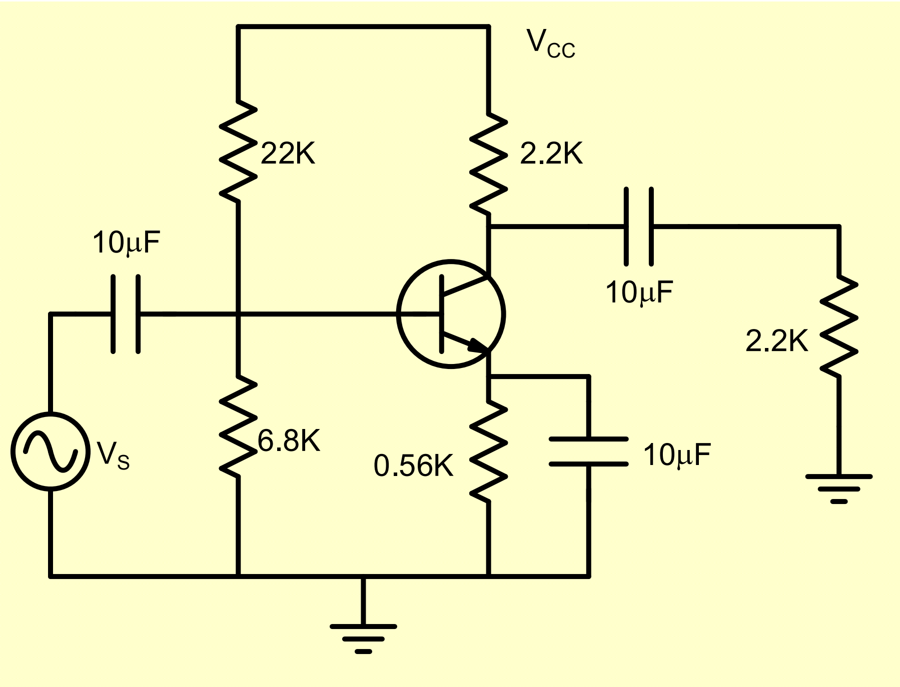
$$\Rightarrow I_{CQ} R_C \leq V_{CC} - 0.7 - V_E$$

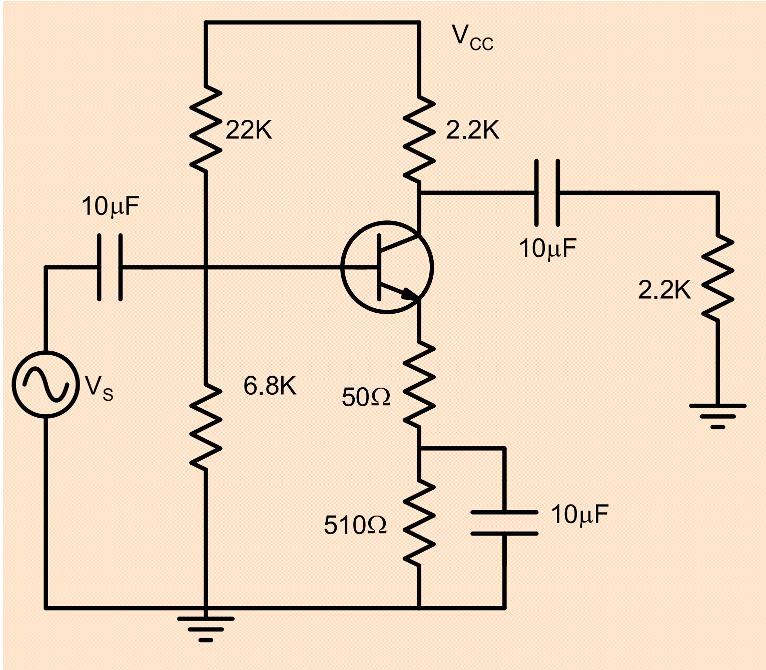
$$v_{om} = 3V \Rightarrow V_{CEQ} \geq 3.2V$$

$$\Rightarrow I_{CQ} R_C \leq V_{CC} - 3.2 - V_E$$

For a fixed V_{CC}, increase in swing decreases gain

Gain-Swing Tradeoff





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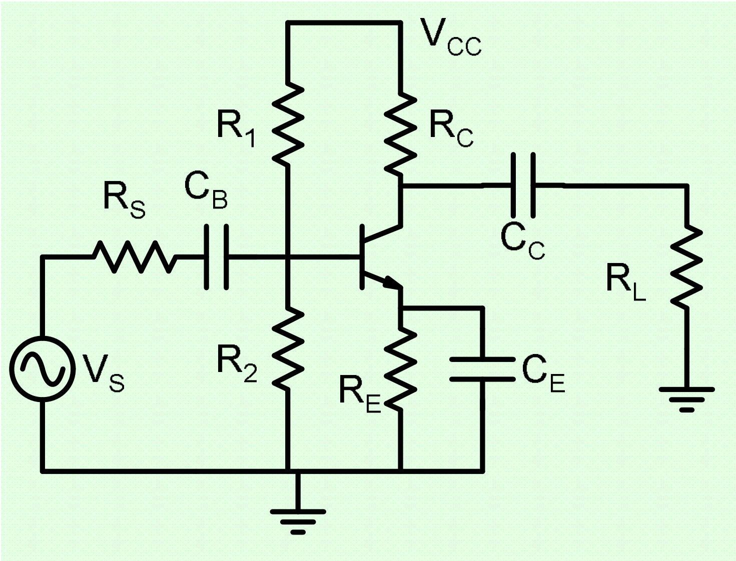
G-Number

Gain-Bandwidth Tradeoff



Lower Cutoff Frequency

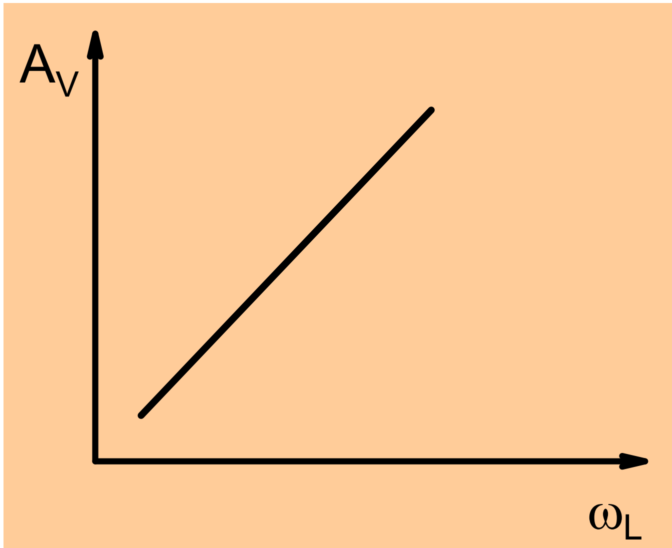
$$\omega_L = \frac{1}{C_E \times \left(R_E \middle\| \frac{(R_S \| R_B) + r_\pi}{\beta}\right)} \cong \frac{\beta}{C_E \times r_\pi}$$

$$\omega_L \times R_{in} = \frac{\beta}{C_E}$$

$$R_{in} = r_\pi \| R_B \cong r_\pi$$

$$\frac{A_V \times R_{in}}{R_O} \leq \beta$$

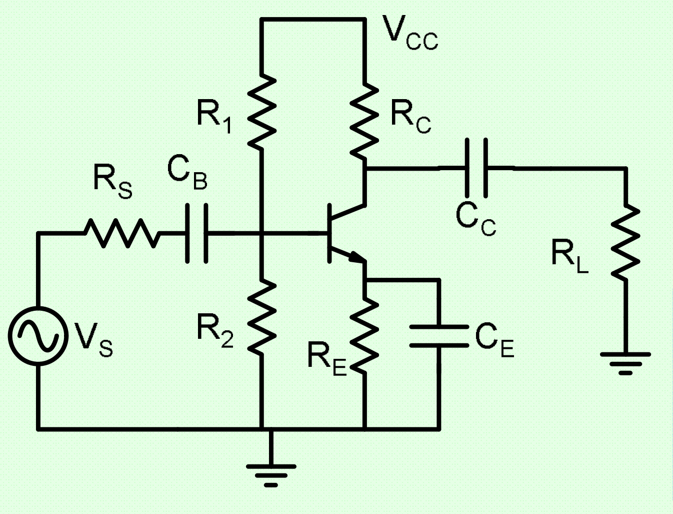
$$\frac{A_V}{R_O \times \omega_L} \leq C_E$$



Gain bandwidth tradeoff !

Gain-Bandwidth Tradeoff

Upper Cutoff Frequency



$$\omega_H \cong \frac{1}{(R'_S \| r_\pi)\{C_\pi + C_\mu(1 + g_m R'_C)\} + R'_C C_\mu}$$

$$\zeta = \frac{r_\pi}{r_\pi + r_{bb}}$$

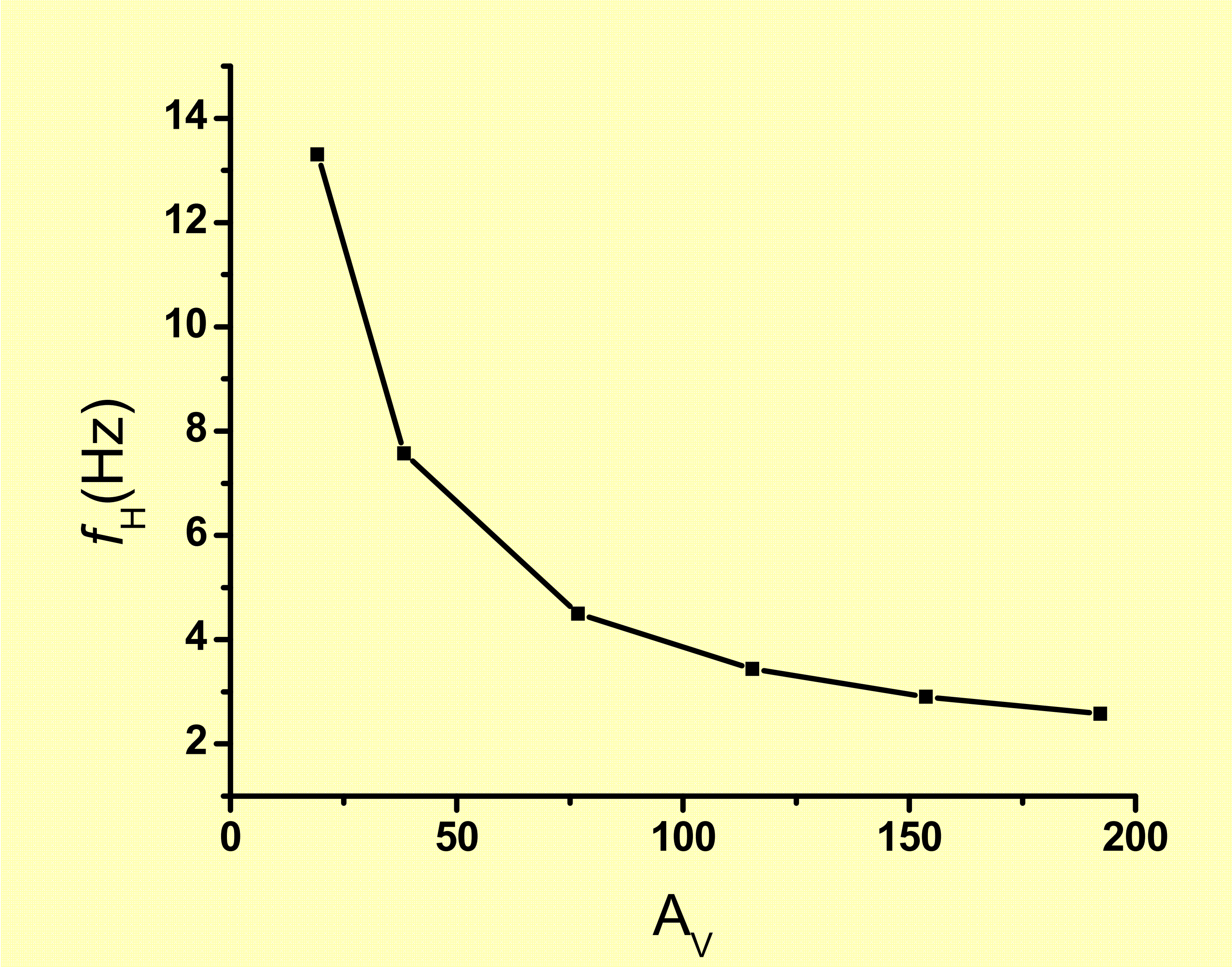
$$C_\pi = g_m \tau_F$$

$$g_m = \frac{I_{CQ}}{V_T}$$

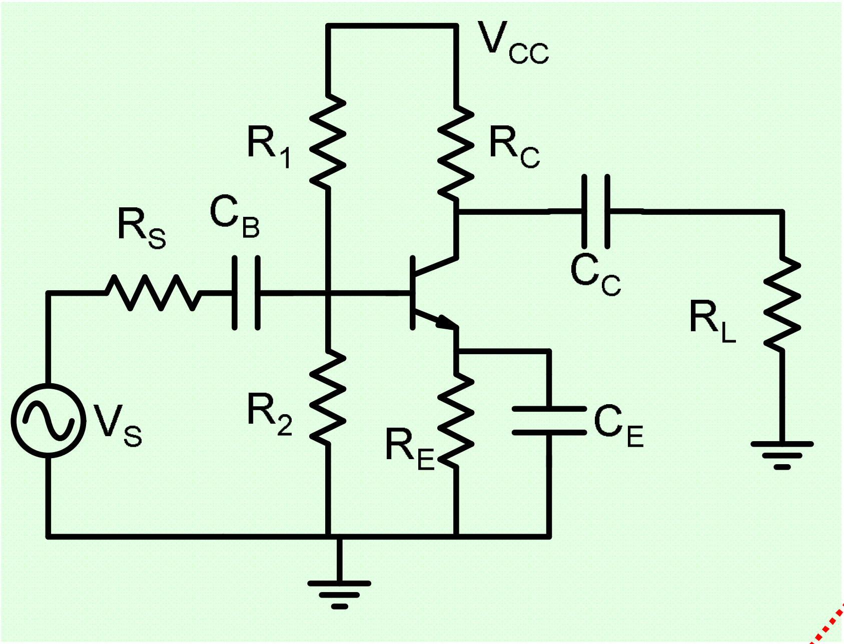
$$A_V = -\zeta \times g_m R'_C$$

$$\omega_H \cong \frac{1}{(R'_S \| r_\pi) \times |A_V| \left(\frac{1}{\zeta \times R'_C} + C_\mu \times \zeta^{-1}\right) + R'_C C_\mu}$$

Gain-Bandwidth Tradeoff



Design of CE Amplifier



Specifications:

$A_V \geq 100 \pm 20\%$ at T=300k

$R_O \leq 2.2k$

$R_{in} \geq 0.75k$

$v_{om} \geq 0.35V$ with THD $\leq 2\%$

$f_L \leq 2$ kHz

$f_H \geq 5$MHz

$R_L = 2.2k; R_S \sim 50\Omega$

Constraints : $V_{CC} \leq 9V$; Low cost; Low power

$$I_{CQ} = \frac{V_{CC}\frac{R_2}{R_1+R_2} - V_{BE}(on)}{\frac{R_B}{\beta} + R_E}; R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$S = \frac{\Delta I_{CQ}/I_{CQ}}{\Delta\beta/\beta} = \frac{1}{1+\frac{\beta R_E}{R_B}}; \quad x_b = \frac{R_B}{r_\pi}$$

$$V_{CC} = V_{CEQ} + I_{CQ}(R_C + R_E)$$

$$A_V = -\frac{I_{CQ}}{V_T} \times R_C \| R_L \qquad R_{in} = r_\pi \| R_B \qquad R_o = R_C$$

$$\omega_L = \frac{1}{C_E \times (R_E \| \frac{(R_S \| R_B) + r_\pi}{\beta})}$$

$$V_{om} = Min.\left\{(V_{CEQ} - V_{CEsat.}), \frac{H_{D2}}{25} \times I_{CQ} R_C \| R_L\right\}$$

$$\omega_H \cong \frac{1}{\left((R_S \| R_B) + r_{bb}\right) \| r_\pi \{C_\pi + C_\mu(1 + g_m R_C \| R_L)\} + C_\mu R_C \| R_L}$$

Design variables:

R_1, R_2, R_C, R_E

C_B, C_C, C_E

V_{CC}

Transistor

Specifications:

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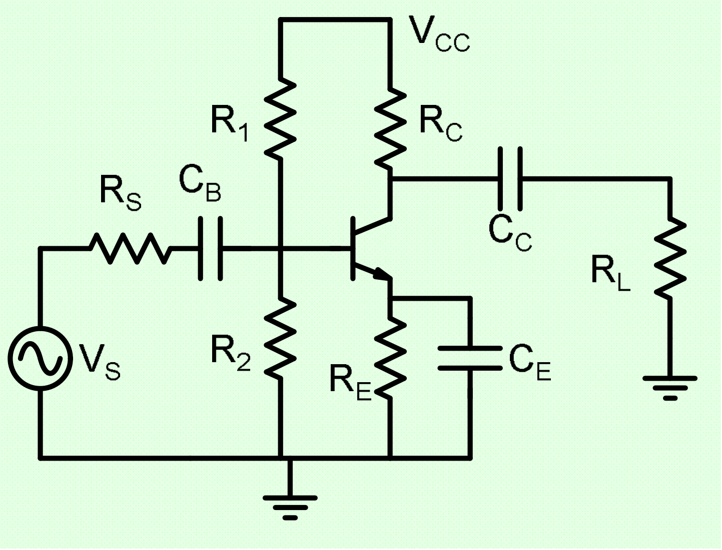
$\mathrm{f}_L \leq 2$ kHz

$f_H \geq 5$MHz

$\mathrm{R}_L = 2.2k; R_S \sim 50\Omega$

Constraints : $V_{CC} \leq 9V$; Low cost; Low power



Design variables:

$\mathrm{R_1, R_2, R_C, R_E}$

$\mathrm{C_B, C_C, C_E}$

$\mathrm{V_{CC}}$

Transistor

Design variables:

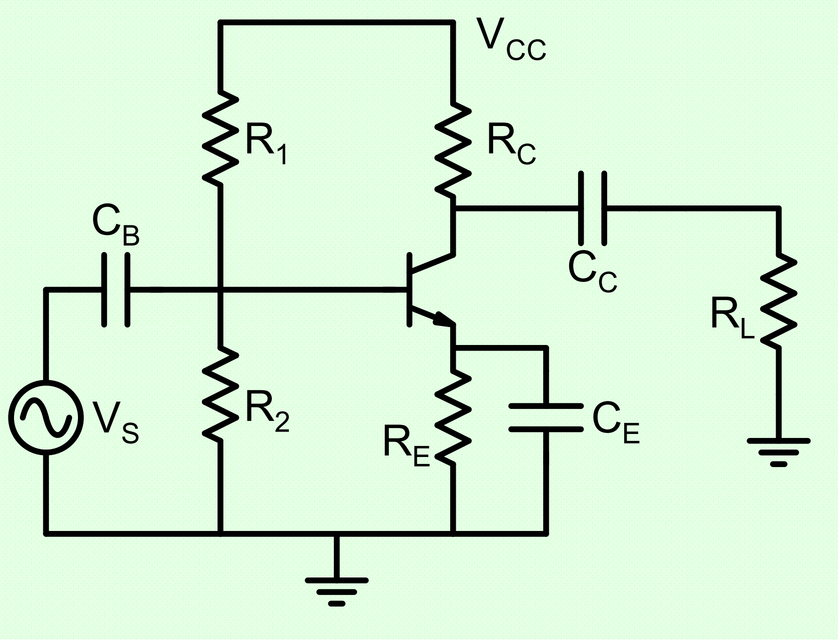
$\left\{\text{Bias point: } I_{CQ}, V_{CEQ}, V_E\right\}$

$\mathrm{R_C}$

$\mathrm{C_E}$

Transistor $\left\{\beta, \tau_F, C_{jeo}, C_{jco}\right\}$

Emitter bias point



$$I_{CQ} = \frac{V_{CC}\dfrac{R_2}{R_1 + R_2} - V_{BE}(on)}{\dfrac{R_B}{\beta} + R_E}$$

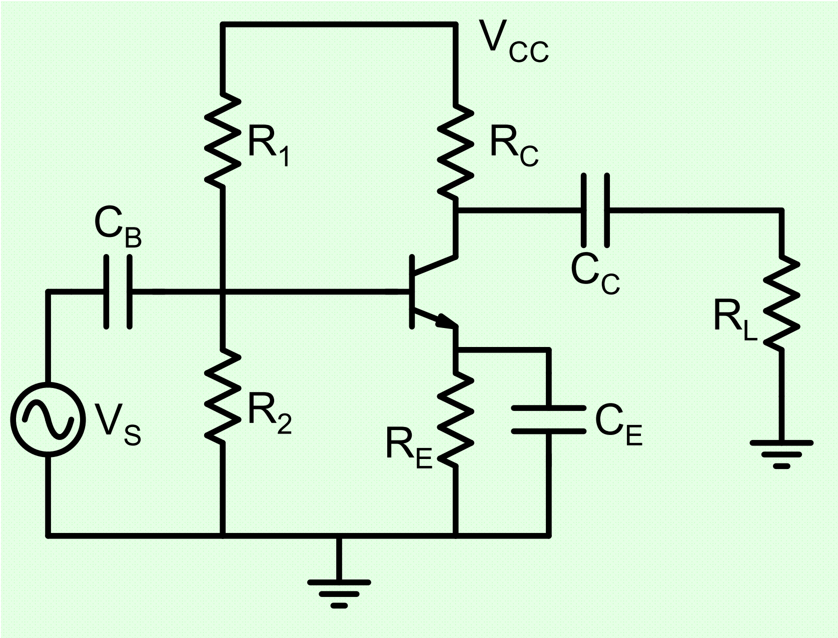
$$S = \frac{\Delta I_{CQ} / I_{CQ}}{\Delta\beta / \beta} = \frac{1}{1 + \dfrac{\beta R_E}{R_B}}; \quad x_b = \frac{R_B}{r_\pi}$$

$$V_E = I_{CQ} R_E$$
$$= \left(\frac{R_B}{r_\pi}\right) \times \left(\frac{R_E}{R_B / \beta}\right) \times V_T$$

$$V_E = x_b \times (S^{-1} - 1) \times V_T$$

For S = 0.1, $V_E = x_b \times 0.23V$; S = 0.01, $V_E = x_b \times 2.3V$

Emitter bias point



$$I_{CQ} = \frac{V_{CC}\dfrac{R_2}{R_1+R_2} - V_{BE}(on)}{\dfrac{R_B}{\beta} + R_E}$$

$$y = \frac{I_{C2} - I_{C1}}{I_{C1}} = \frac{(\beta_2 - \beta_1)}{(\beta_1 + x_e\beta_2)}; x_e = \frac{\beta_1 R_E}{R_B}$$

$$x_e = \frac{\beta_1 R_E}{R_B} \geq \frac{\beta_2 - \beta_1 \times (1+y)}{y\beta_2}$$

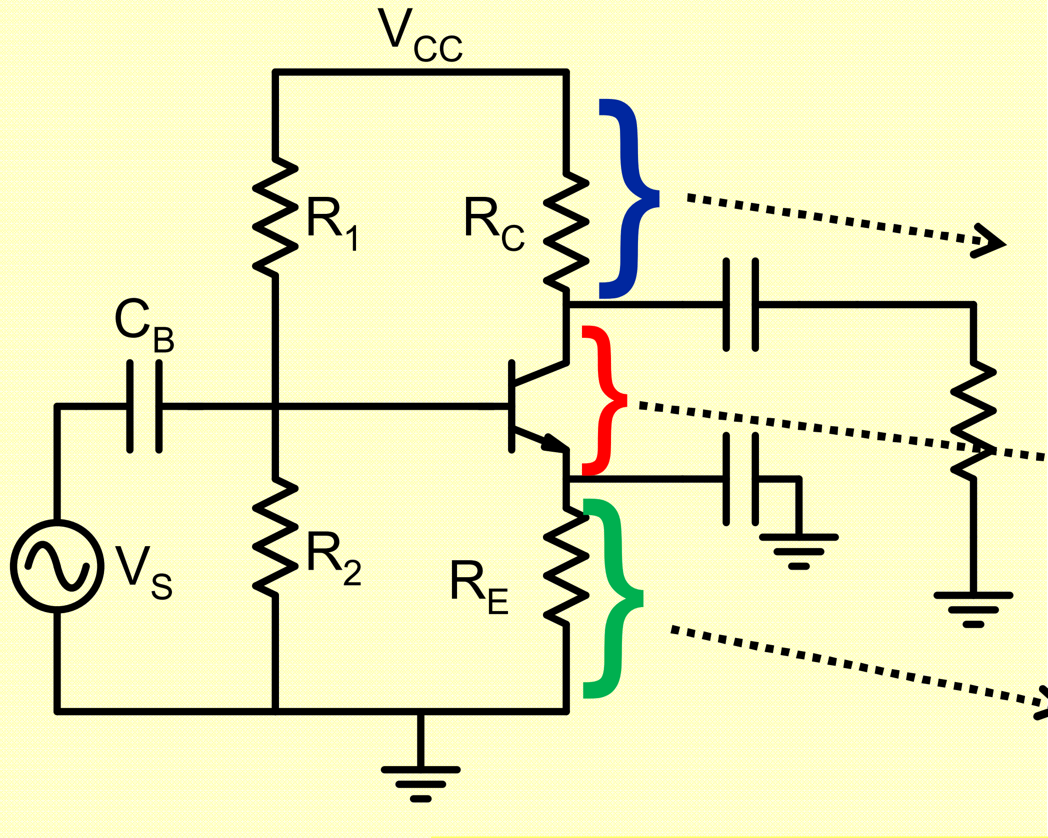
$$V_E = x_b \times x_e \times V_T; x_b = R_B / r_\pi$$

For β_1=100, β_2=200; y = 0.05 $\Rightarrow$ $x_e = 10.52 \Rightarrow V_E = 0.27 x_b$

Supply Voltage Budgeting

$$V_{om} = Min.\left\{(V_{CEQ} - V_{CEsat.}), \frac{H_{D2}}{25} \times I_{CQ} R_C \| R_L\right\}$$

$$A_V = -\frac{I_{CQ}}{V_T} \times R_C \| R_L$$



$$I_{CQ} \times R_C \| R_L = A_V \times V_T$$

$$I_{CQ} \times R_C \| R_L \geq v_{om} \times \frac{25}{HD_2}$$

$$V_{CEQ} \geq v_{om} + 0.2$$

$$V_E = x_b \times (S^{-1} - 1) \times V_T$$

$$V_{CC} > A_V V_T \times (1 + R_L / R_O) + v_{om} + x_b (S^{-1} - 1) V_T$$

$$S = \frac{\Delta I_{CQ} / I_{CQ}}{\Delta\beta / \beta} = \frac{1}{1 + \frac{\beta R_E}{R_B}}; \quad x_b = \frac{R_B}{r_\pi}$$

Supply Voltage Budgeting

$$V_{CC} > A_V V_T \times (1 + R_o / R_L) + v_{om} + x_b (S^{-1} - 1) V_T$$

Example: Suppose $A_V = 200$; $R_L / R_O = 1$

$$V_{CC} > 10.4 + ? + ?$$

Suppose S = 0.01 $V_{CC} > ? + ? + 23.4$

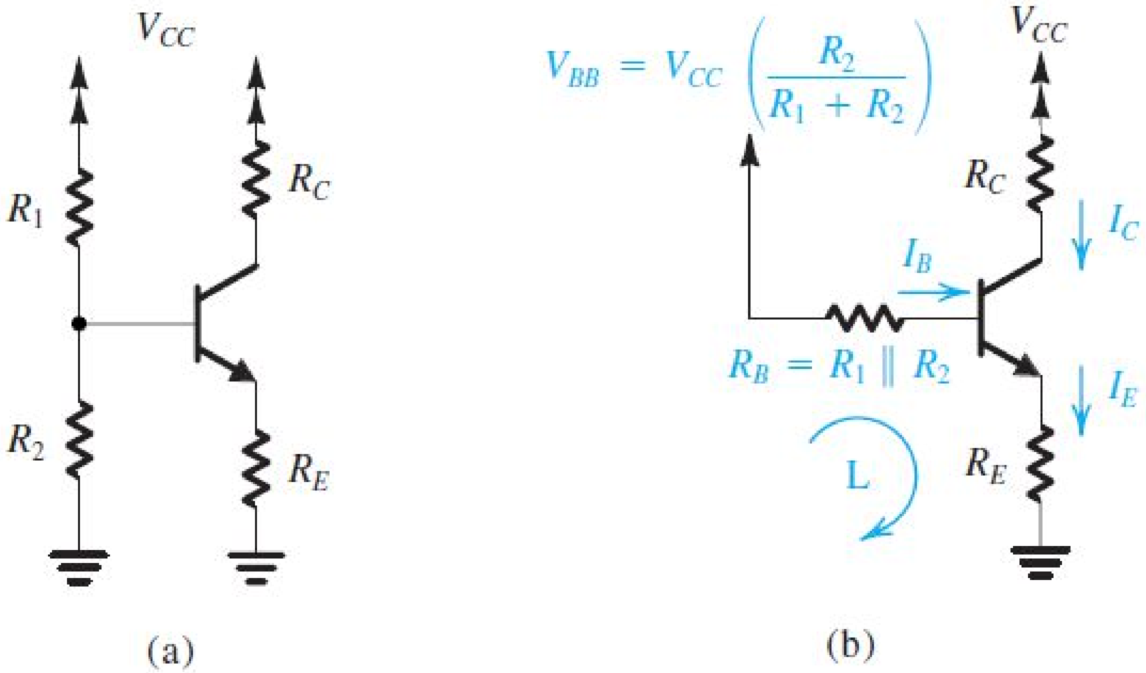


Figure 6.60 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

Figure 6.60(b) shows the same circuit with the voltage divider network replaced by its Thévenin equivalent,

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{6.102}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{6.103}$$

The current I_E can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting $I_B = I_E/(\beta + 1)$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{6.104}$$

To make I_E insensitive to temperature and β variation,[17] we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \tag{6.105}$$

$$R_E \gg \frac{R_B}{\beta + 1} \tag{6.106}$$

Condition (6.105) ensures that small variations in V_{BE} ($\simeq 0.7$ V) will be swamped by the much larger V_{BB}. There is a limit, however, on how large V_{BB} can be: For a given value of the supply voltage V_{CC}, the higher the value we use for V_{BB}, the lower will be the sum of voltages across R_C and the collector–base junction (V_{CB}). On the other hand, we want the voltage across R_C to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want V_{CB} (or V_{CE}) to be large to provide a large signal swing (before transistor saturation). Thus, as is the case in any design, we have a set of conflicting requirements, and the solution must be a trade-off. As a rule of thumb, one designs for V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$.

Example 6.20

We wish to design the bias network of the amplifier in Fig. 6.60 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_2 and another one-third to the voltage drop across R_C, leaving one-third for possible negative signal swing at the collector. Thus,

$$V_B = +4 \text{ V}$$

$$V_E = 4 - V_{BE} \simeq 3.3 \text{ V}$$

and R_E is determined from

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage divider current of $0.1I_E = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

Thus $R_2 = 40$ kΩ and $R_1 = 80$ kΩ.

At this point, it is desirable to find a more accurate estimate for I_E, taking into account the nonzero base current. Using Eq. (6.104),

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \frac{(80 \parallel 40)(\text{k}\Omega)}{101}} = 0.93 \text{ mA}$$

This is quite a bit lower than 1 mA, the value we are aiming for. It is easy to see from the above equation that a simple way to restore I_E to its nominal value would be to reduce R_E from 3.3 kΩ by the magnitude of the second term in the denominator (0.267 kΩ). Thus a more suitable value for R_E in this case would be $R_E = 3$ kΩ, which results in $I_E = 1.01 \text{ mA} \simeq 1$ mA.[19]

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to I_E (i.e., 1 mA), resulting in $R_1 = 8$ kΩ and $R_2 = 4$ kΩ. We shall refer to the circuit using these latter values as design 2, for which the actual value of I_E using the initial value of R_E of 3.3 kΩ will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

Example 6.20 *continued*

In this case, design 2, we need not change the value of R_E.

Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99 \text{ mA} \simeq 1 \text{ mA}$ results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4 \text{ k}\Omega$$

EXERCISE

6.47 For design 1 in Example 6.20, calculate the expected range of I_E if the transistor used has β in the range of 50 to 150. Express the range of I_E as a percentage of the nominal value ($I_E \simeq 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

Ans. For design 1: 0.94 mA to 1.04 mA, a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.