EE210: Microelectronics-I

Lecture-27 :Output Stage-1

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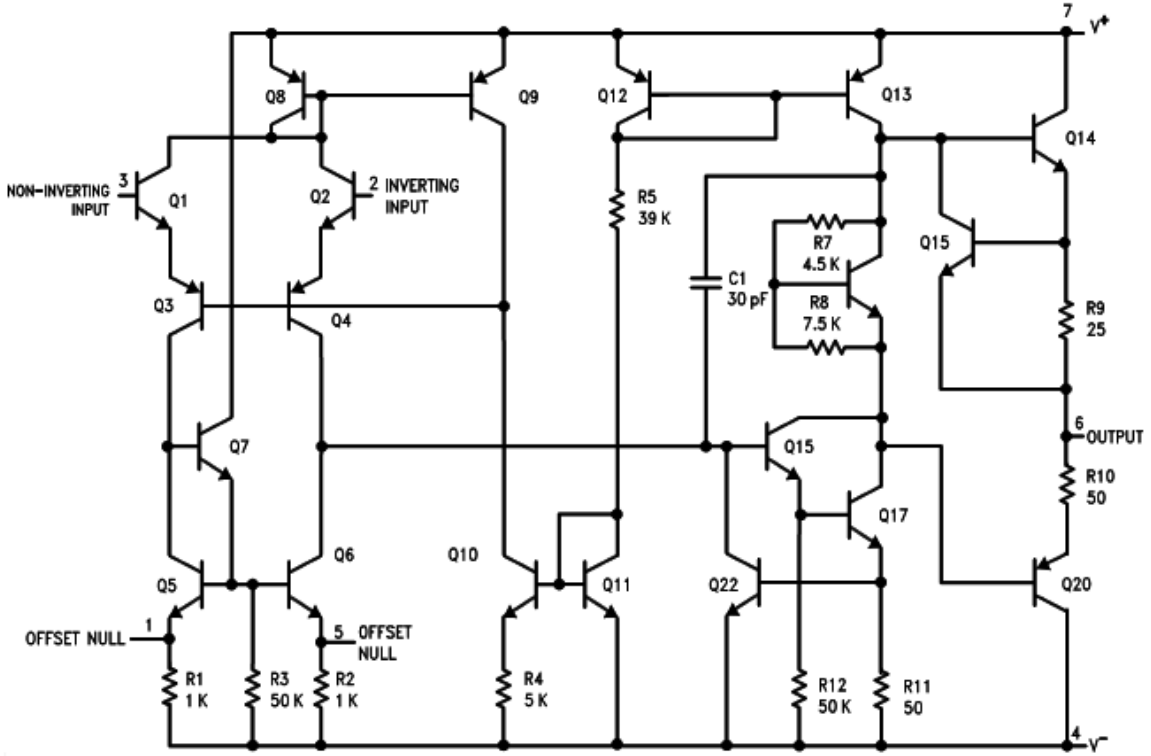
Most Amplifiers are Multi-stage

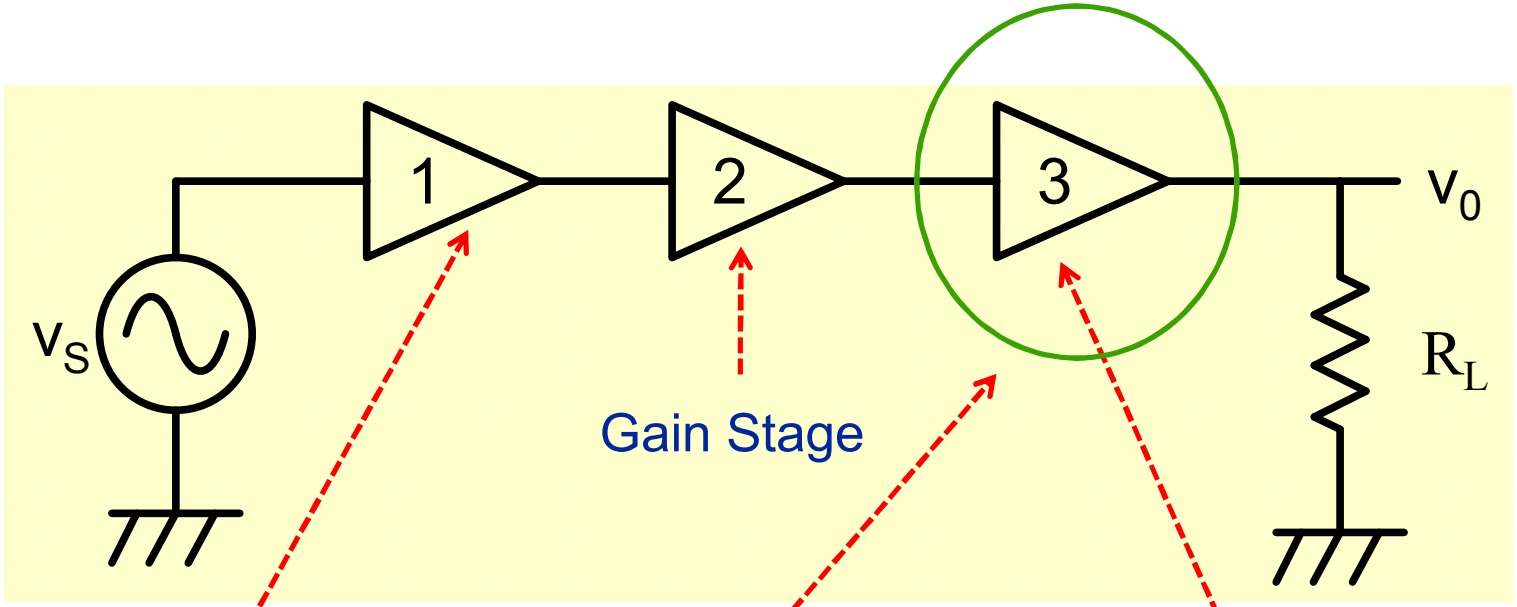
Schematic Diagram



The reason is that a single amplifier stage cannot provide all the desired characteristics.

Tradeoffs exist amongst amplifier characteristics

Principle of Division of labor !

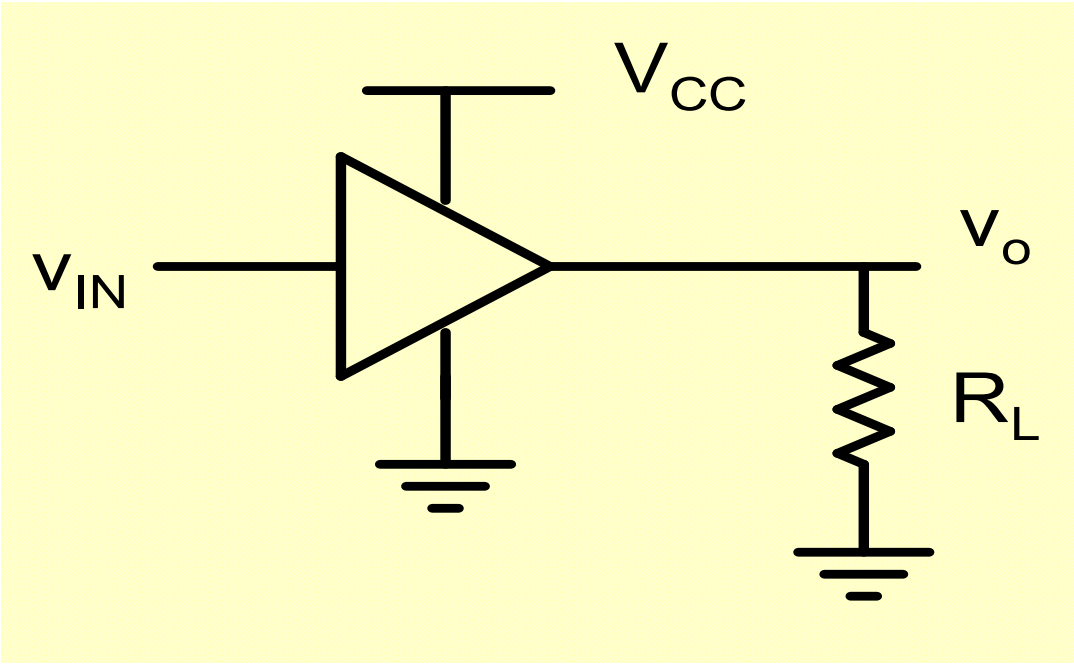


Specialize in input resistance

Specialize in output resistance and power delivery

Focus of the present discussion

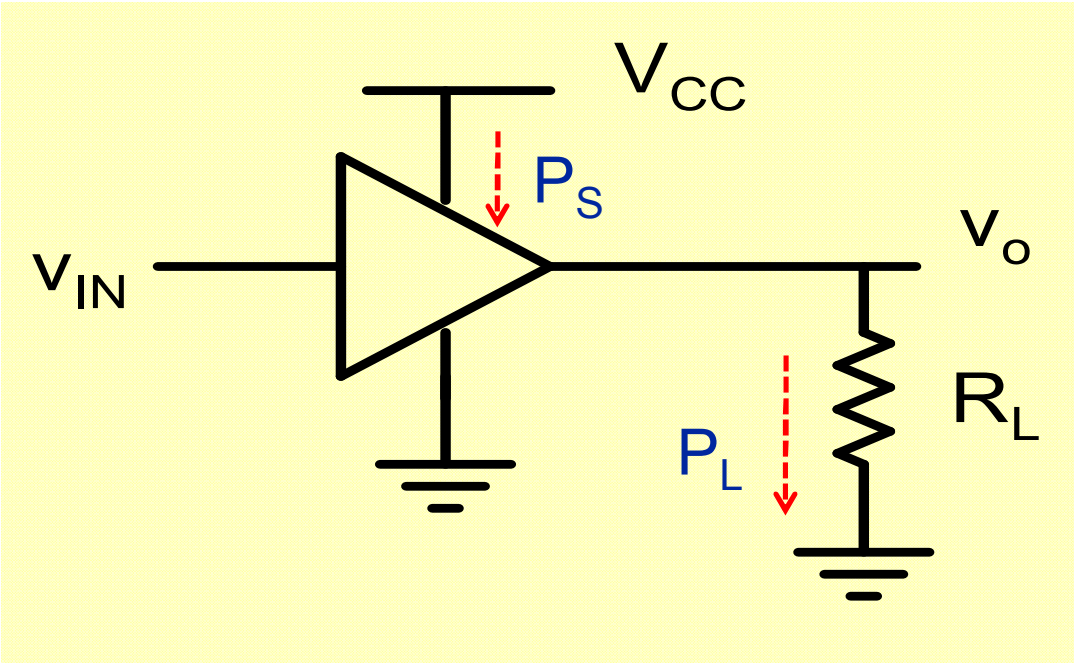
Output Stage: Important Characteristics



1. Output Resistance

2. Voltage Swing with low distortion

Output Stage: Important Characteristics

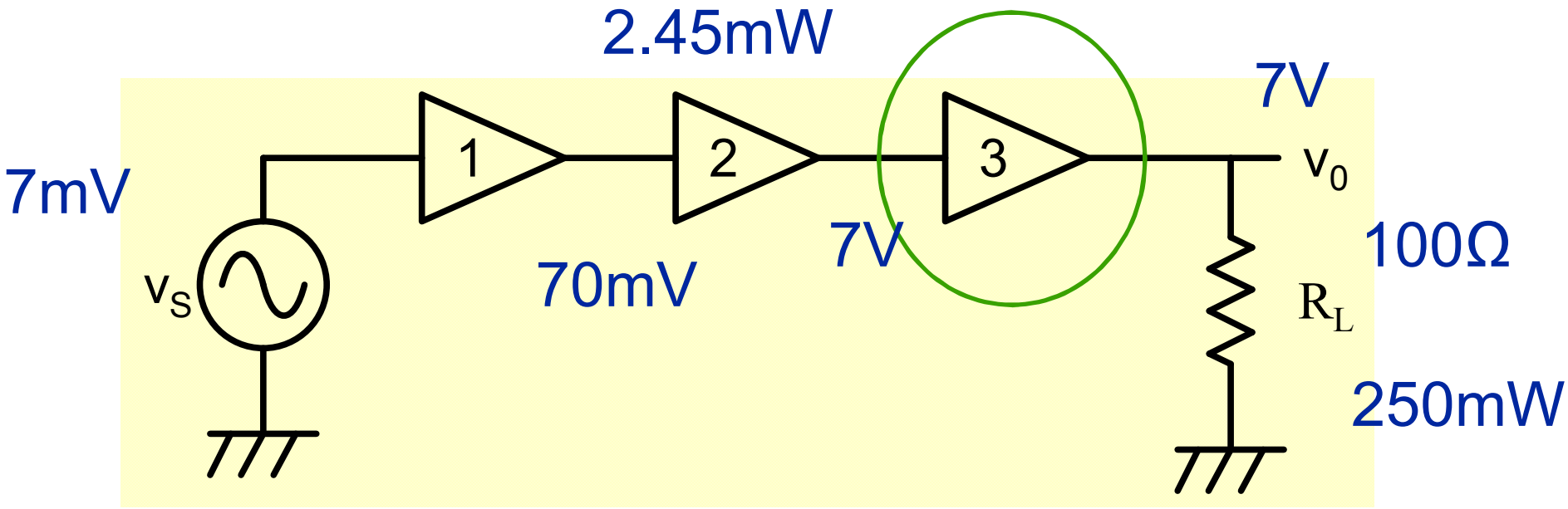


3. Power Conversion Efficiency:

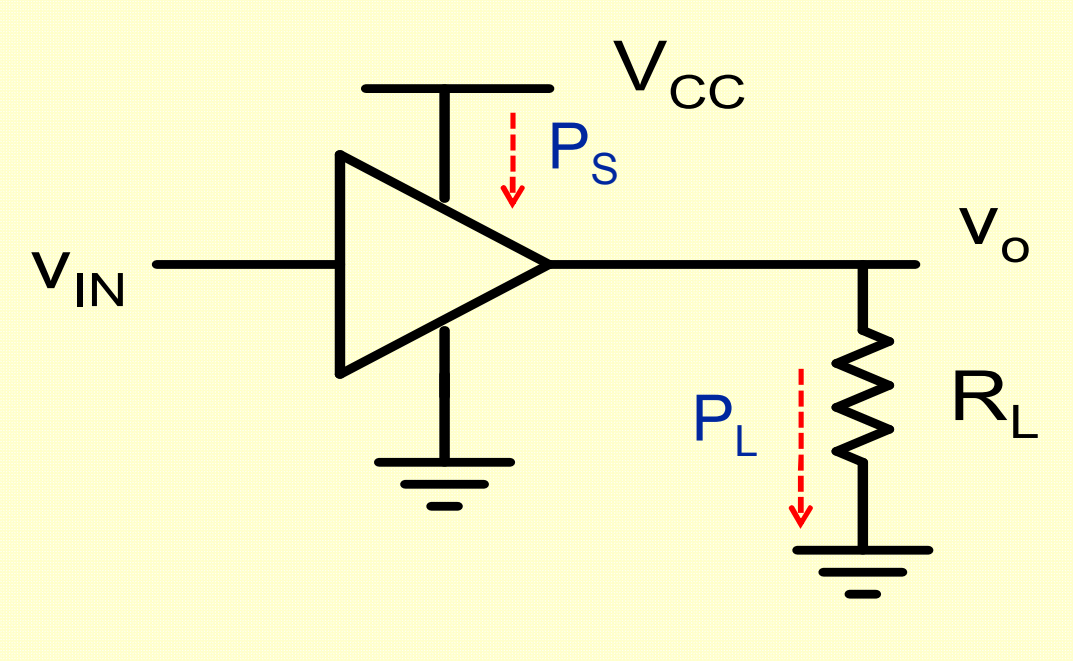
$$\eta = \frac{P_L}{P_S} \times 100$$

We would like all the power drawn from the power supply to be delivered to the Load and thus have high power conversion efficiency !

Power dissipation!



Power Lost

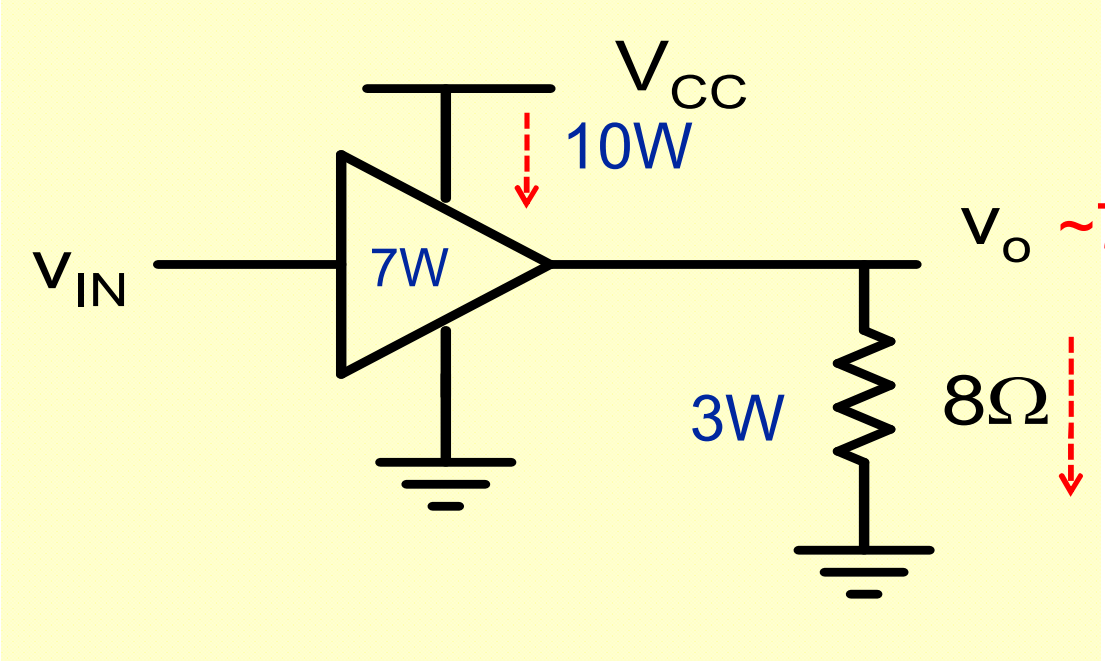


$$\eta = \frac{P_L}{P_S} \times 100$$

Power dissipated in the amplifier itself: $(1 - \frac{\eta}{100}) P_S$

This power is lost as HEAT

Transistor Selection



-one has to ensure that transistors can withstand the heat dissipated in them

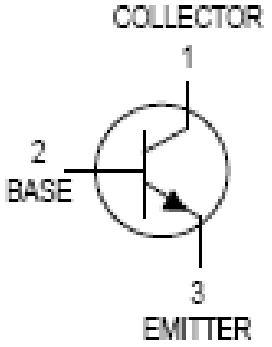
-Transistor should be able to handle the voltage levels

-Transistor should be able to handle the required current levels

Amplifier Transistors

NPN Silicon

P2N2222A



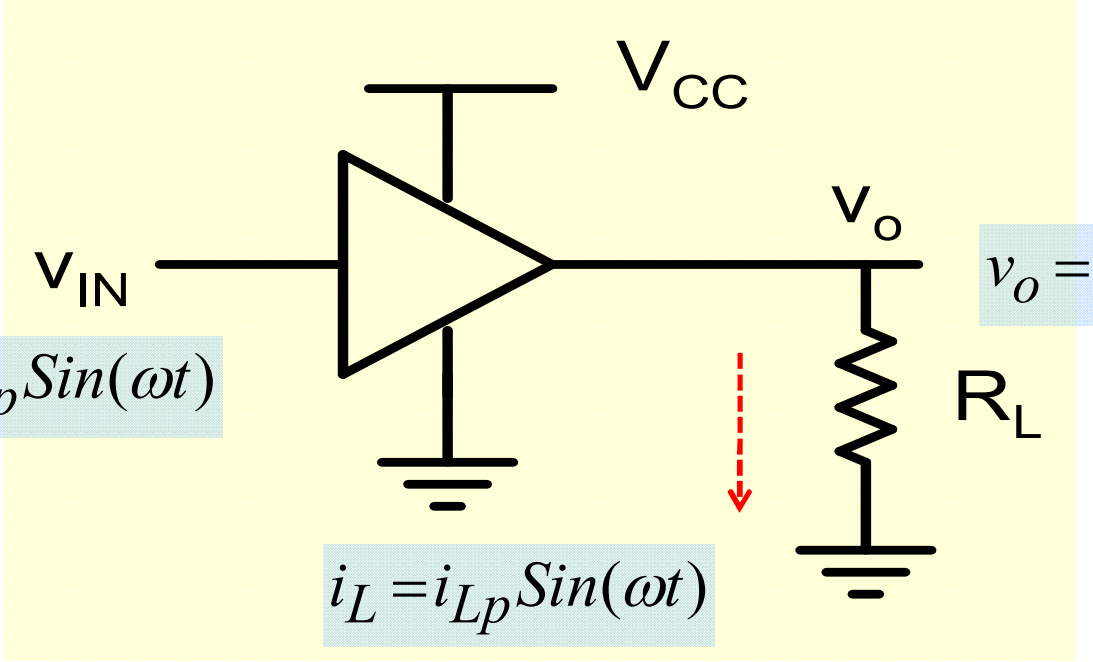
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	75	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

Load Power



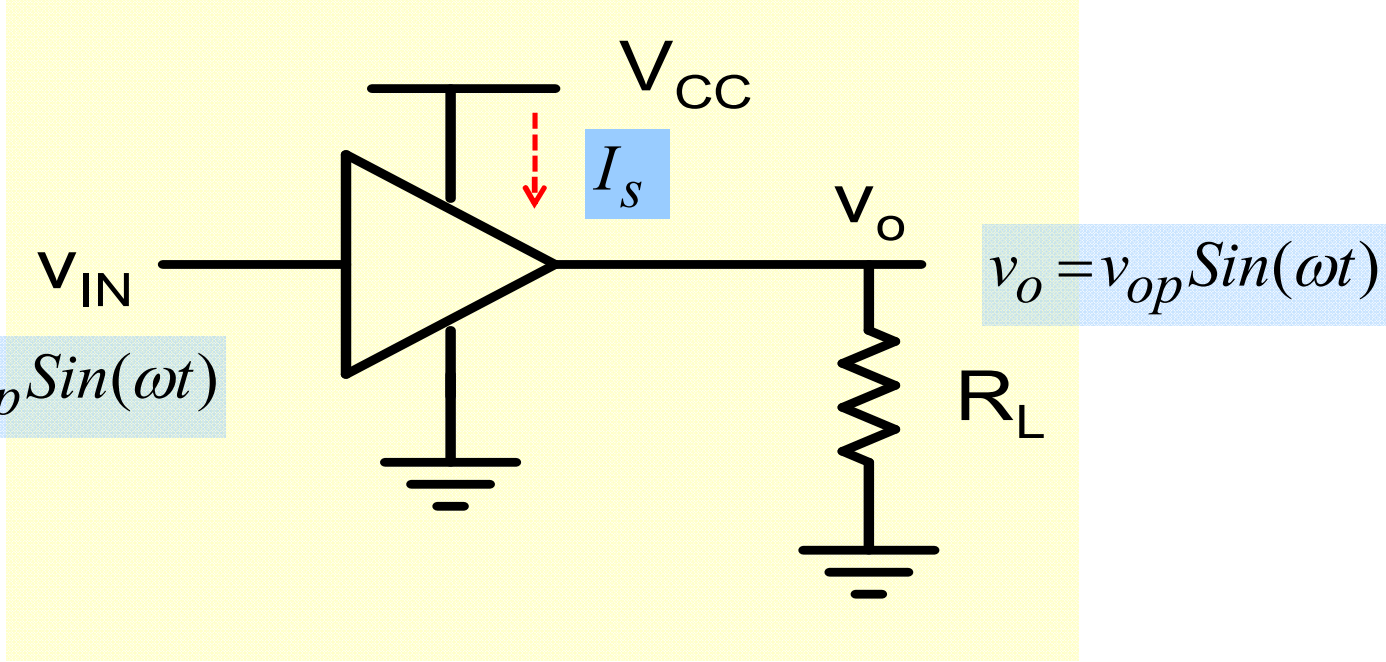
P: peak

Average Power delivered to load : $P_L = \frac{1}{T}\int_0^T \frac{v_{op}^2 Sin^2(\omega t)}{R_L} dt = \frac{v_{op}^2}{2R_L}$

$$P_L = \frac{i_{Lp}^2 R_L}{2}$$

$$P_L = \frac{v_{op} i_{Lp}}{2}$$

Input Power



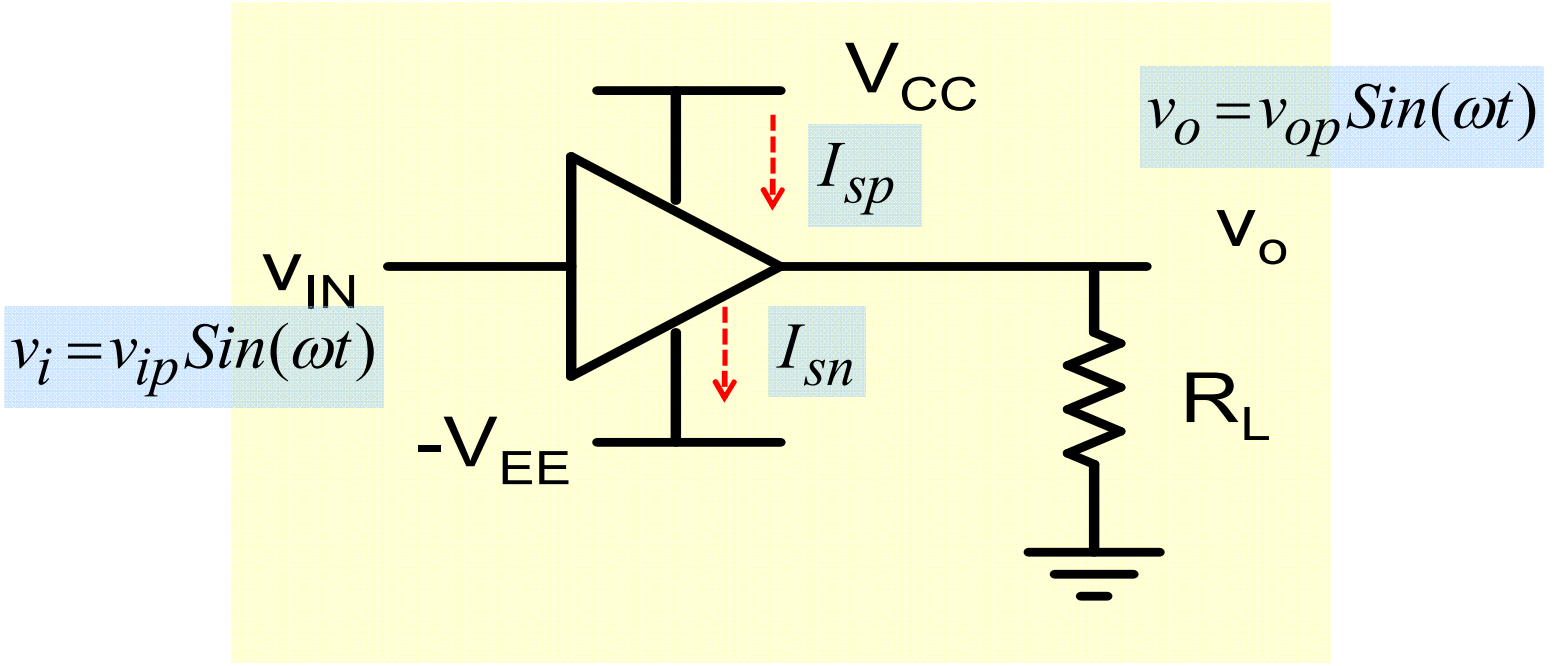
Average Power taken from Supply:

$$P_S = \frac{1}{T}\int_0^T V_{CC} \times I_s \, dt$$

$$P_S = V_{CC} \times \frac{1}{T}\int_0^T I_s \, dt = V_{CC} \times I_s(avg)$$

Average supply current

Input Power with dual supply

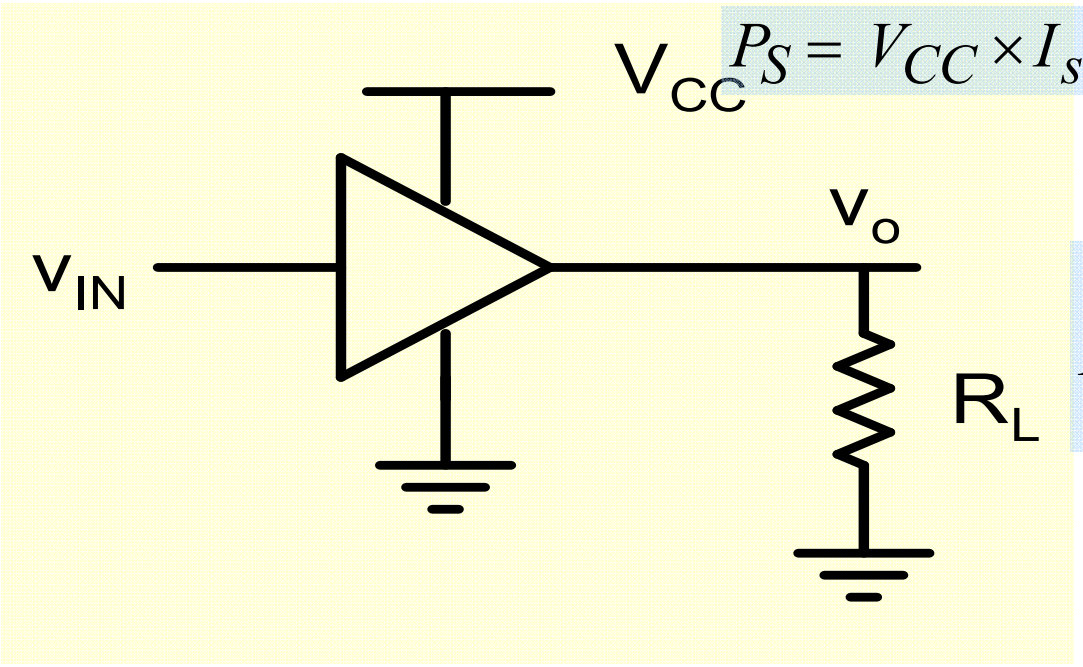


Average Power taken from Supply:

$$P_S = \frac{1}{T}\int_0^T (V_{CC} \times I_{sp} + V_{EE} \times I_{sn})\, dt$$

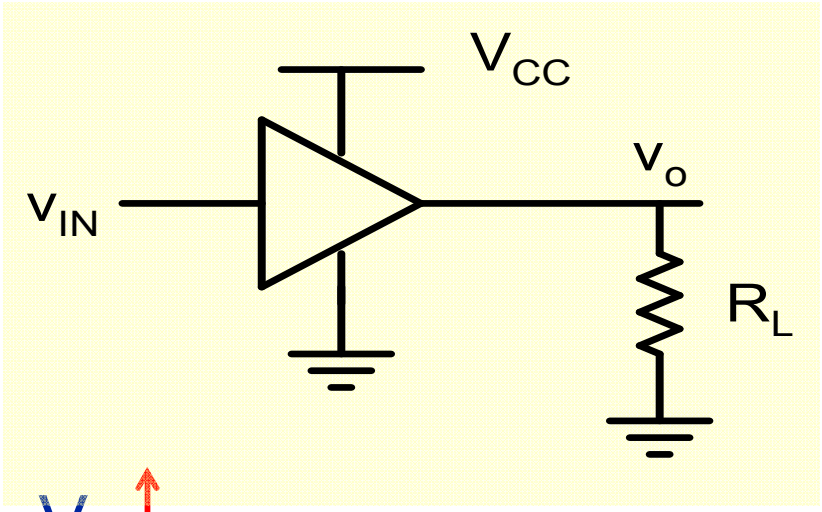
$$P_S = V_{CC} \times I_{sp}(avg.) + V_{EE} \times I_{sn}(avg.)$$

Efficiency

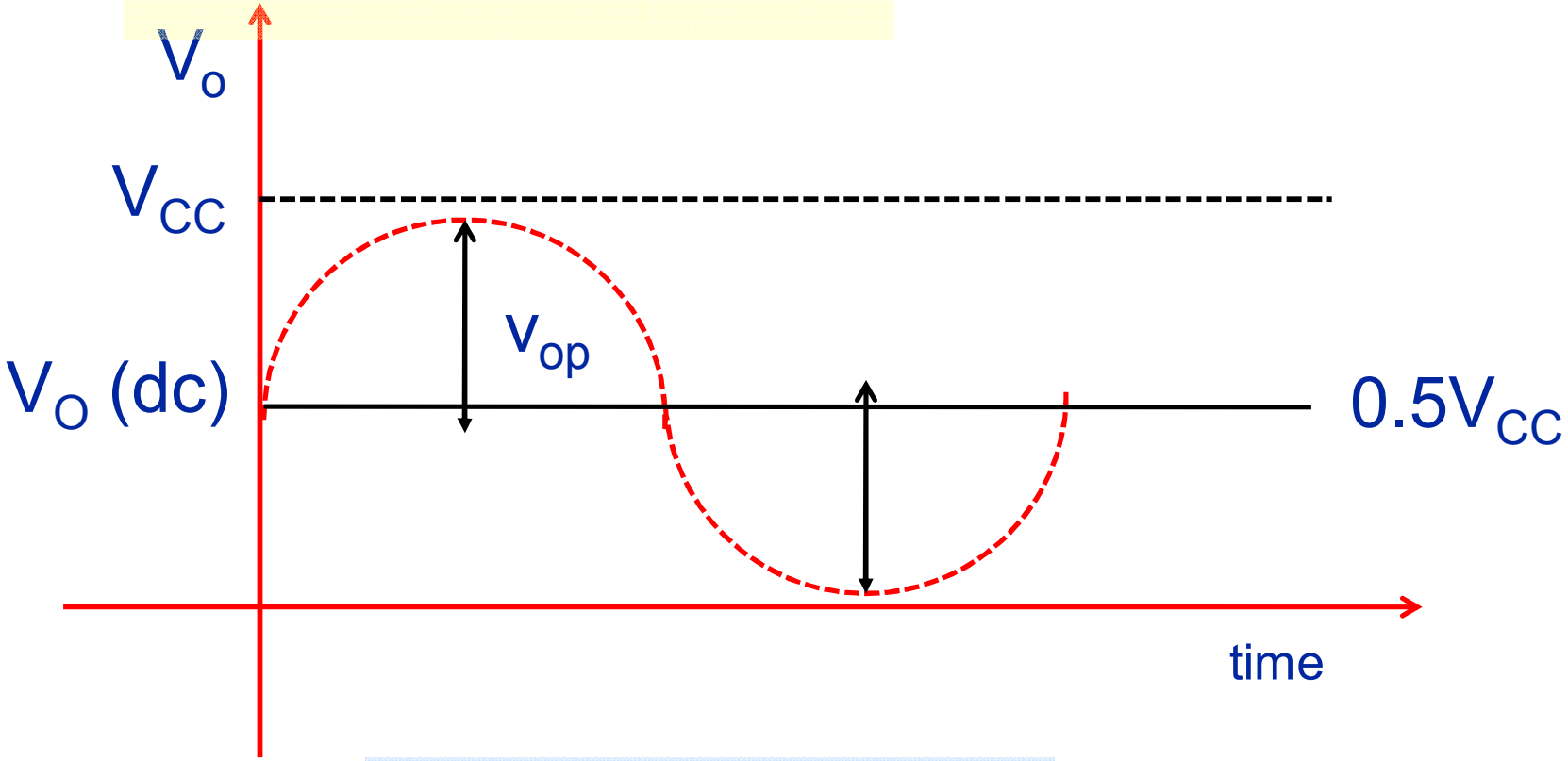


$$\eta = \frac{P_L}{P_S} \times 100 = 50 \times \frac{v_{op}}{V_{CC}} \times \frac{v_{op}/R_L}{I_s(avg.)}$$

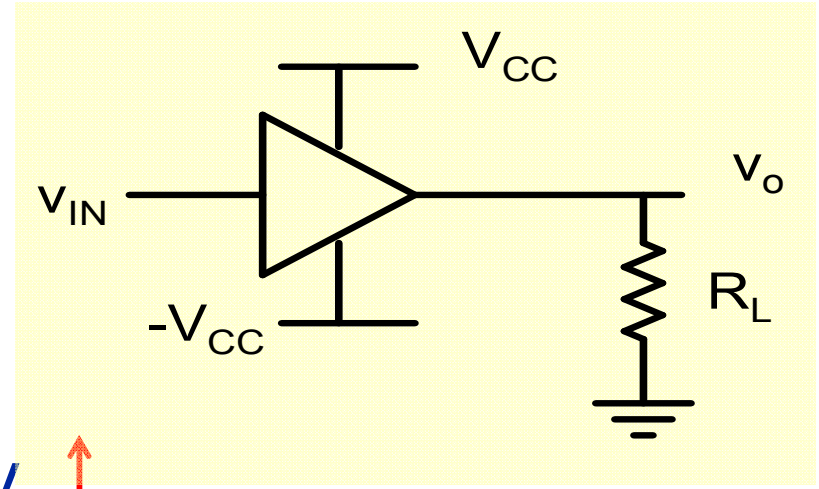
Efficiency increases with increase in output voltage (or load power) and Highest efficiency is obtained when output voltage (or load power) is maximum



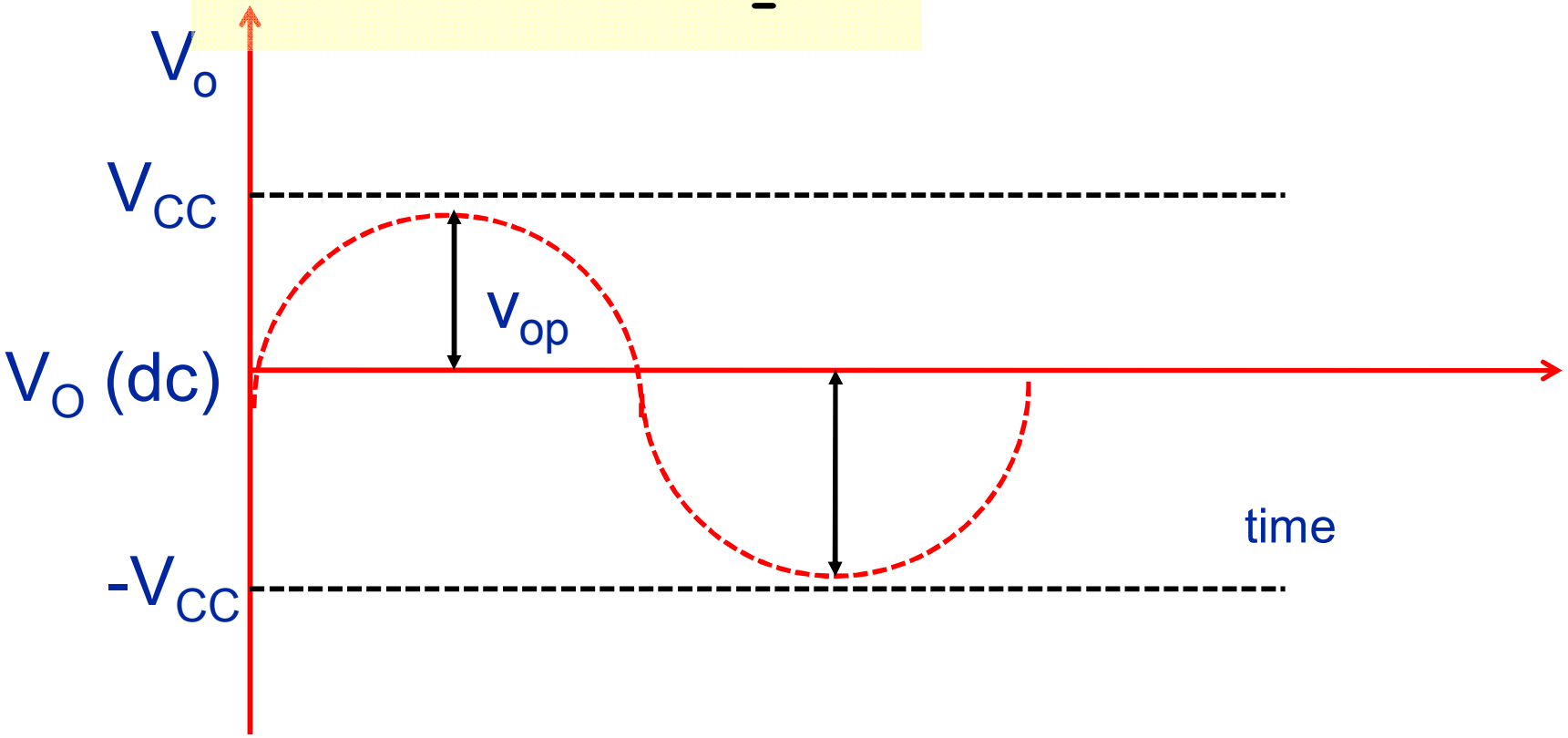
$$\eta = 50 \times \frac{v_{op}}{V_{CC}} \times \frac{v_{op} / R_L}{I_s(avg.)}$$



Design Goal: $v_{op} \approx V_{CC} / 2$

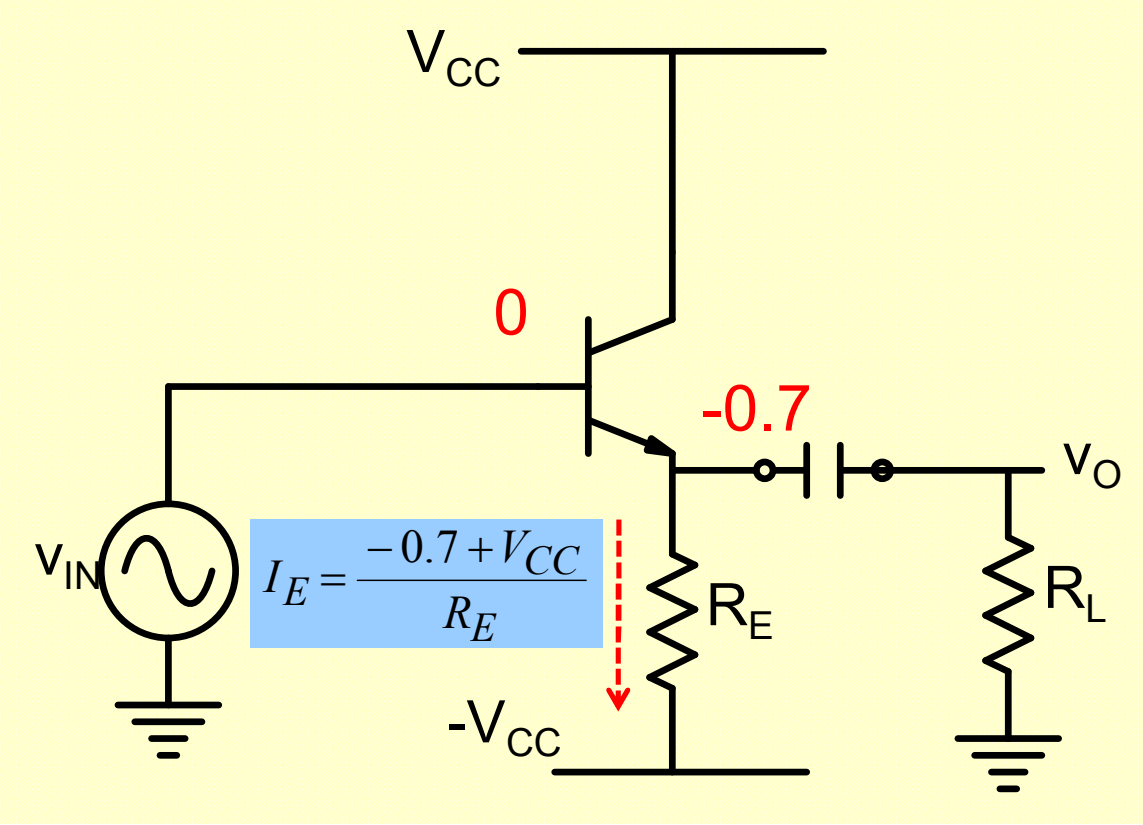


$$\eta = 50 \times \frac{v_{op}}{2V_{CC}} \times \frac{v_{op} / R_L}{I_{sp}(avg.)}$$



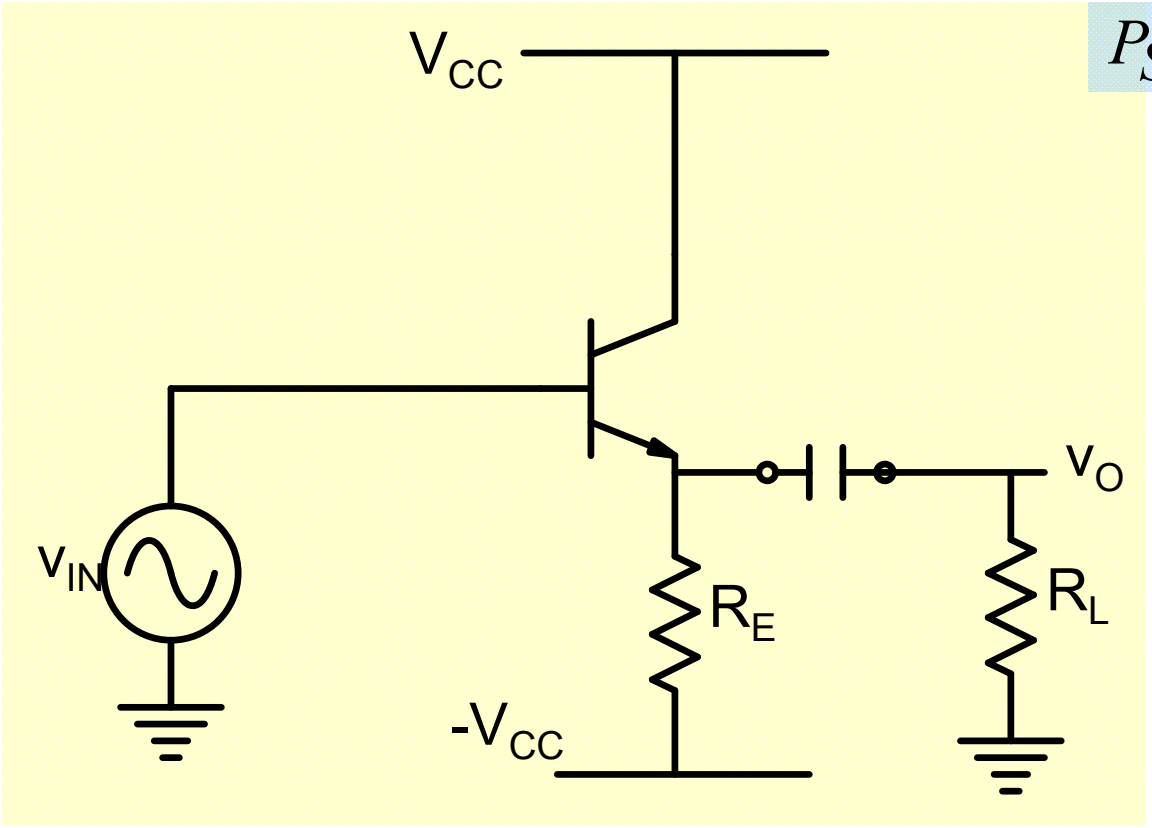
Design Goal: $v_{op} \approx V_{CC}$

CC Stage as a Power Amplifier



Low Output Resistance

Design for maximum Efficiency



$$P_S = V_{CC} I_C + V_{CC} I_E \cong 2 V_{CC} I_E$$

$$P_L = \frac{v_{op}^2}{2R_L}$$

$$I_E = \frac{-0.7 + V_{CC}}{R_E} \cong \frac{V_{CC}}{R_E}$$

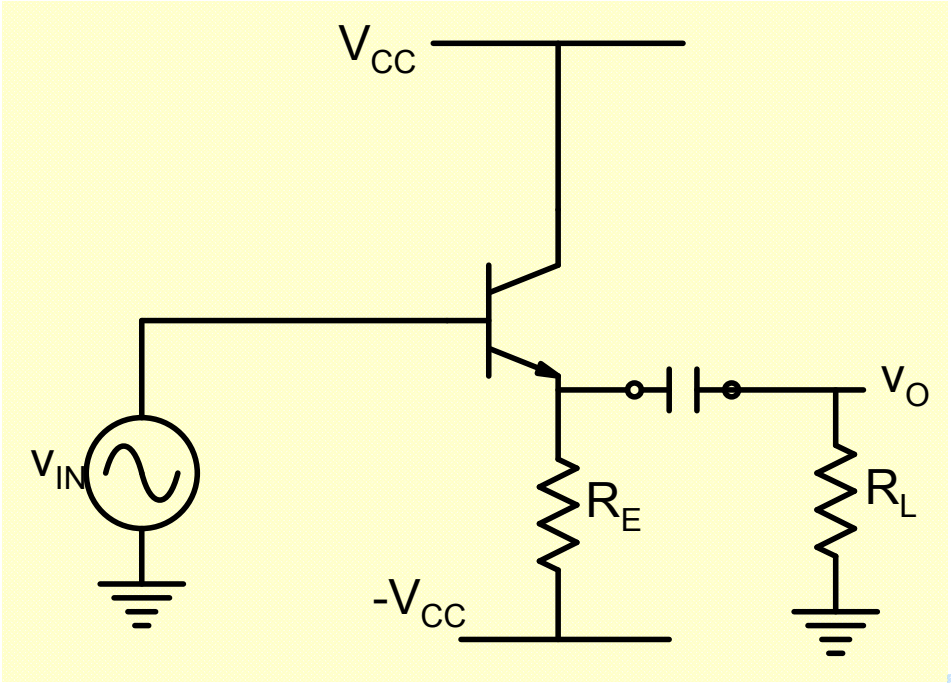
$$v_{op} = I_E R_E \| R_L$$

$$\eta = \frac{P_L}{P_S} = 25 \times \frac{(R_E \| R_L)^2}{R_L R_E}$$

To maximize efficiency : $\frac{d\eta}{dR_E} = 0$ $\Rightarrow \frac{R_E}{R_L} = 1$ $\eta_{\max} < 6.25\%$

Example

$$Specs:\ R_L = 100\Omega\ ;\ P_L = 20mW\ ;\ V_{CC} = \text{ any value}$$



$$P_L = \frac{v_{op}^2}{2R_L}$$

$$vop = \sqrt{2 \times P_L \times R_L} = 2V$$

$$R_E = R_L = 100\Omega$$

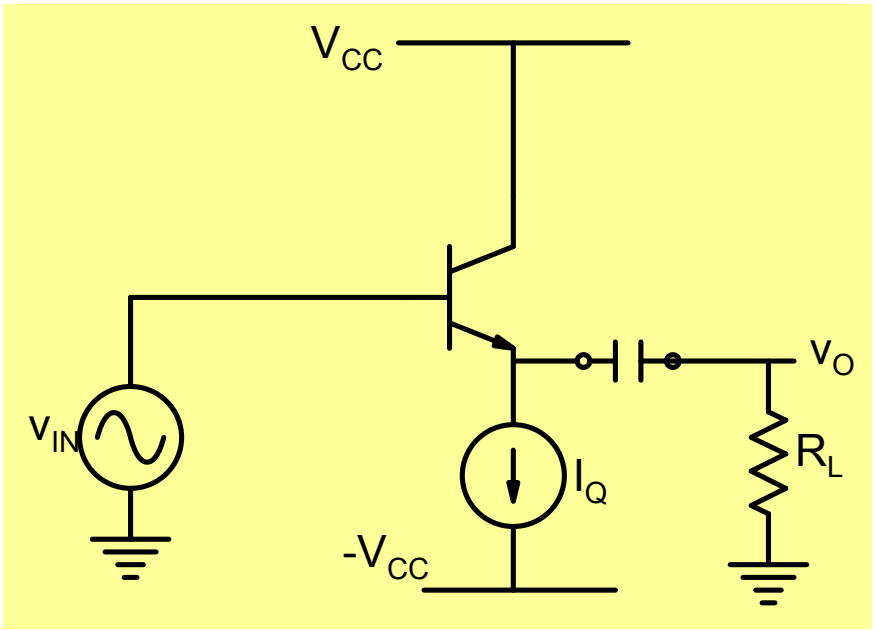
$$v_{op} = I_E R_E \| R_L$$

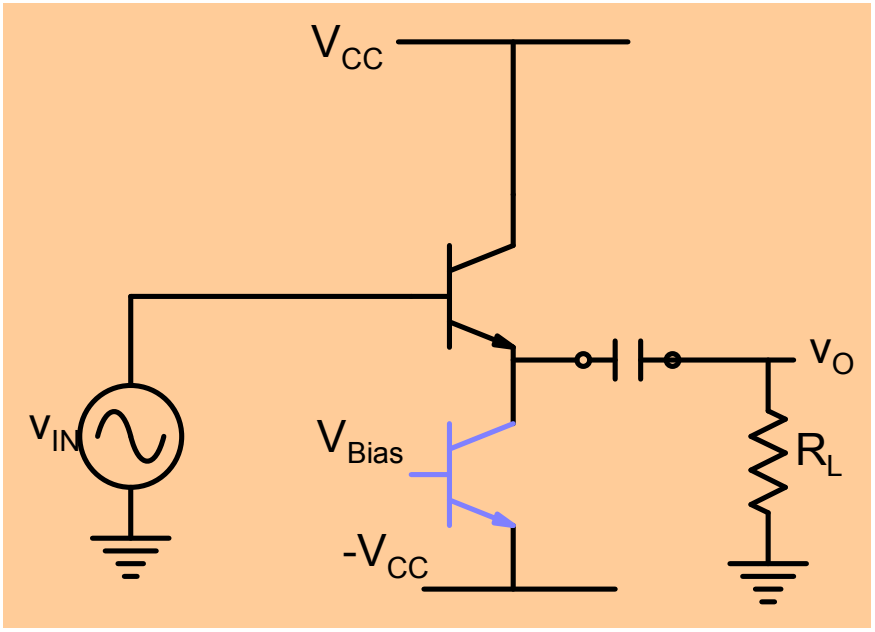
$$\Rightarrow I_E = 40mA$$

$$I_E = \frac{-0.7 + V_{CC}}{R_E} \Rightarrow V_{CC} = 4.7V$$

$$\eta = \frac{P_L}{P_S} = \frac{v_{op}^2}{2R_L \times 2V_{CC} I_E} = 5.3\%$$

Current Source Biasing





$$\frac{v_{op}^2}{2R_L} = P_L \Rightarrow v_{op} = \sqrt{2R_L P_L}$$

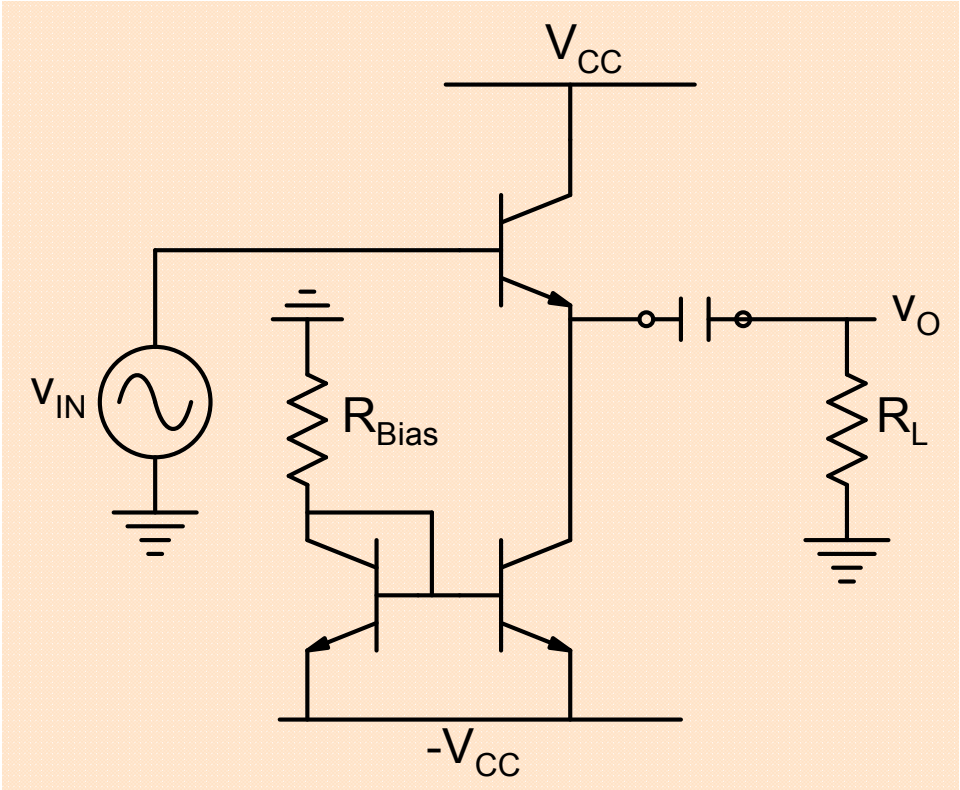
$$I_Q = \frac{v_{op}}{R_L}$$

$$V_{CC} \cong v_{op}$$

$$\eta = \frac{P_L}{P_S} = \frac{1}{4} \times \left(\frac{v_{op}}{V_{CC}}\right)\left(\frac{v_{op}}{I_E \times R_L}\right) < 25\%$$

Example

$$Specs:\ R_L = 100\Omega\ ;\ P_L = 20mW\ ;\ V_{CC} = \text{ any value}$$



$$P_L = \frac{v_{op}^2}{2R_L}$$

$$vop = \sqrt{2 \times P_L \times R_L} = 2V$$

$$v_{op} \le I_E R_L \Rightarrow I_E = 20mA$$

$$-0.7 - v_{op} - (-V_{CC}) \ge 0.2$$

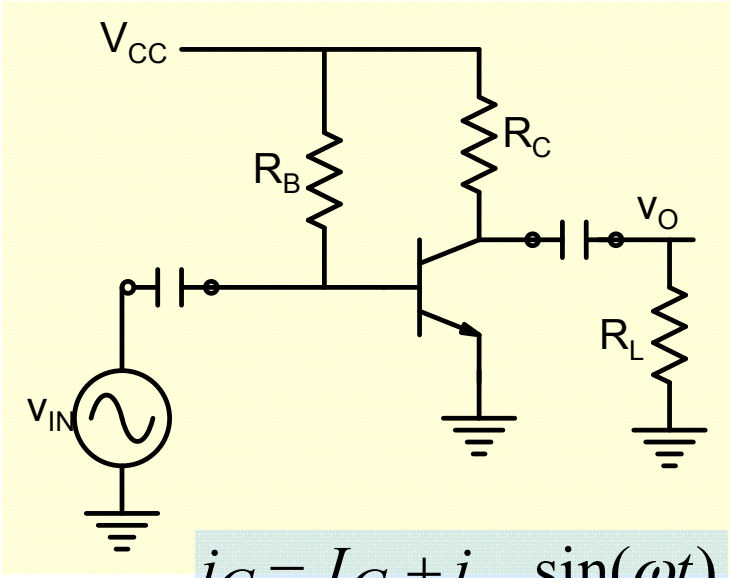
$$\Rightarrow V_{CC} = 2.9V$$

$$R_{Bias} = \frac{-0.7 + V_{CC}}{I_E} = 110\Omega$$

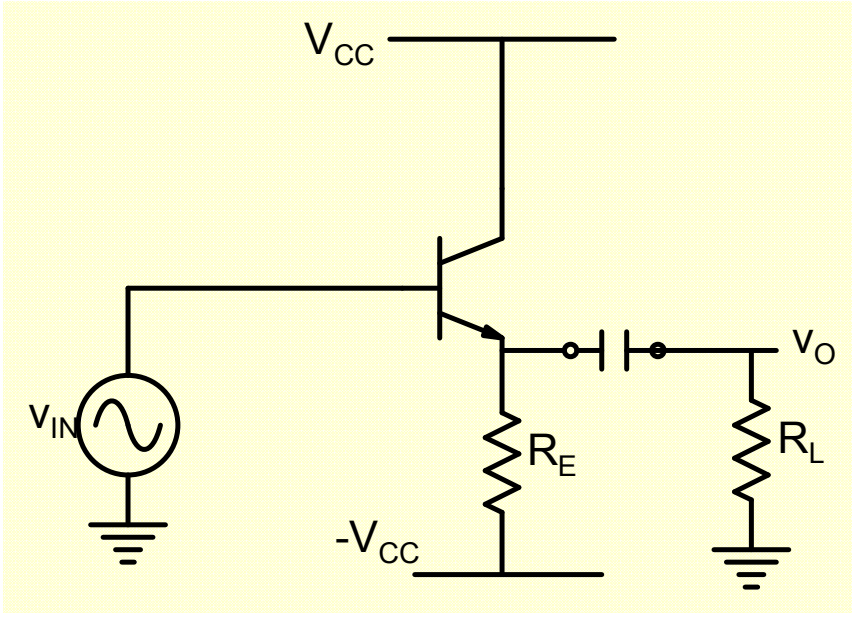
$$\eta = \frac{P_L}{P_S} = \frac{v_{op}^2}{2R_L \times 2V_{CC} I_E} = 17.2\%$$

Class A Power Amplifiers

-Amplifiers in which the transistor is ON (or conducts current) for the entire duration of sinusoidal cycle.

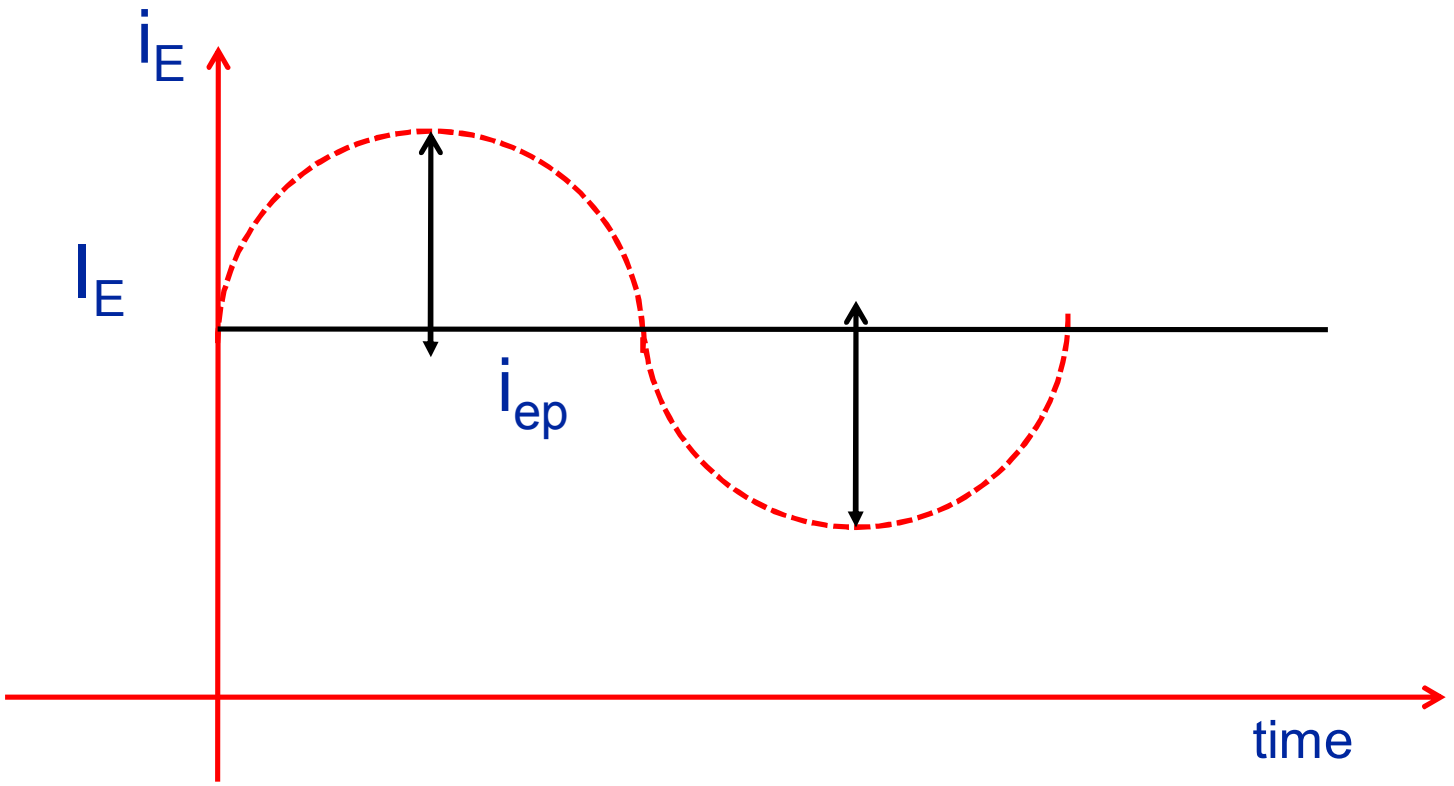


$$i_C = I_C + i_{cp}\sin(\omega t)$$

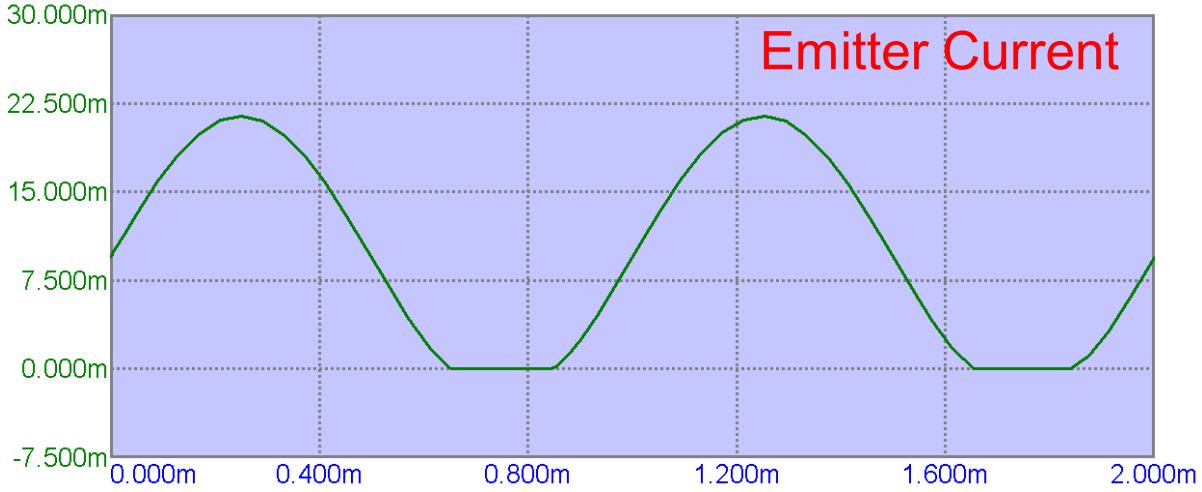


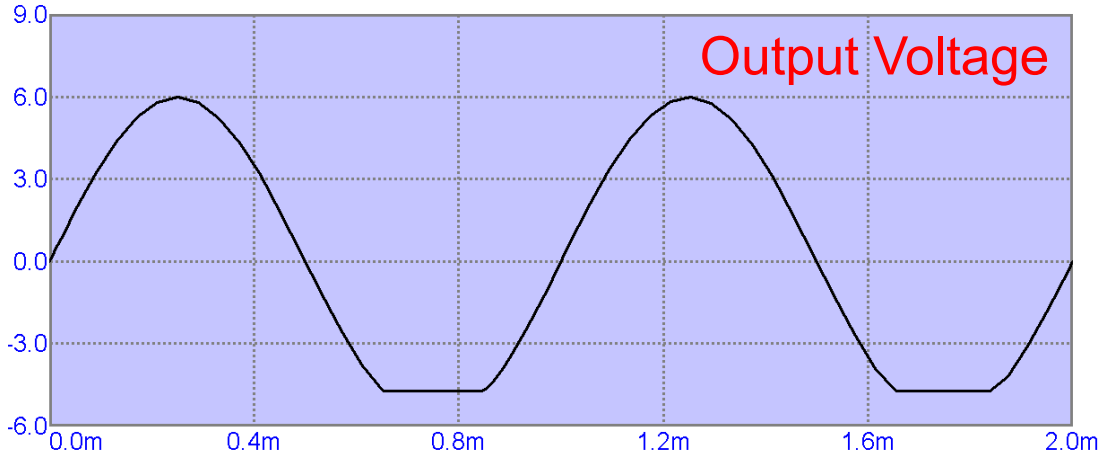
$$i_E = I_E + i_{ep}\sin(\omega t)$$

$$i_{ep} \le I_E$$


i_E
I_E
i_{ep}
time

If current becomes zero, clipping in current and output voltage would occur.

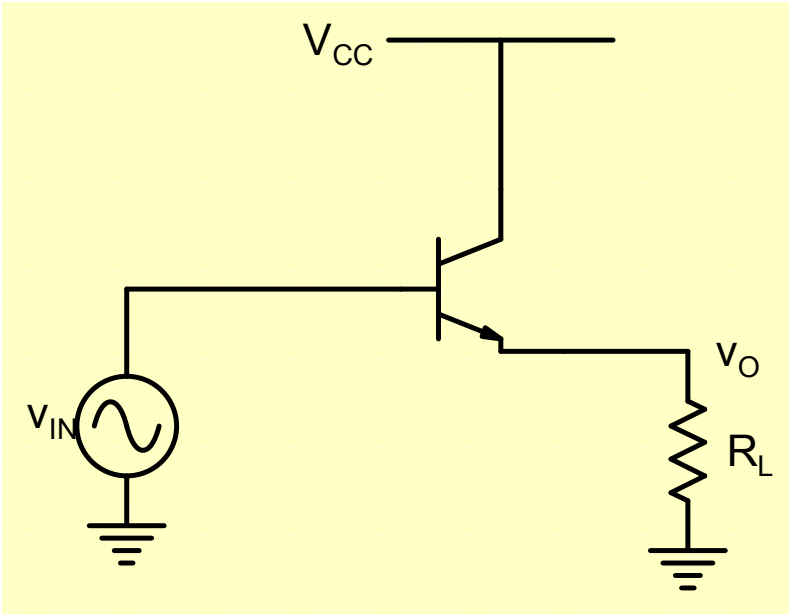


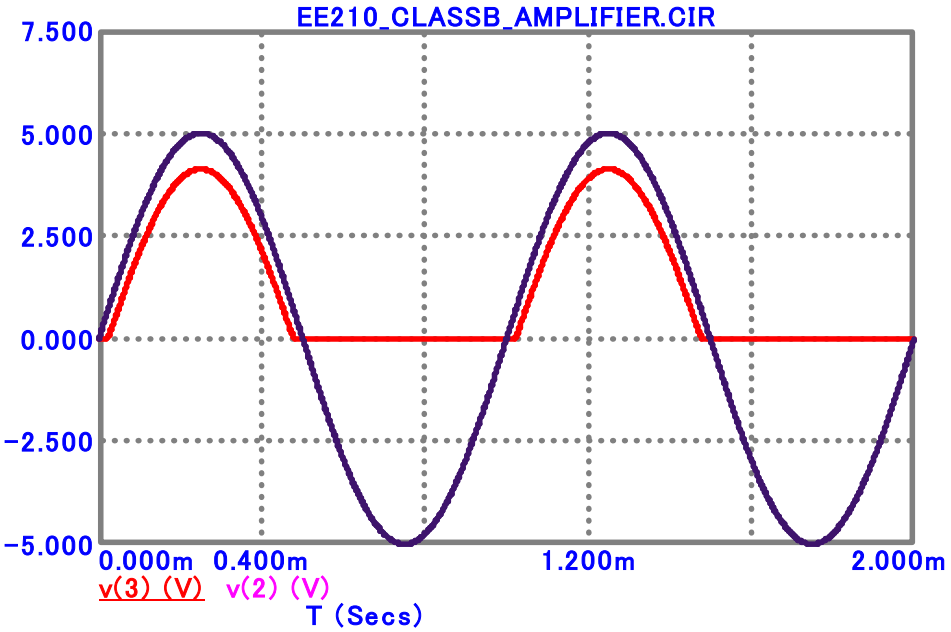


In Class A amplifiers, transistors need to be biased at a certain non-zero collector current so that no distortion occurs. As a consequence of this, even when no power is delivered to the load, power is taken from the supply.

An efficient amplifier should take power from the supply only when power is to be delivered to the load !

Amplifier with zero standby power

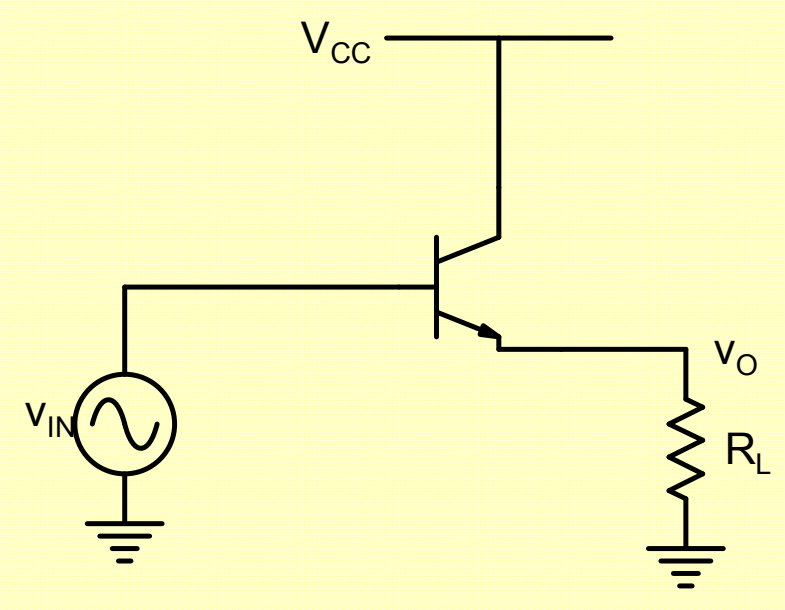


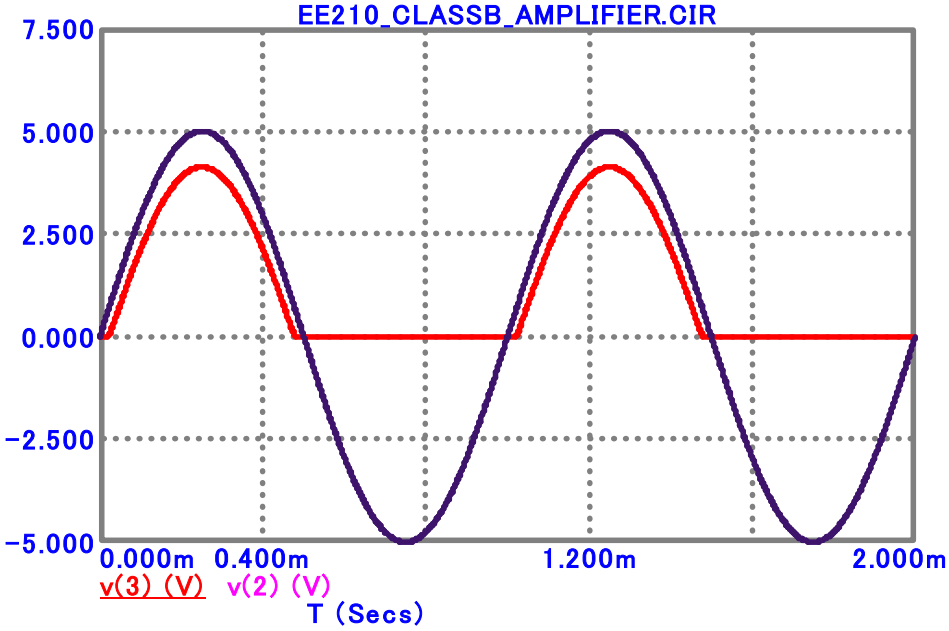


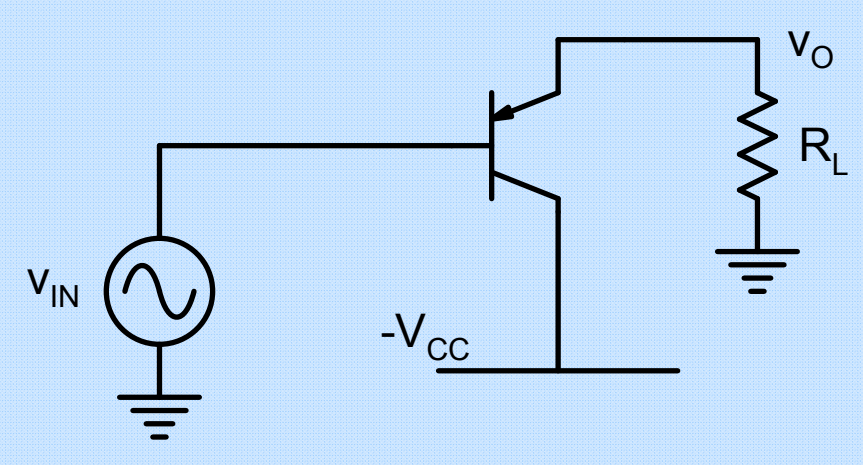
Although distorted, we can notice that this amplifier draws current from supply only when current is delivered to the load

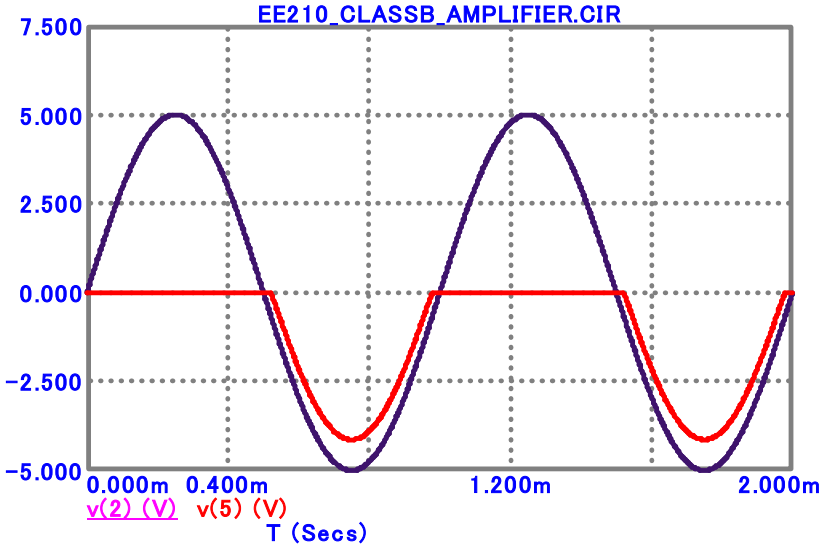
It can be shown that this amplifier has efficiency as large as 78.5% !

How do we reduce distortion?

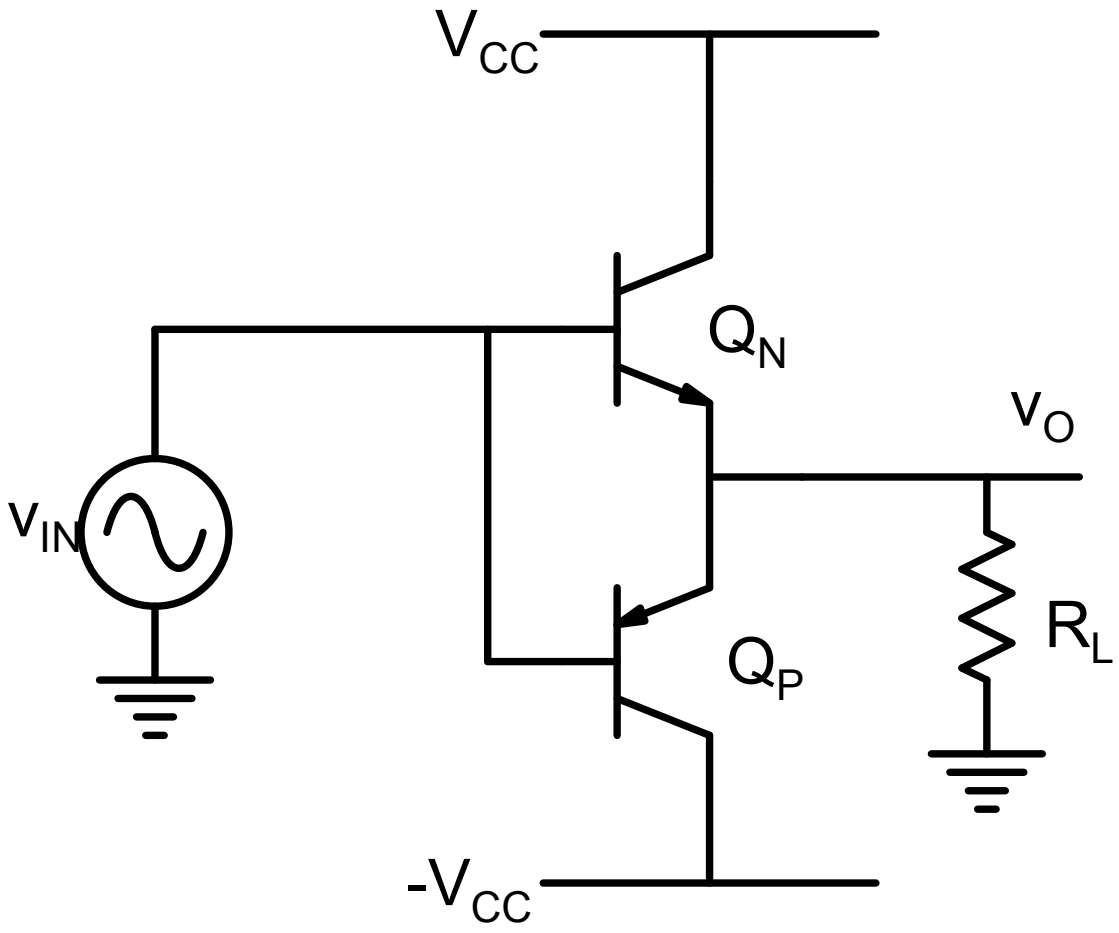




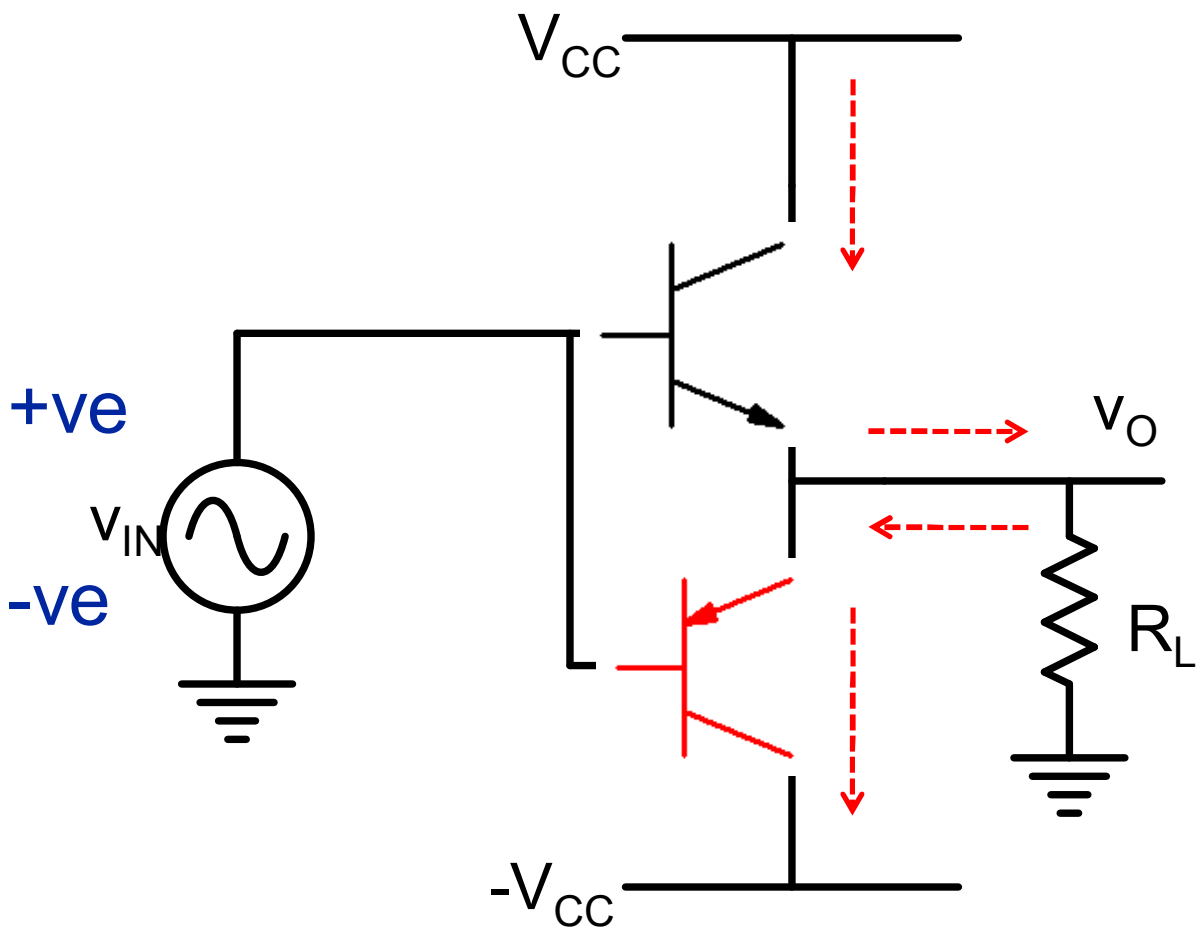




Natural solution is to combine both NPN and PNP stages



Class B amplifier: Each transistor conducts for half the sinusoidal cycle



Class B push-pull amplifier