

SRAM Compiler Design Plan v0.2

RIOS Lab

2023-01

Memory Compiler (AI based)

- **Key Feature**

- Advanced read / write assistant for advanced process node(beyond 7nm)
- First open-source high speed SRAM memory compiler

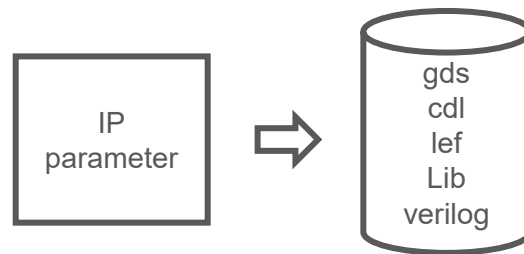
- **Challenge**

- Mixed-signal (digital+analog) high speed design
- May need fast spice simulator

- **Main configuration of memory macro**

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

Memory Compiler



Parameters		YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1
		Max	64	32	16
		Step	1	1	1
	ba = 2	Min	2	2	2
		Max	128	64	32
		Step	1	1	1

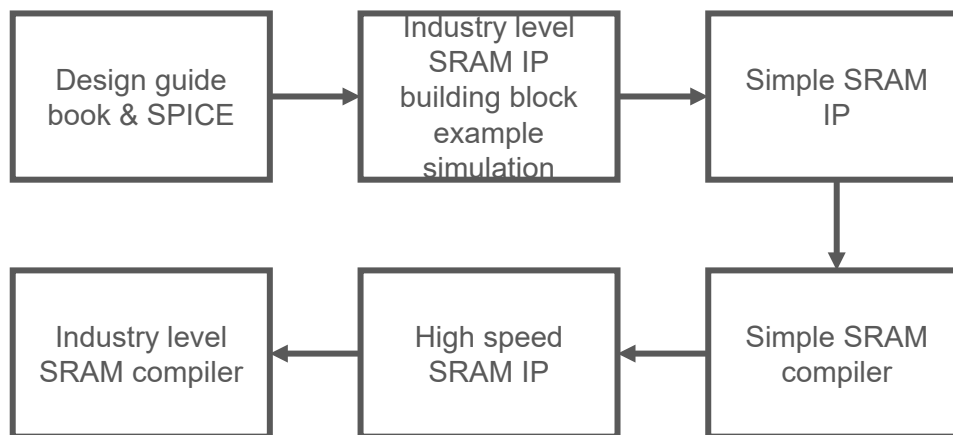
OpenXRAM

- OpenXRAM
 - A set of various, parameterized lib generators.
- Layout Generator(LEF/GDS)
 - Generates an array of custom, pitch-matched lef cells and final GDSII file.
- Schematic Generator & Netlister(CDL)
 - Generates a spice or CDL netlist which can be used for both LVS and functional verification.
- Function & Timing Model Generators(Lib/V)
 - Generates behavior simulation, dynamic/static timing analysis and synthesis models.

Ctrl & IO	Pre-Charge	BE	Pre-Charge	Pre-Charge	BE	Pre-Charge
	ARY	WL Dec & Driver	ARY	ARY	WL Dec & Driver	ARY
	CMUX&SA Datapath	LCtrl	CMUX&SA Datapath	CMUX&SA Datapath	LCtrl	CMUX&SA Datapath
	Datapath CMUX&SA	LCtrl	Datapath CMUX&SA	Datapath CMUX&SA	LCtrl	Datapath CMUX&SA
	ARY	WL Dec & Driver	ARY	ARY	WL Dec & Driver	ARY
	Pre-Charge	BE	Pre-Charge	Pre-Charge	BE	Pre-Charge

OpenXRAM

Design Stage



1 Introduction

2 IC design flow with EDA

2.1 Design flow

2.2 SPICE language

3 PDK and standard cell library

4 SRAM architecture

4.1 Simple architecture

4.2 Full typical architecture

5 SRAM timing

6 SRAM building block

6.1 Array

6.2 Decoder

6.2.1 WL decoder&driver

6.2.2 WL control (timing)

6.2.3 Pre-charge

6.2.4 Column mux

6.2.5 Pre-decoder

6.3 Read and write

6.3.1 Sense amp

6.3.2 Write driver

6.3.3 Datapath

6.4 Control

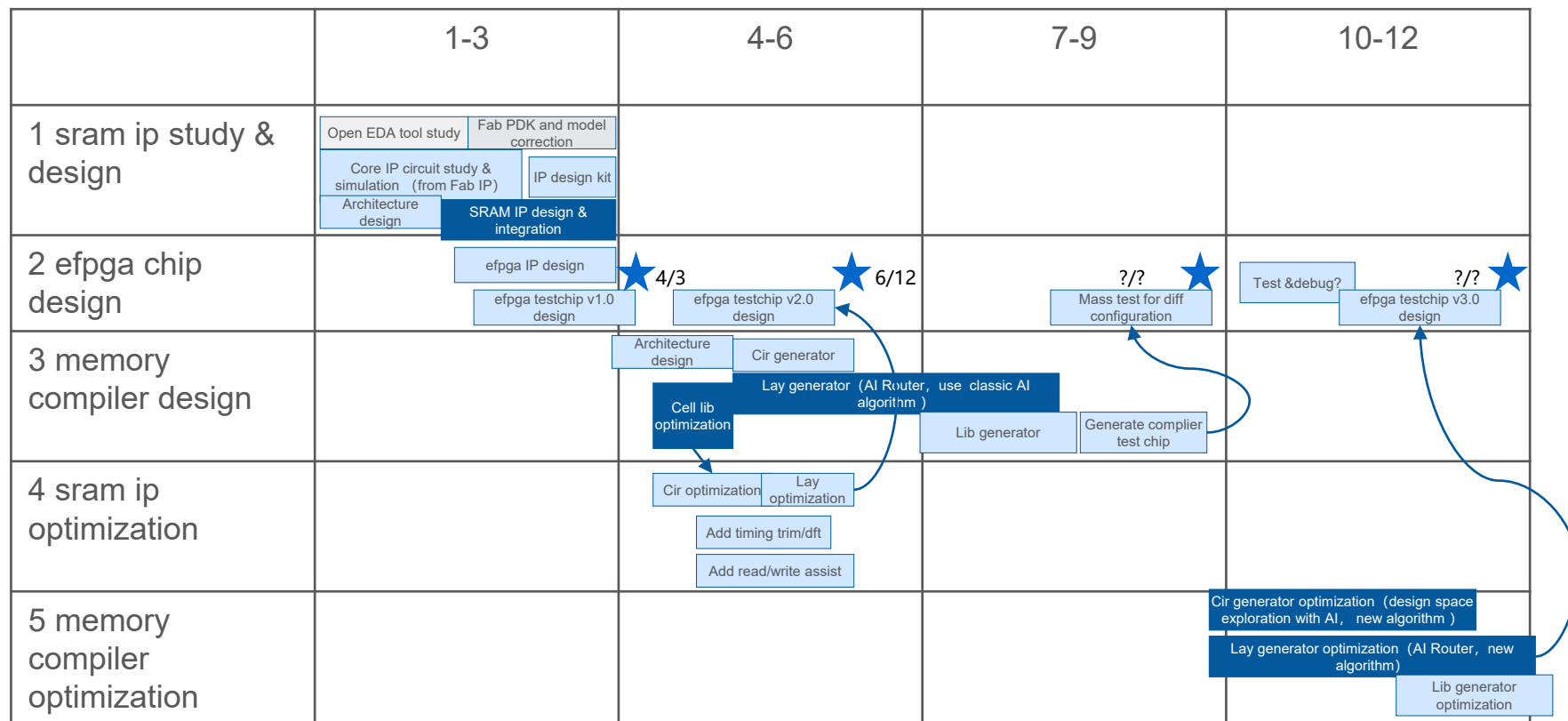
6.4.1 Control Unit

6.4.2 Timer

6.5 DFT (Optional)

7 Verification

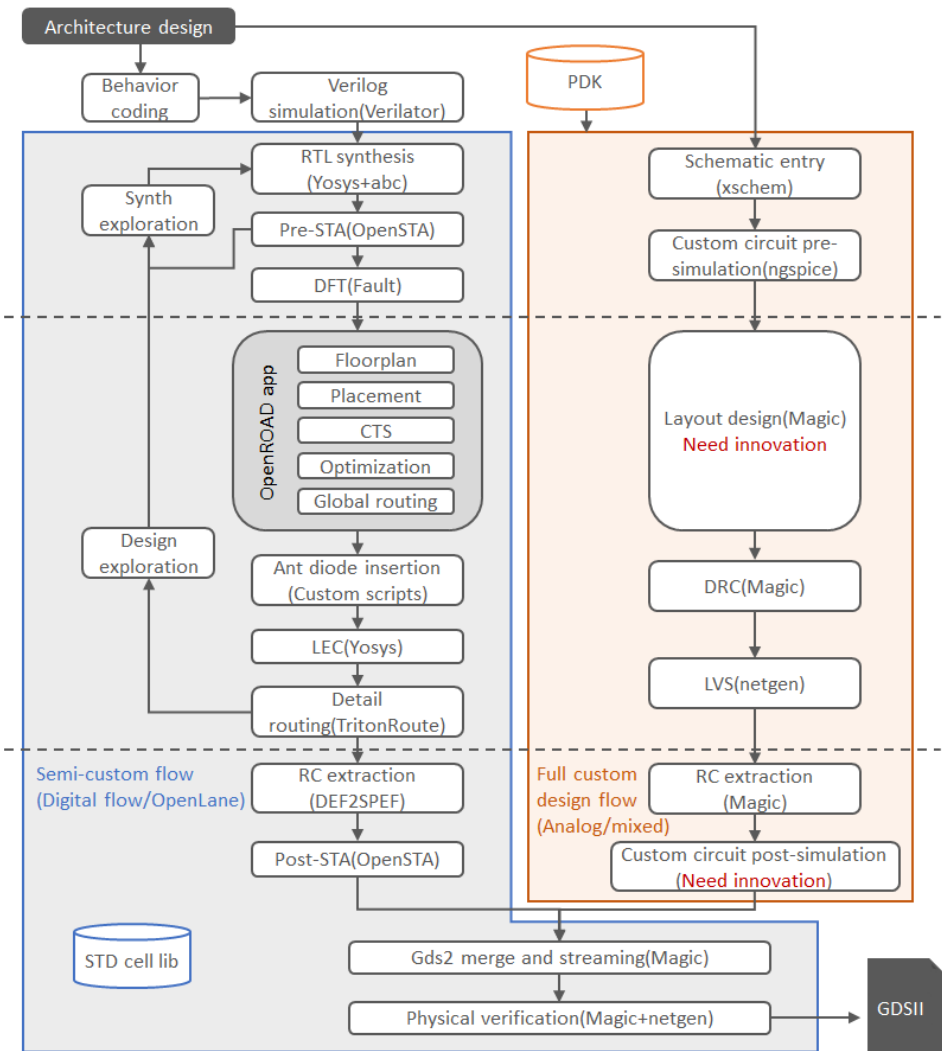
Memory Compiler (AI based) Roadmap



EDA Design Flow

• Design Flow

- Design with SPICE simulator
- Mixed-signal design flow
- **Based on OpenLane**
- Full custom design → Automation generator



High Performance Single Port SRAM Embedded Memory Macro

- **High performance Single Port SRAM Macro**

- 100 MHz operation
- 1-Clock cycle time
- Pipelined read access timing
- 32/64Bit wide data buses
- Byte write enables
- Simple standard SRAM interface

- **High Yield and Reliability**

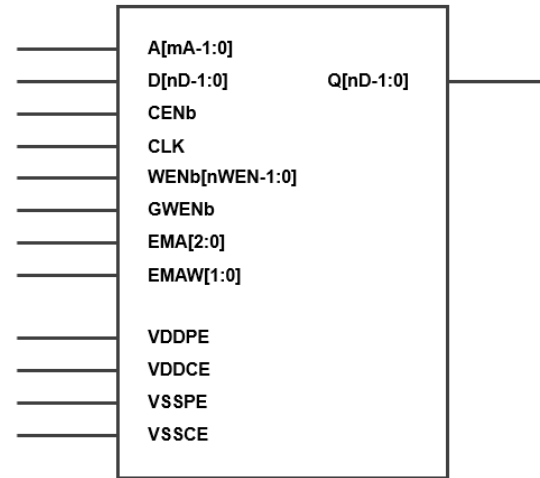
- Built-in redundancy for enhanced yield

- **Standard Logic Process**

- Skywater 0.13μm process with **open PDK**
- Logic design rules
- Uses 4 metal layers
- Routing over macro possible in layers 5 or more

- **Power**

- Single VDD voltage supply
- Low power consumption



Basic PINs

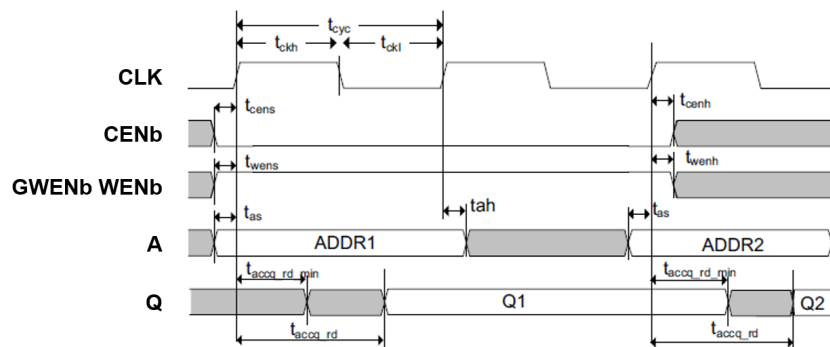
Name	Valid	Type	Description
A[mA-1:0]	positive CLK edge	Input	addresses (A[0] = LSB)
D[nD-1:0]	positive CLK edge	Input	data inputs (D[0] = LSB)
CENb	positive CLK edge	Input	chip enable, active LOW
CLK	clock	Input	clock
Q[nD-1:0]	positive CLK edge	Output	data outputs, Q[0] = LSB
WENb[nWEN-1:0]	positive CLK edge	Input	byte write enable, active LOW
GWENb	positive CLK edge	Input	global write enable, active LOW
VDDPE		Input	periphery power supply pin
VDDCE		Input	core array power supply pin
VSSPE		Input	periphery power ground pin
VSSCE		Input	core array power ground pin
EMA[2:0]	positive CLK edge	Input	extra margin adjustment, EMA[0] = LSB
EMAW[1:0]	positive CLK edge	Input	extra margin adjustment write, EMAW[0] = LSB

Multi-bank

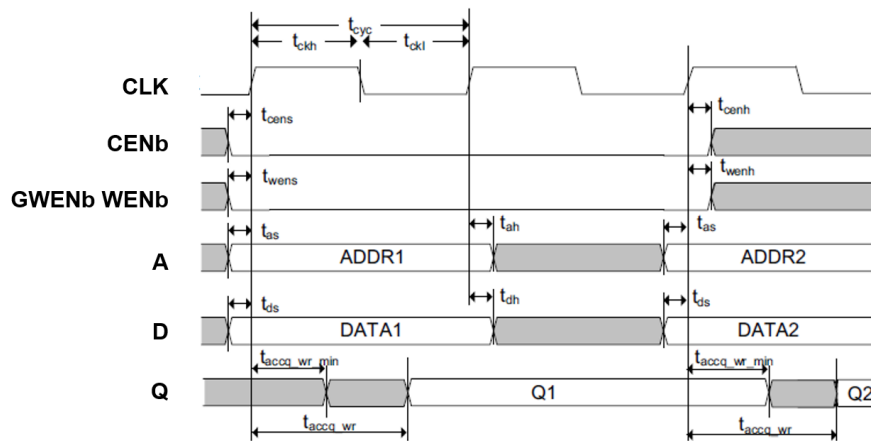
Ctrl & IO	Pre-Charge	BS	Pre-Charge	Pre-Charge	BS	Pre-Charge
	ARY	WL Dec & Driver	ARY	ARY	WL Dec & Driver	ARY
	CMUX&SA Datapath	LCtrl	CMUX&SA Datapath	CMUX&SA Datapath	LCtrl	CMUX&SA Datapath
	Datapath CMUX&SA	LCtrl	Datapath CMUX&SA	Datapath CMUX&SA	LCtrl	Datapath CMUX&SA
	ARY	WL Dec & Driver	ARY	ARY	WL Dec & Driver	ARY
	Pre-Charge	BS	Pre-Charge	Pre-Charge	BS	Pre-Charge

Multi-bank architecture to enhance performance

Timing



Read timing

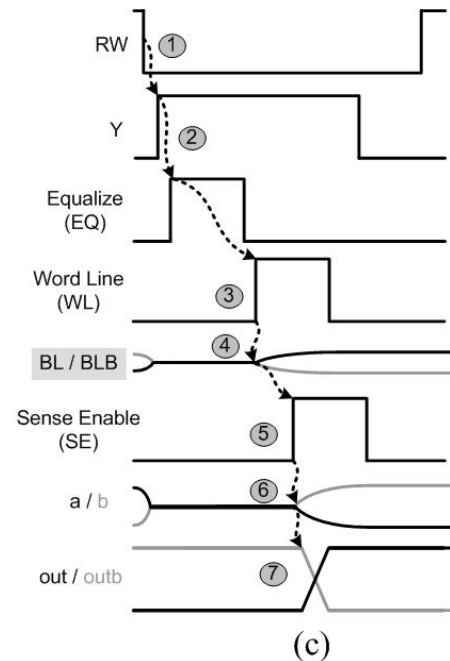
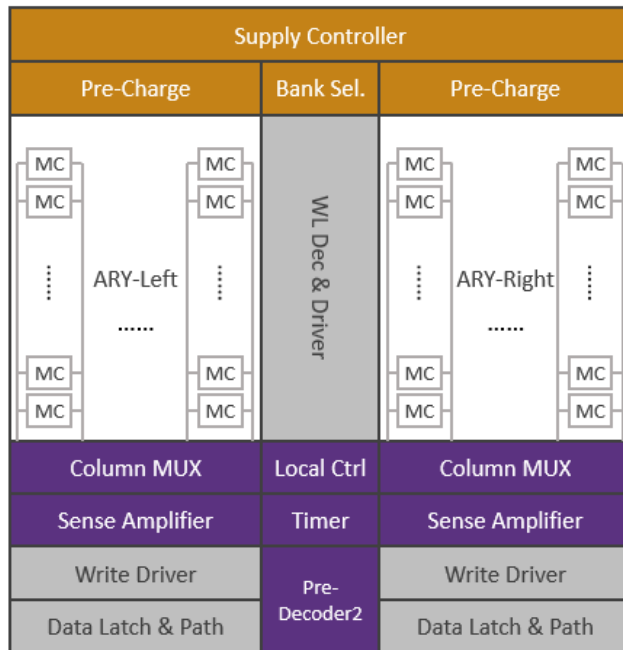


Write timing

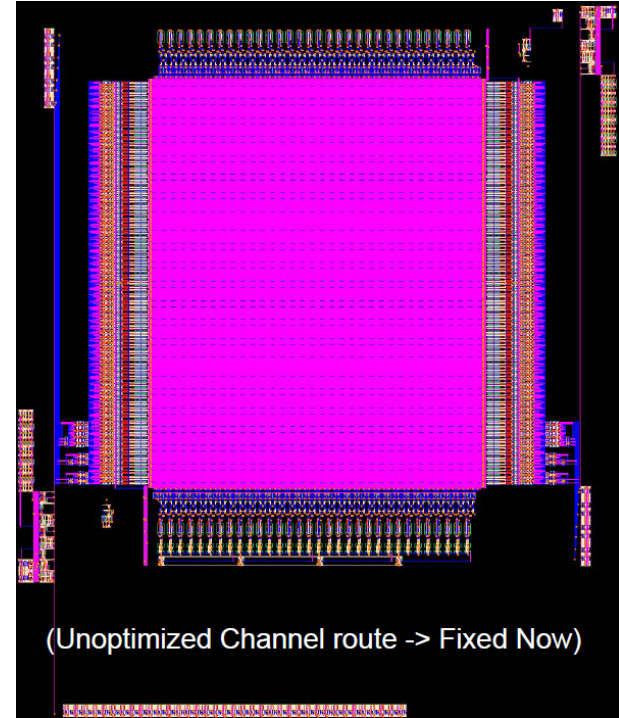
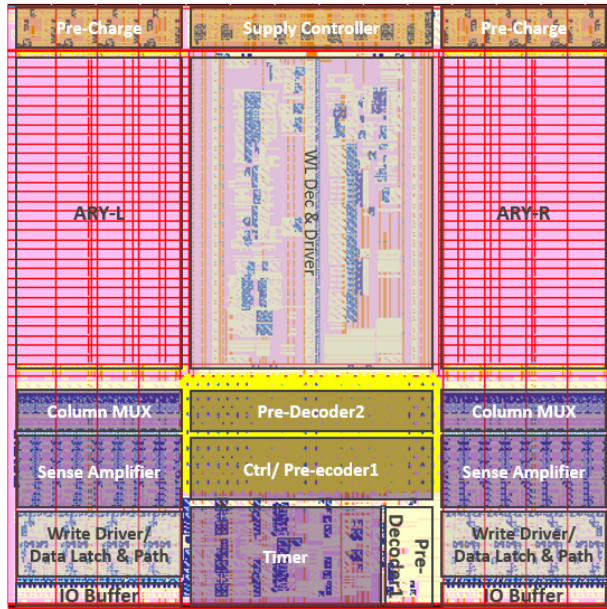
SRAM Base Architecture

• Build Block

- Array
 - WL decoder & driver
 - WL control (timing)
 - Pre-charge
 - Column mux
 - Pre-decoder
- Read and write
 - Sense amp
 - Write driver
 - Datapath
- Control
 - Control Unit
 - Timer
- DFT (Optional)



Industrial Level Layout



(Unoptimized Channel route -> Fixed Now)

OpenXRAM layout (Multi-array, left) v.s. OpenRAM layout(Right)

THANKS