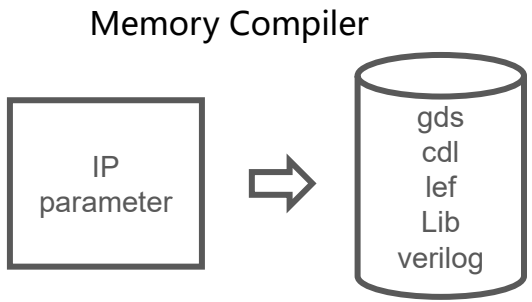
SRAM Compiler Design Plan v0.2

RIOS Lab

2023-01

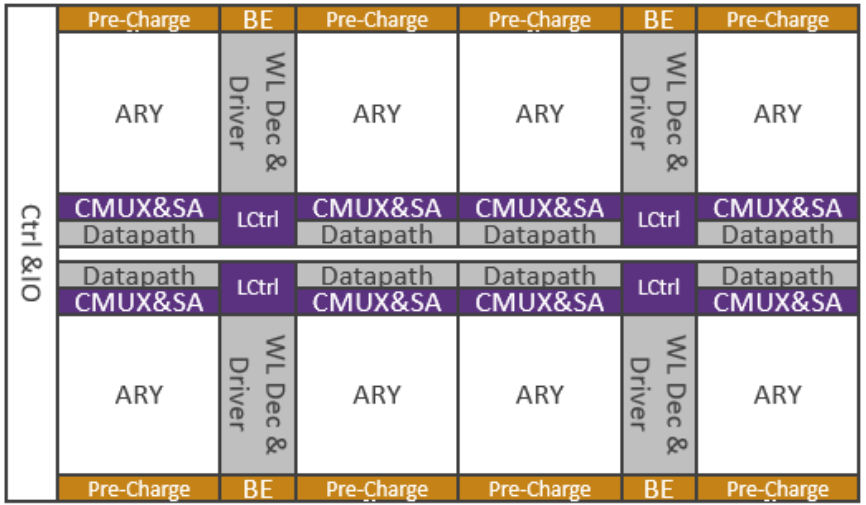
Memory Compiler（AI based）

- **Key Feature**
  - Advanced read / write assistant for advanced process node(beyond 7nm)
  - First open-source high speed SRAM memory compiler
- **Challenge**
  - Mixed-signal (digital+analog) high speed design
  - May need fast spice simulator



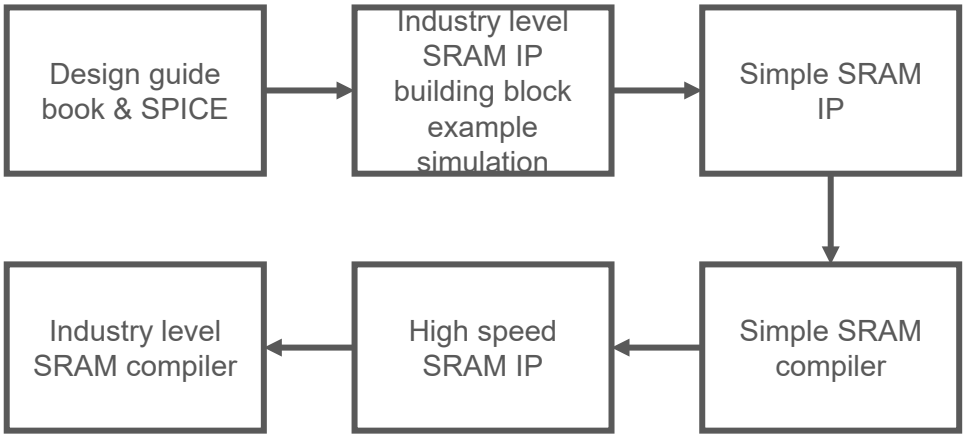
OpenXRAM

- OpenXRAM
  - A set of various, parameterized lib generators.
- Layout Generator(LEF/GDS)
  - Generates an array of custom, pitch-matched lef cells and final GDSII file.
- Schematic Generator & Netlister(CDL)
  - Generates a spice or CDL netlist which can be used for both LVS and functional verification.
- Function & Timing Model Generators(Lib/V)
  - Generates behavior simulation, dynamic/static timing analysis and synthesis models.



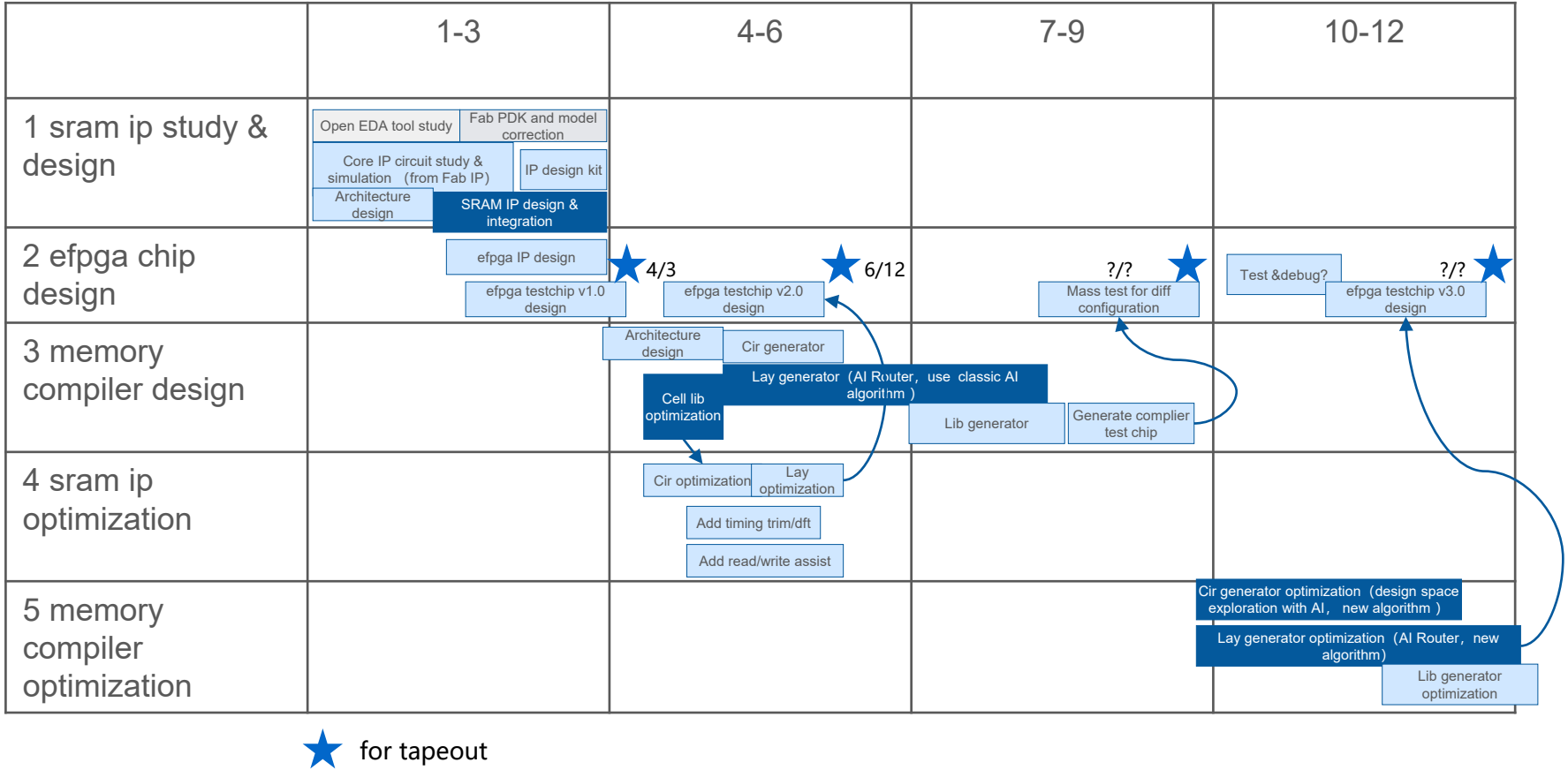
OpenXRAM

Design Stage



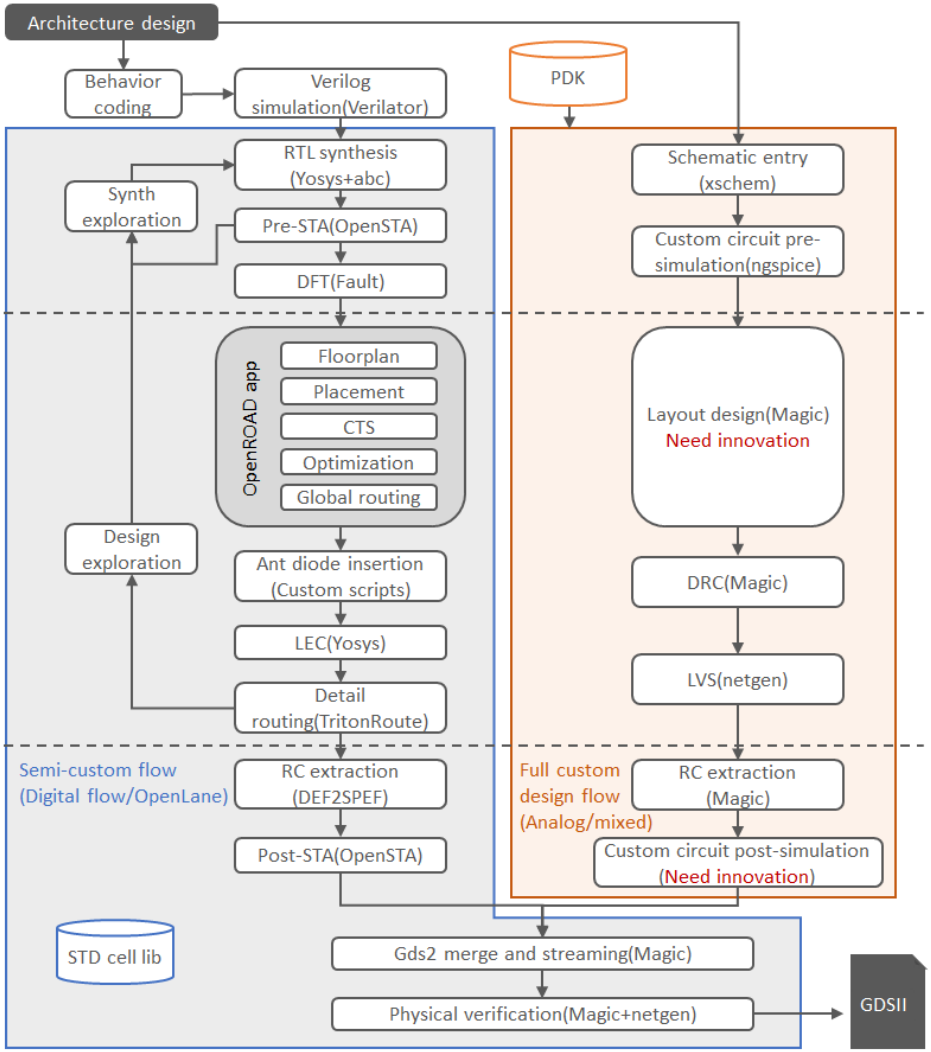
sram ip design guide-v0.1-202301

Memory Compiler（AI based）Roadmap



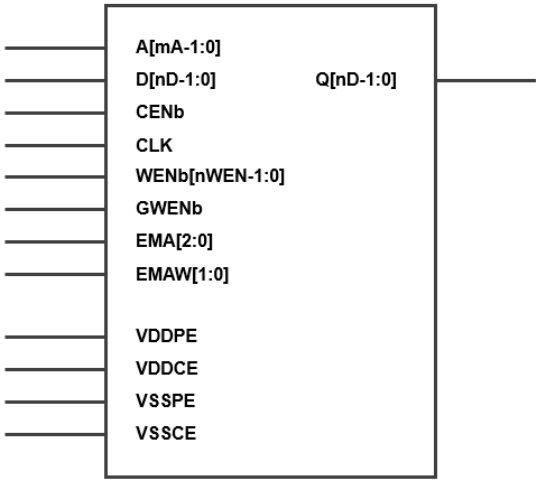
EDA Design Flow

- **Design Flow**
  - Design with SPICE simulator
  - Mixed-signal design flow
  - **Based on OpenLane**
  - Full custom design → Automation generator



High Performance Single Port SRAM Embedded Memory Macro

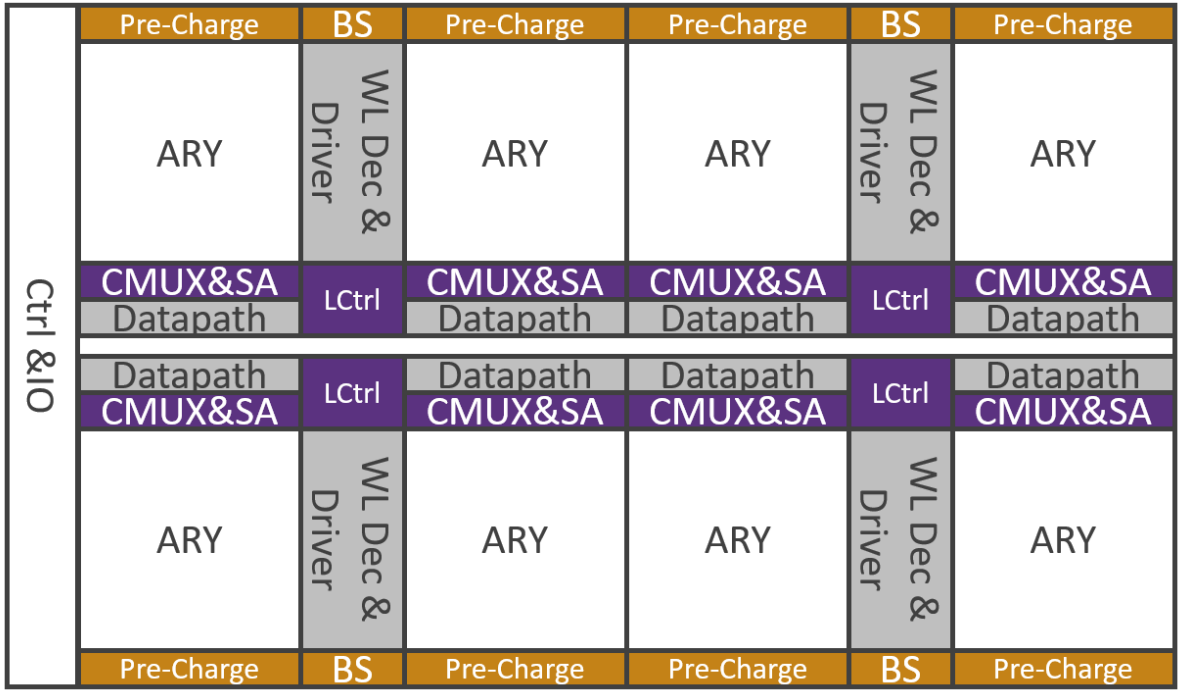
- **High performance Single Port SRAM Macro**
  - 100 MHz operation
  - 1-Clock cycle time
  - Pipelined read access timing
  - 32/64Bit wide data buses
  - Byte write enables
  - Simple standard SRAM interface
- **High Yield and Reliability**
  - Built-in redundancy for enhanced yield
- **Standard Logic Process**
  - Skywater 0.13µm process with **open PDK**
  - Logic design rules
  - Uses 4 metal layers
  - Routing over macro possible in layers 5 or more
- **Power**
  - Single VDD voltage supply
  - Low power consumption



Basic PINs

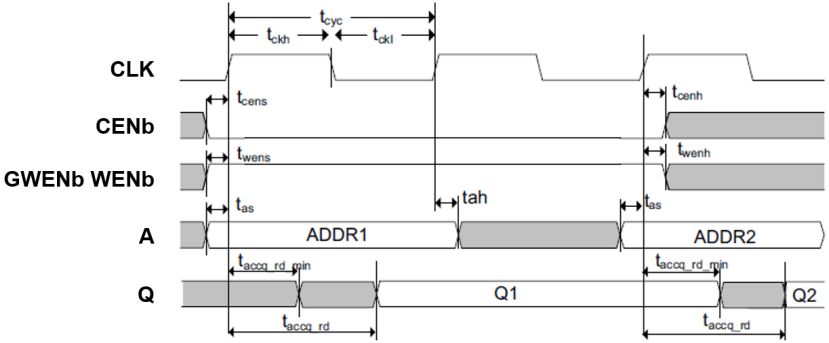
Name	Valid	Type	Description
A[mA-1:0]	positive CLK edge	Input	addresses (**A[0]** = LSB)
D[nD-1:0]	positive CLK edge	Input	data inputs (**D[0]** = LSB)
CENb	positive CLK edge	Input	chip enable, active LOW
CLK	clock	Input	clock
Q[nD-1:0]	positive CLK edge	Output	data outputs, **Q[0]** = LSB
WENb[nWEN-1:0]	positive CLK edge	Input	byte write enable, active LOW
GWENb	positive CLK edge	Input	global write enable, active LOW
VDDPE		Input	periphery power supply pin
VDDCE		Input	core array power supply pin
VSSPE		Input	periphery power ground pin
VSSCE		Input	core array power ground pin
EMA[2:0]	positive CLK edge	Input	extra margin adjustment, **EMA[0]** = LSB
EMAW[1:0]	positive CLK edge	Input	extra margin adjustment write, **EMAW[0]** = LSB

Multi-bank

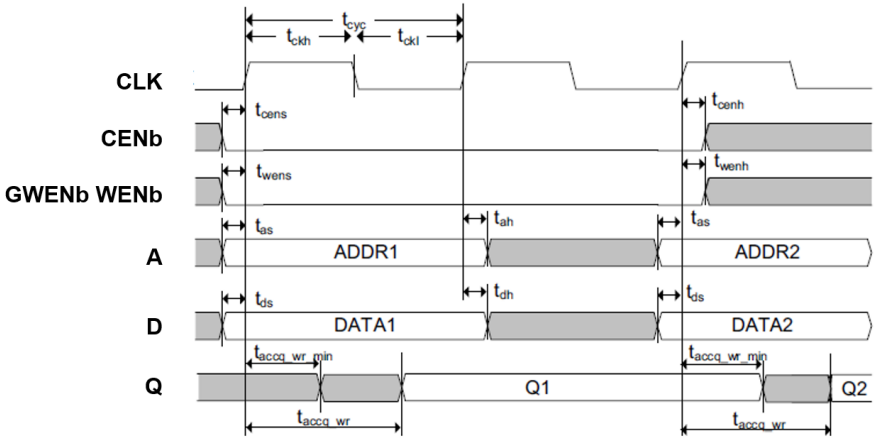


Multi-bank architecture to enhance performance

Timing



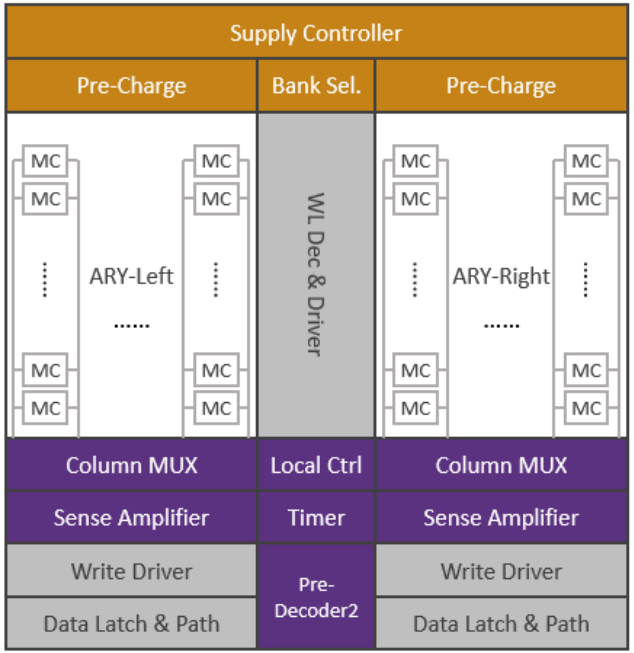
Read timing

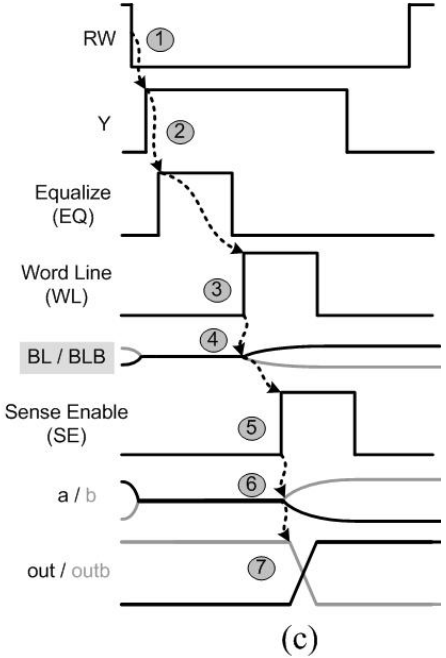


Write timing

SRAM Base Architecture

- **Build Block**
  - Array
  - Decoder
    - WL decoder & driver
    - WL control（timing）
    - Pre-charge
    - Column mux
    - Pre-decoder
  - Read and write
    - Sense amp
    - Write driver
    - Datapath
  - Control
    - Control Unit
    - Timer
  - DFT（Optional）





THANKS