Dual Stage CMOS Operational Amplifier Design in Sky-Water 130nm Technology

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2021 International Conference on Advances in Computing, Communication, and Control (ICAC3) | 978-1-6654-2634-3/21/$31.00 ©2021 IEEE | DOI: 10.1109/ICAC353642.2021.9697325

***Abstract*—A Two stage CMOS OPAMP with frequency compensation has been designed using open source Google's SkyWater 130nm Technology. This OPAMP operates at 1.8V of Vdd single supply voltage. This circuit has been designed and simulated using eSim open source EDA tool developed by IIT Bombay. Pre-layout simulations of OPAMP gives 62dB of voltage gain with Unity gain bandwidth of 20MHz. Post-layout simulations were carried out using open source MAGIC tool and Ngspice. Post-layout simulations of OPAMP gives 55dB of voltage gain with Unity gain bandwidth of 120MHz with output slew rate of 38 V/µs. It is a low power OPAMP with power consumption of 54µW.**

Keywords— eSim EDA tool; Sky-Water 130nm Technology; Operational Amplifier; Gain Bandwidth Product; CMRR; SR.

I. INTRODUCTION

In the last few years, Semiconductor Industry has transformed from micro-technology to Nano-technology. From few micron process it has come to a 7nm process node. Post Covid19 Pandemic the world is facing a global chip shortage. So to combat this crisis an initiative "Tape-Out World" has been taken by Google, efabless and many such organizations.

OPAMP i.e. Operational Amplifier is basic building block of most of the analog and mixed signal circuits. Op-amp consists of Bias circuit, 1st stage Differential Amplifier stage, 2nd stage of Common source amplifier, Compensation circuit and Output Buffer stage if required based on load. Vast applications of opamp includes the basic DC as well as AC amplification, filtering, signal conditioning, analog to digital converters, Digital to analog converters, mathematical functions such as integration and differentiation. One of the very important application that is Instrumentation amplifier uses opamp as basic element to amplify sensor signals (in few millivolts) to some of volts [1]. Dual stage Opamp with RC compensation designed with 180 nm process node [2] operated at 1.8 V single supply gives unity gain bandwidth of 140 MHz but its input is bias dependent.

This paper uses Google's SkyWater 130nm Open source Process node [3] to design two stage OPAMP with necessary frequency compensation using RC compensation for stability. The required bias voltage i.e. 0.7 V has been generated with the help of NMOS and pull up resistor separately and has been indicated by OPAMP bias block in schematic. This paper uses eSim v 2.1 open source EDA tool [4] developed by FOSSEE, IIT Bombay for the circuit simulation. The schematic is made in KiCad and the Spice netlist is generated by Kicad to Ngspice conversion. This Spice netlist is then edited to include sky130 device model libraries and then run again to get pre-layout simulation results. Open source MAGIC layout editor tool [5] is used to draw the layout. By using a "ext2spice" command in tkon window of magic tool spice netlist is generated. This spice netlist is then edited to include sky130 device model libraries. This spice file is then run into ngspice [6] to view post-layout results.

The flow of a Paper: Proposed two stage Opamp circuit design with steps is presented in Section II. Section III and IV includes Pre-layout and Post-layout simulation results and discussions respectively. Section V concludes the design of the proposed Op-amp circuit followed by the Acknowledgement section VI.

II. PROPOSED OPAMP CIRCUIT DESIGN

General specifications of Opamp such as open loop gain, Phase margin, Gain Bandwidth Product, Slew Rate, CMRR, settling time, Output voltage swing are considered while designing the Opamp circuit [7]. Fig 1 shows the general structure of two stage Opamp with frequency which consists of opamp bias, Input Differential stage, RC compensation network and last i.e high gain common source amplifier stage. This Opamp is designed with the single supply voltage of 1.8V to get basic performance parameters as follows:

- Phase margin > 60º
- Open loop gain > 60 dB
- Unity Gain Bandwidth > 10MHz
- Slew Rate > 10 V/us

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- Output Voltage swing > 900mVpp
- CMRR > -20dB

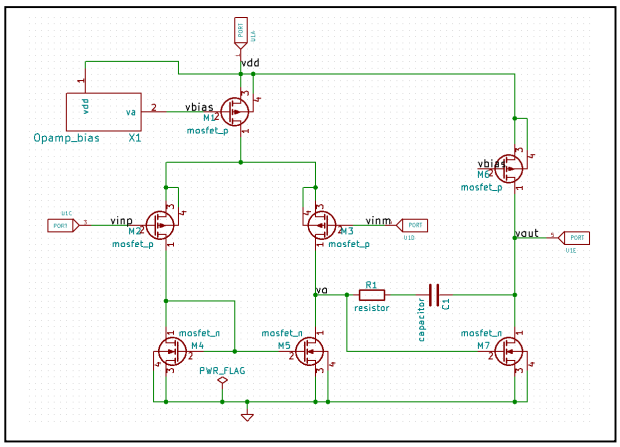


Fig. 1 OPAMP Schematic drawn in eSim.

The OPAMP design steps are as follows.

A. *OPAMP Bias Circuit:*

Opamp Bias circuit generates the required bias voltage i.e. Vbias which is then applied to 1st Input Differential Amplifier stage i.e. M1 PMOS transistor and 2nd High gain common source amplifier stage. This Bias circuit is designed using a single NMOS in series with a pull up resistor.

B. *First Stage: Input Differential Amplifier Circuit*

First stage of amplification consists of a PMOS differential pair as driver and current mirror NMOS pair as load. Differential input voltages Vinp and Vinm are applied to P MOSFETs M2 and M3 respectively. P channel MOSFETs are used as drivers because they have lower noise than N channel MOSFETs. This P MOS pair will convert input differential voltages into equivalent differential currents. These differential currents are then applied to the current mirror circuit formed by NMOS pair transistors M4 and M5. To achieve symmetry and matching following aspect ratios conditions must be satisfied. W/L$_{M2}$ = W/L$_{M3}$ and W/L$_{M4}$ = W/L$_{M5}$.

The output differential current produced by this 1st differential input stage is given by

$$Io = gm2(vinp - vinm) \quad (1)$$

$$gm2 = \sqrt{2kp'(\frac{w}{l})Id2} \quad (2)$$

First stage Gain, $Av1 = -\frac{gm2}{(gdm3+gdm4)}$ (3)

C. *Second Stage: CS Amplifier Voltage Gain Stage*

Second stage of amplification includes common source NMOS M7 transistor and its current source PMOS M6 transistor as a load. This stage provides a high gain and also helps to achieve frequency compensation with the help of compensating capacitor C1.

Second stage Gain, $Av2 = -\frac{gm7}{(gdm7+gdm6)}$ (4)

Therefore Total Gain, $Av = Av1 + Av2$

Gain Bandwidth Product, $GBW = \frac{gm2}{C1}$ (5)

Zero, $wz1 = \frac{gm7}{C1}$ (6)

Output Pole, $wp2 = \frac{gm7}{CL}$ (7)

The Slew Rate is given by $SR = \frac{ID1}{C1}$ (8)

Phase Margin of 60ºis accepted for most of the OPAMP applications. So to have a minimum of 60º Phase margin, compensation capacitor value C1 > 0.22C$_L$ is selected.

D. *Frequency Compensation Circuit*

Frequency compensation circuit consists of a series combination of Resistor R1 and Capacitor C1 connected between first stage output Vo and second stage output Vout as shown in fig. 1. This compensation capacitor C1 provides the stability of OPAMP by attaining Phase Margin more than 60º. The Resistor R1 in series with C1 is responsible for translating RHP zero into LHP. Table I shows the aspect ratios of all the transistors

TABLE I. DEVICE PARAMETERS OF OPAMP CIRCUIT

Device	W/L	Device	W/L
M1	20/1	M5	20/1
M4	20/1	M6	20/1
M2	50/1	M3	50/1
M7	50/1	R1	290 Ω
		C1	0.5pF

III. PRE LAYOUT SIMULATION RESULTS

The proposed circuit has been designed using Google's SkyWater 130nm process design kit (PDK) and circuit simulation has been done using eSim Open Source EDA tool developed by FOSSEE IIT Bombay. Magic Layout editor and Ngspice is used to carry out post layout simulations. Table II shows the SkyWater 130nm Process parameters.

TABLE II. SKYWATER 130 nm PROCESS PARAMETERS (0.13 MICRON)

Process parameters	NMOS	PMOS
Vt (V)	0.634	0.949
Process Trans-conductance ($\mu A/V^2$)	113.19	61.50

The OPAMP circuit simulation is done using a single power supply of 1.8 V. Fig.2 shows the transient response of opamp. For the input peak to peak signal voltage of 1mv, Vout swings from 0V to 1.4 V. AC analysis of the proposed circuit has been shown in Fig. 3. In that (a) shows the Differential mode gain ADM which is 62dB also Unity gain Bandwidth is found to be 30MHz.

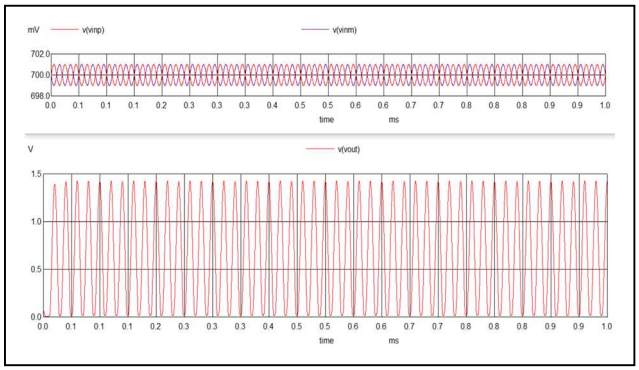
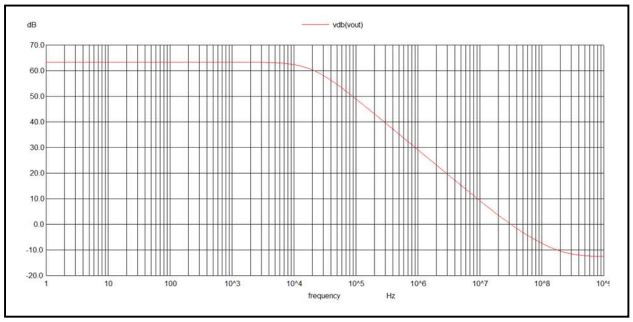
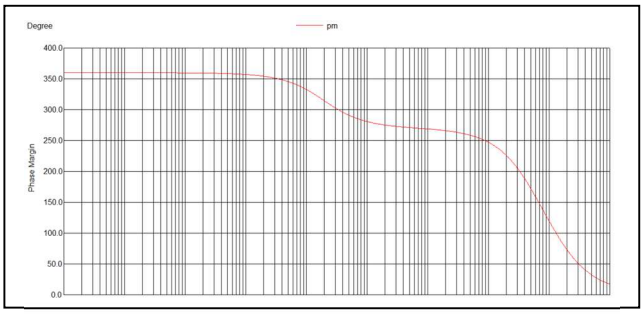


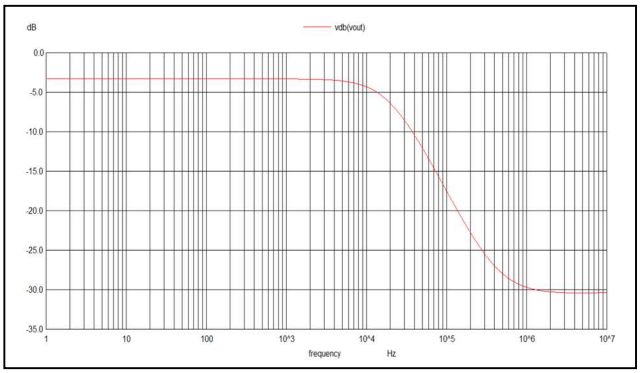
Fig. 2 Pre-Layout Transient Response of OPAMP.



(a) Differential Mode Gain (ADM) Magnitude Response



(b) Phase Margin Plot



(c) Common Mode Gain (ACM) Plot

Fig. 3. Pre-Layout Frequency Response of OPAMP

Fig. 3b shows the direct phase margin (PM) plot of OPAMP where it can be observed that this circuit gives a very good phase margin of 200º keeping the op-amp stable. The common mode gain ACM plot is shown in fig. 3c. Fig. 4 shows the slew rate of OPAMP in pre layout simulation. It gives a Rise slew rate of 14.22 V/µS and fall slew rate of 15.55 V/µS.

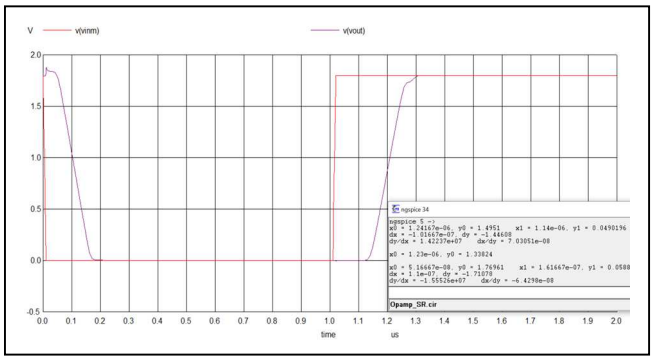


Fig. 4. Pre-Layout Simulation Result of Rise and Fall Slew Rate

IV. POST LAYOUT SIMULATION RESULTS

The layout of OPAMP drawn using Magic layout is shown in Fig.5. Post layout simulation is then performed on the extracted spice netlist using Ngspice.

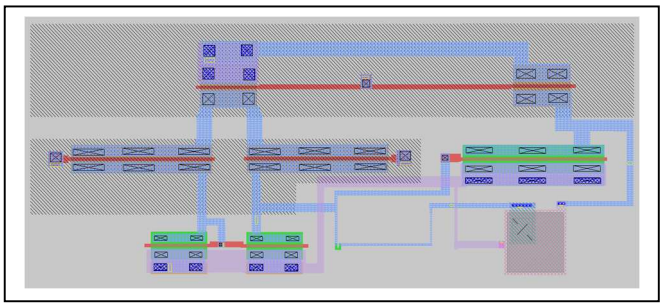


Fig. 5. Layout of Two Stage OPAMP drawn in MAGIC Tool

Fig. 6 shows post layout transient response of OPAMP. For input voltage of 1mv, full swing output voltage of 1.8 V is obtained. It gives a Rise slew rate of 38.66 V/µS and Fall slew rate of 43.13 V/µS as shown in fig. 7.

Fig. 6. Post-Layout Transient Response of OPAMP.

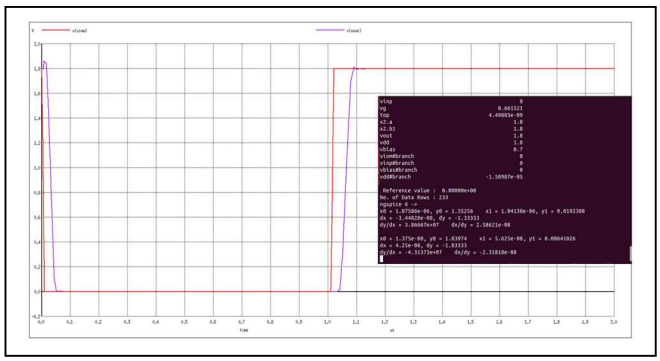
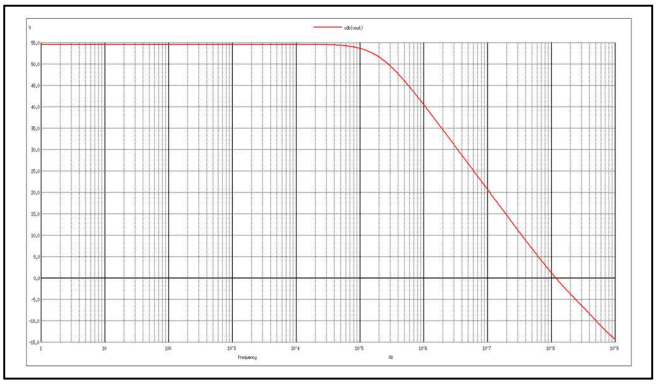
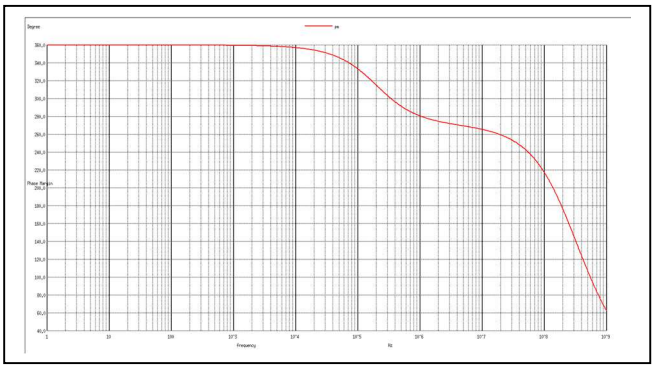


Fig. 7. Post-Layout Simulation Result of Rise and Fall Slew Rate

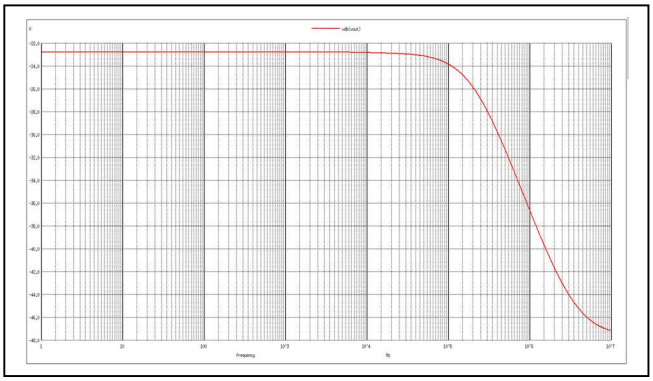
Fig. 8 shows post layout ac analysis results of OPAMP. It gives 55dB of Differential mode gain (ADM) and -23 dB of Common mode gain (ACM) resulting in 78 dB of Common mode rejection ratio (CMRR). Fig. 8b shows the Phase Margin plot of OPAMP. It offers 210⁰ of Phase margin at unity gain frequency. Power consumption by OPAMP circuit is calculated from the transient analysis. It draws 30 µA of supply current with 1.8 V of supply voltage consuming very less power as 54 µW.



(a) Differential Mode Gain (ADM) Magnitude Response



(b) Phase Margin Plot



(c) Common Mode Gain (ACM) Plot

Fig. 8. Post-Layout Frequency Response of OPAMP

The simulation results of Opamp (Pre-layout and Post-layout) are shown in Table III. From the comparative analysis it can be observed that post-layout values are in good approximation with pre-layout values. Except for Differential mode gain, performance is found to be improved in post-layout simulation for other performance parameters.

TABLE III. PRE-LAYOUT AND POST-LAYOUT SIMULATION RESULTS

Parameter	Pre-layout Values	Post-layout Values
ADM0	63 dB	55 dB
ACM0	-5 dB	-23 dB
Phase Margin	200º	210º
Slew Rate (Rise)	14.22 V/µS	38.66 V/µS
Slew Rate (Fall)	15.55 V/µS	43.13 V/µS
Output Voltage Swing	1.4 V	1.8 V
Power Consumption	59 µW	54 µW

V. CONCLUSION

A Two stage CMOS Operational Amplifier with frequency compensation technique has been designed using Google's Sky-Water 130nm open source process design kit. Pre-layout circuit simulation is performed using eSim (Open Source EDA tool developed by FOSSEE IIT Bombay) and then verified with post-layout simulation results obtained with Magic layout tool and Ngspice. This two stage OPAMP provides a stable operation with a High gain of 55 dB and large CMRR of 78 dB providing very good noise signal rejection. It operates over a very large bandwidth with a Gain-Bandwidth product of 120 MHz and that too with very less power consumption i.e. 54 µW.

VI. ACKNOWLEDGEMENT

The author would like to thank Prof. Kannan Moudgalya FOSSEE, IIT Bombay and Mr. Kunal Ghosh Co-founder at VSD Corp. Pvt. Ltd. for conducting nationwide eSim circuit design marathon using fully open source Skywater 130nm technology. This Paper is the extended work of the project that has been done in a marathon.

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