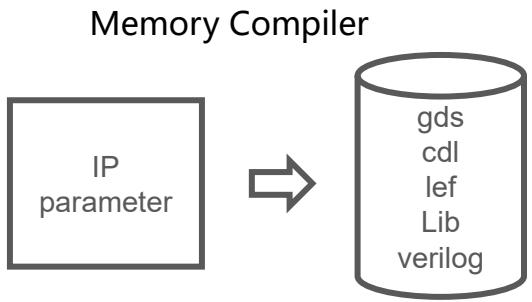
SRAM Compiler Design Plan v0.1

RIOS Lab

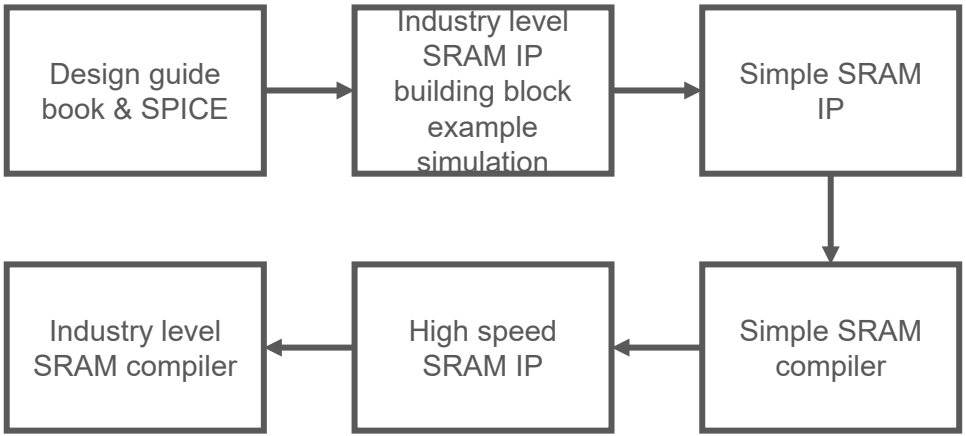
2023-01

Memory Compiler（AI based）

- **Key Feature**
  - Advanced read / write assistant for advanced process node(beyond 7nm)
  - First open-source high speed SRAM memory compiler
- **Challenge**
  - Mixed-signal (digital+analog) high speed design
  - May need fast spice simulator

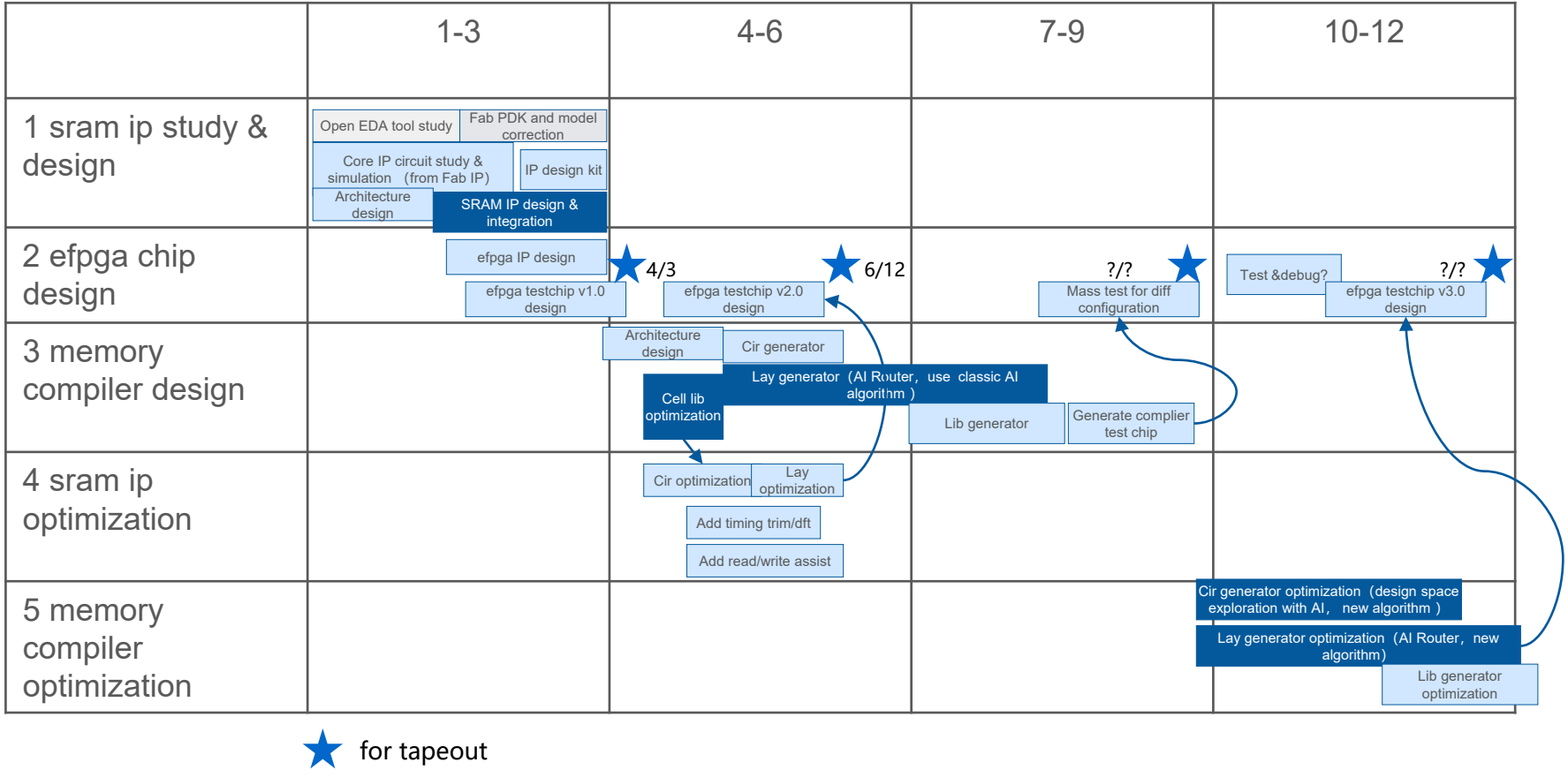


Design Stage



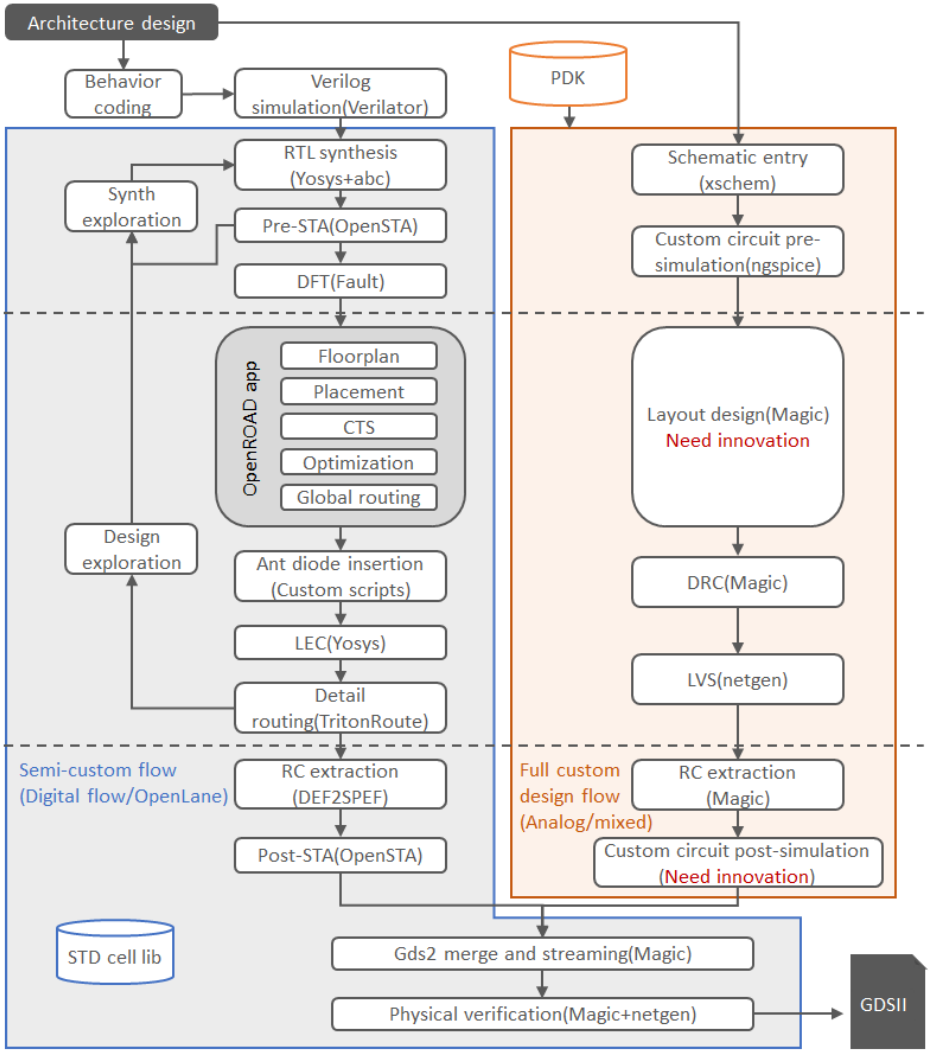
sram ip design guide-v0.1-202301

Memory Compiler（AI based）Roadmap

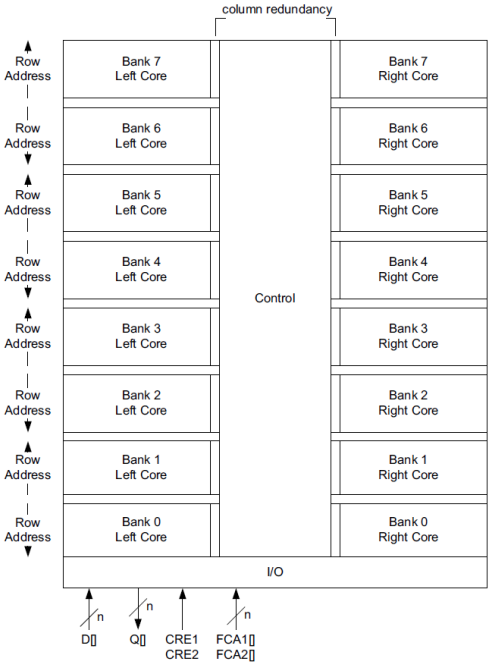


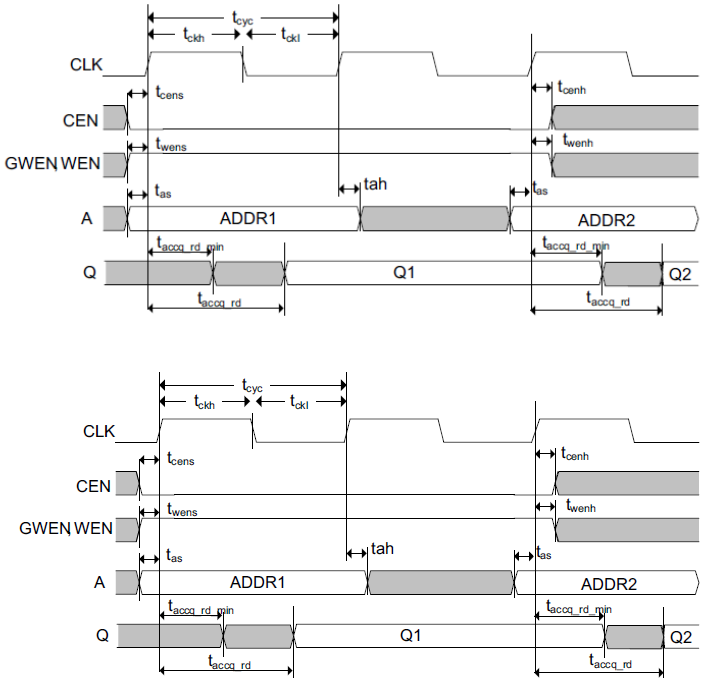
EDA Design Flow

- **Design Flow**
  - Design with SPICE simulator
  - Mixed-signal design flow
  - OpenLane
  - Full custom design → Automation generator



Multi-bank and Timing

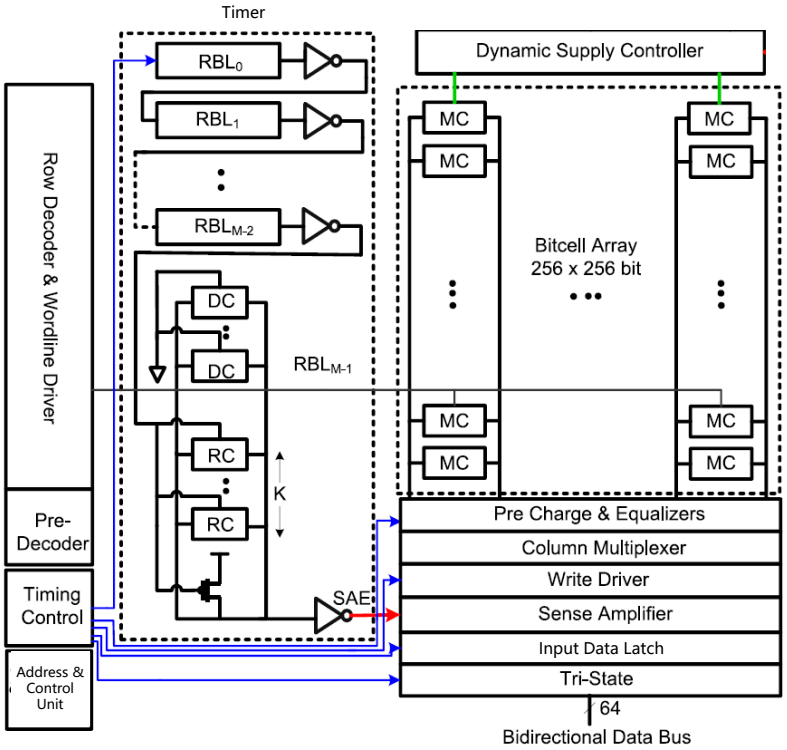


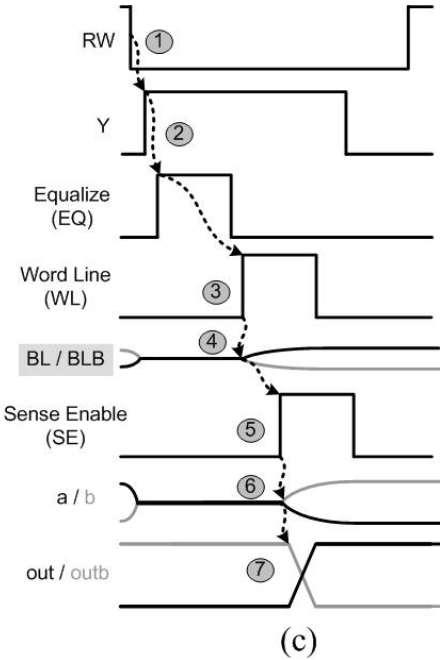


Multi-bank architecture to enhance performance

SRAM Base Architecture

- **Build Block**
  - Array
  - Decoder
    - WL decoder & driver
    - WL control (timing)
    - Pre-charge
    - Column mux
    - Pre-decoder
  - Read and write
    - Sense amp
    - Write driver
    - Datapath
  - Control
    - Control Unit
    - Timer
  - DFT (Optional)
- **Timing**





THANKS