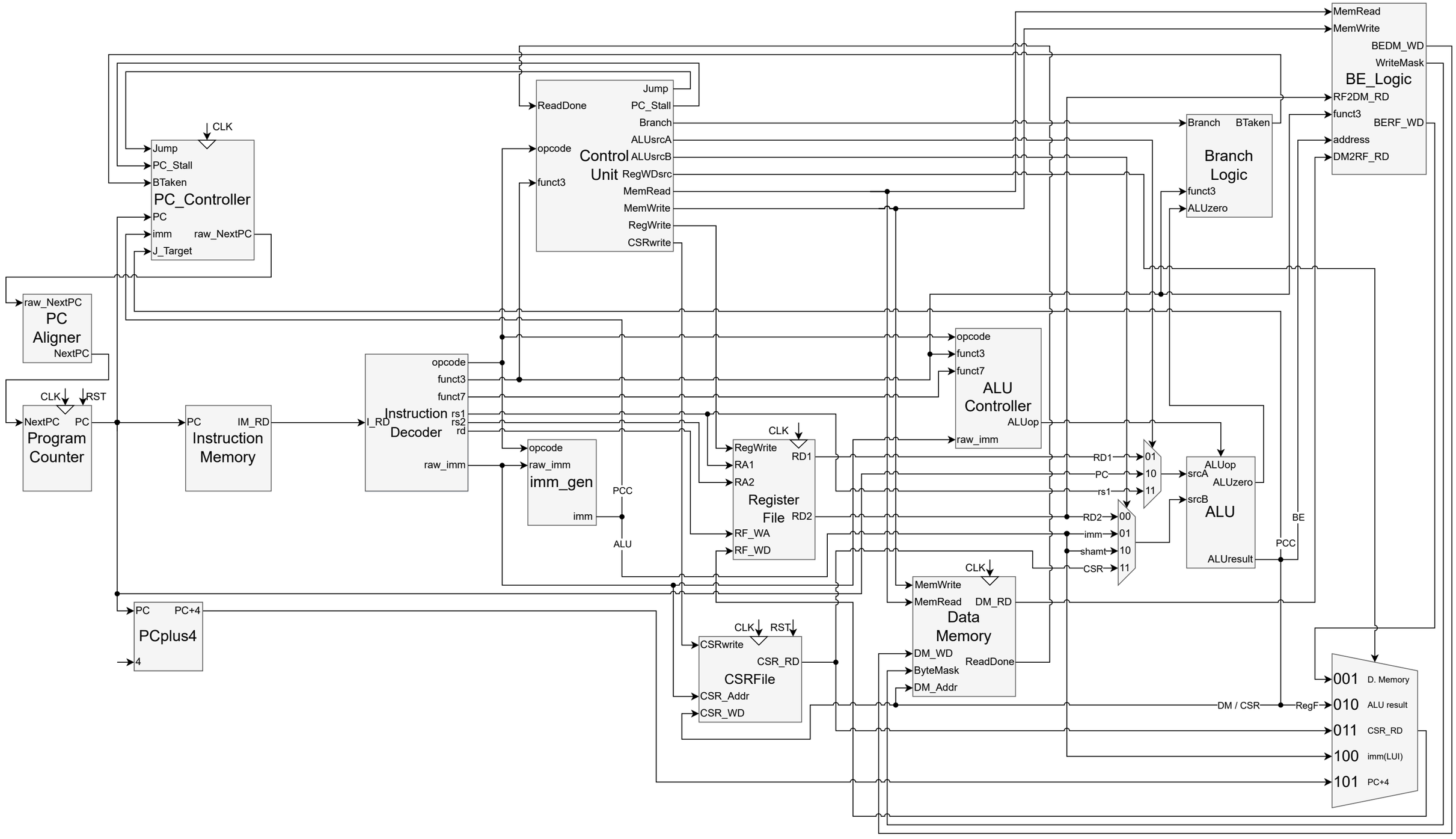

KHWL_RV32I43F.R2

One of Final version of milestone; RV32s project.
R2 : Read Done, PC_Stall signal for *Data Memory's Read operation issue*. PCC's Misalign handling delegated to PC_Aligner. Misaligned memory write operates as HINT. Supports 43 Instructions with CSR File added base modules. (37F Architecture's 37 Instructions + Zicsr 6 Instructions = 43)
Misaligned Address access is in PC_Aligner by making lower 2 bits 0. (2'b0)

23:00 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.06(木)