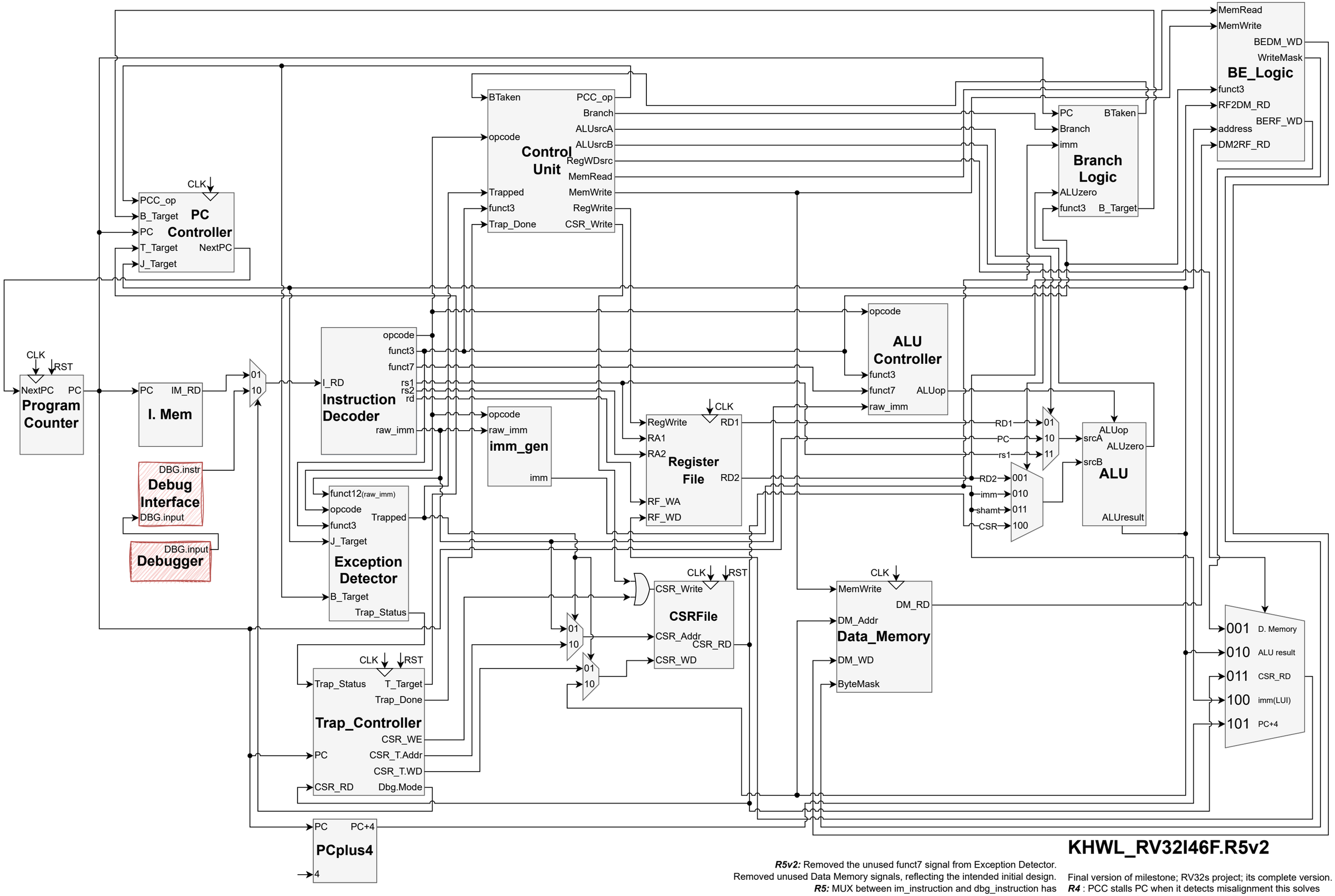

KHWL_RV32I46F.R5v2

Final version of milestone; RV32s project; its complete version.
R4 : PCC stalls PC when it detects misalignment this solves **next_pc freeze issue**. It was because PC works at posedge clk.
R3 : PCC_op signal for **next_pc race condition issue**
R2: Non-cache version of RV32I47NF.R1 revision of 46F is synced.
Supports 46 Instructions including EBREAK, ECALL, mret.

R5v2: Removed the unused funct7 signal from Exception Detector.
Removed unused Data Memory signals, reflecting the intended initial design.
R5: MUX between im_instruction and dbg_instruction has been extracted back to top-module.

22:12 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.05.18(日)