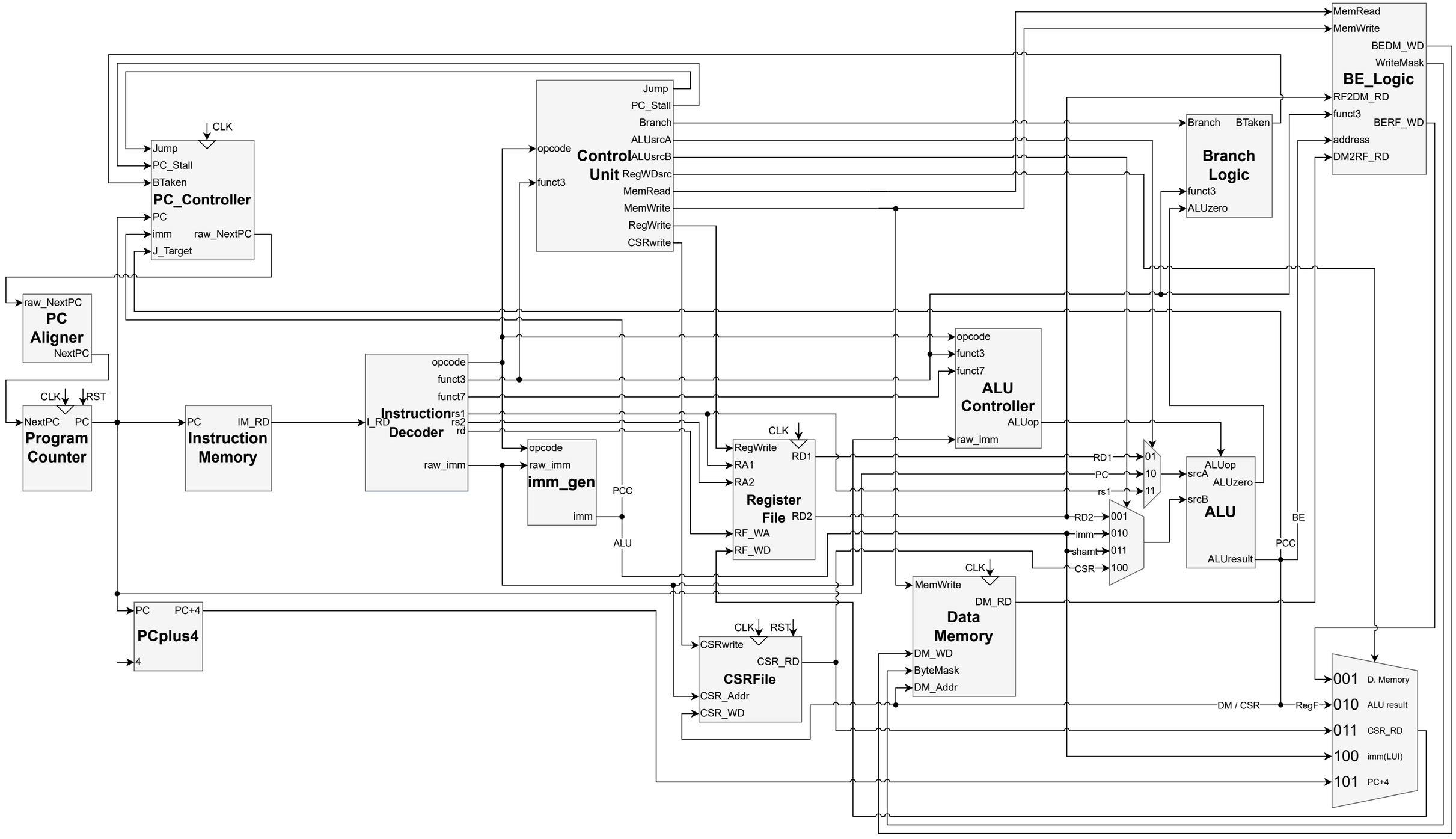

KHWL_RV32I43F.R3v2

One of Final version of milestone; RV32s project.
R3 : Data Memory is Async read. ReadDone, MemRead removed(DM). Synchronous RW Memory will be back to 5SP.
R2 : Read Done, PC_Stall signal for *Data Memory's Read operation issue*. PCC's Misalign handling delegated to PC_Aligner. Misaligned memory write operates as HINT.
Supports 43 Instructions by adding CSR Module.
(37F Architecture's 37 Instructions + Zicsr 6 Instructions = 43)

v2 for ALUsrcB MUX correction
21:56 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.27(木)