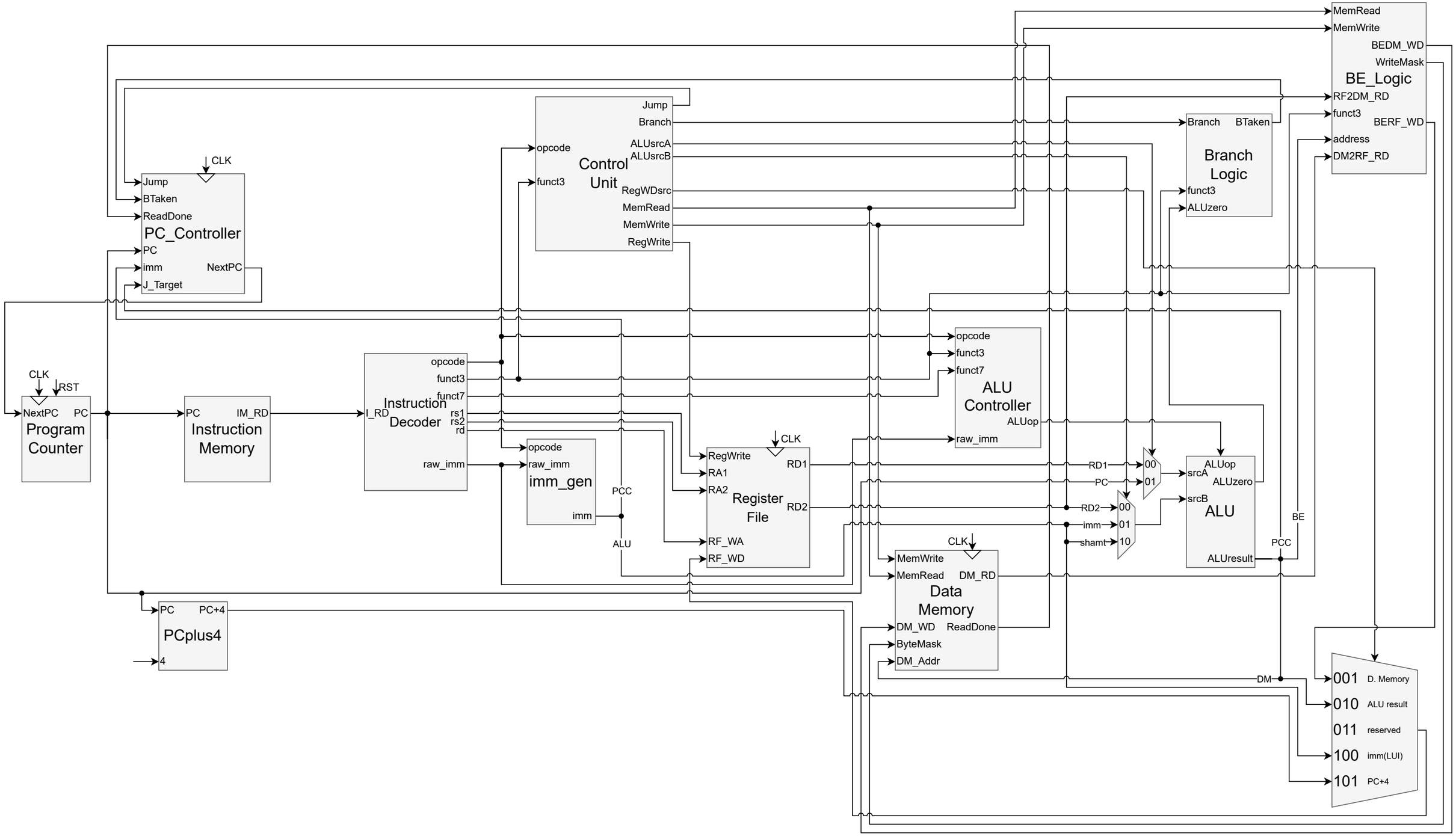

KHWL_RV32I37F.R2v2

One of Final version of milestone; RV32s project.
R2v2; ReadDone for Data Memory's proper read operation.
R2 revised ALUsrcB by adding shamt; (32-bit ext,imm) [4:0] for R&I Type Shift calculations.
Supports 37 Instructions with basic modules.
Misaligned Address access is internally handled in PCC by making lower 2 bits 0. (2'b0)
Reg_WD_MUX's 011 is reserved for CSR Module

19:19 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.02(日)