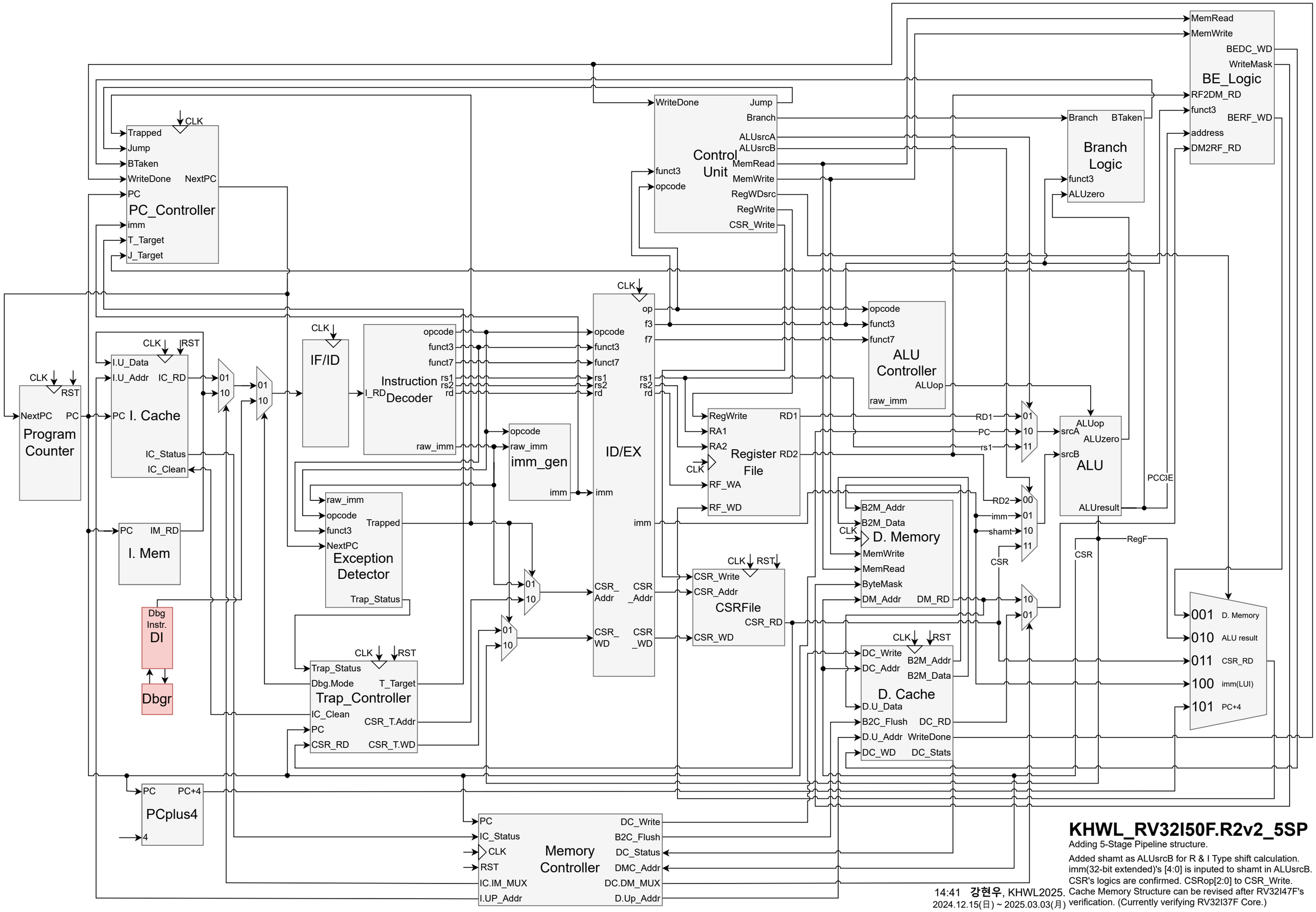

KHWL_RV32I50F.R2v2_5SP

Adding 5-Stage Pipeline structure.

Added shamt as ALUsrcB for R & I Type shift calculation.
imm(32-bit extended)'s [4:0] is inputed to shamt in ALUsrcB.
CSR's logics are confirmed. CSRop[2:0] to CSR_Write.
Cache Memory Structure can be revised after RV32I47F's verification. (Currently verifying RV32I37F Core.)

14:41 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.03(月)