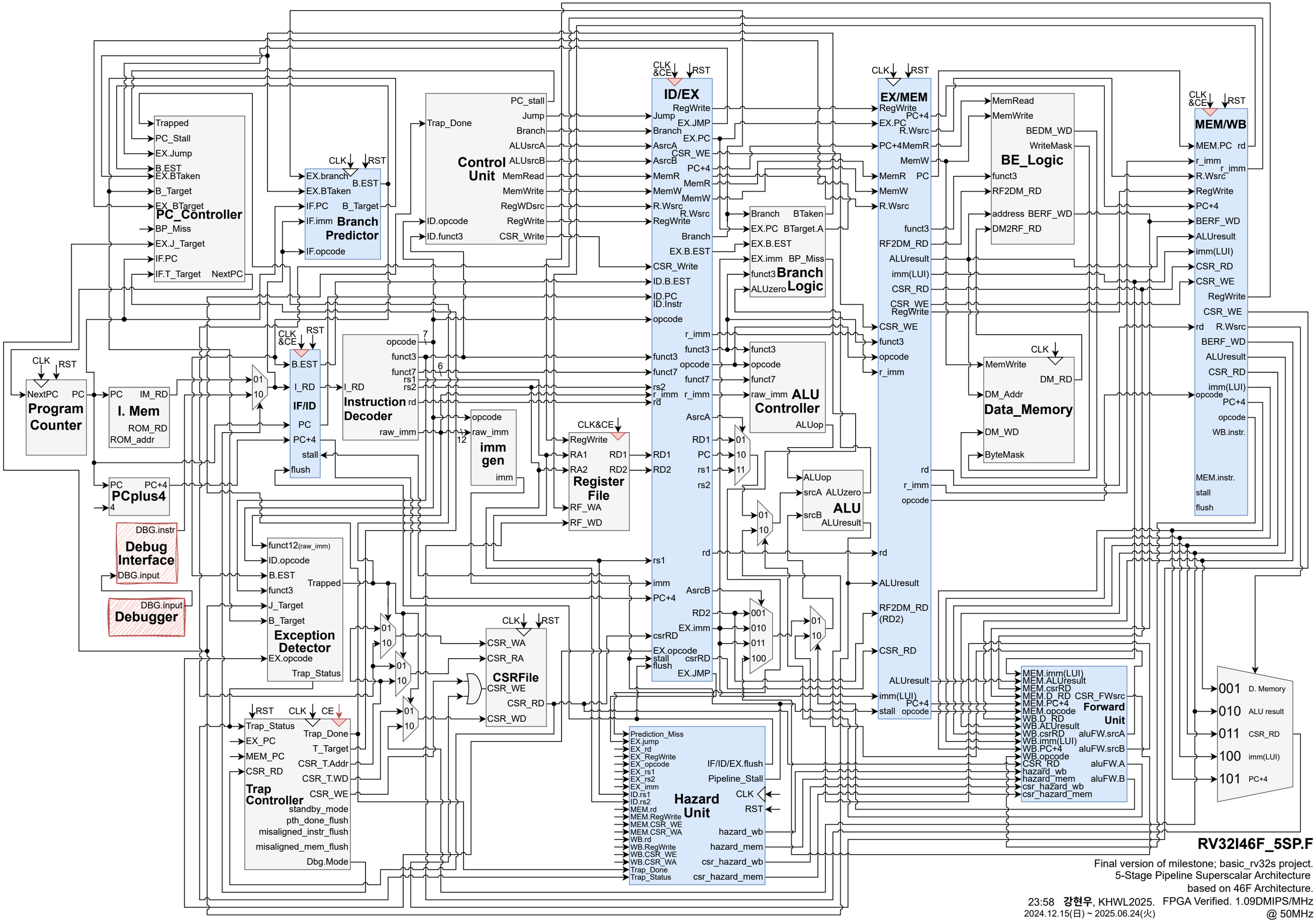

RV32I46F_5SP.F

Final version of milestone; basic_rv32s project.
5-Stage Pipeline Superscalar Architecture
based on 46F Architecture.

23:58 **강현우**, KHWL2025. FPGA Verified. 1.09DMIPS/MHz
2024.12.15(日) ~ 2025.06.24(火) @ 50MHz