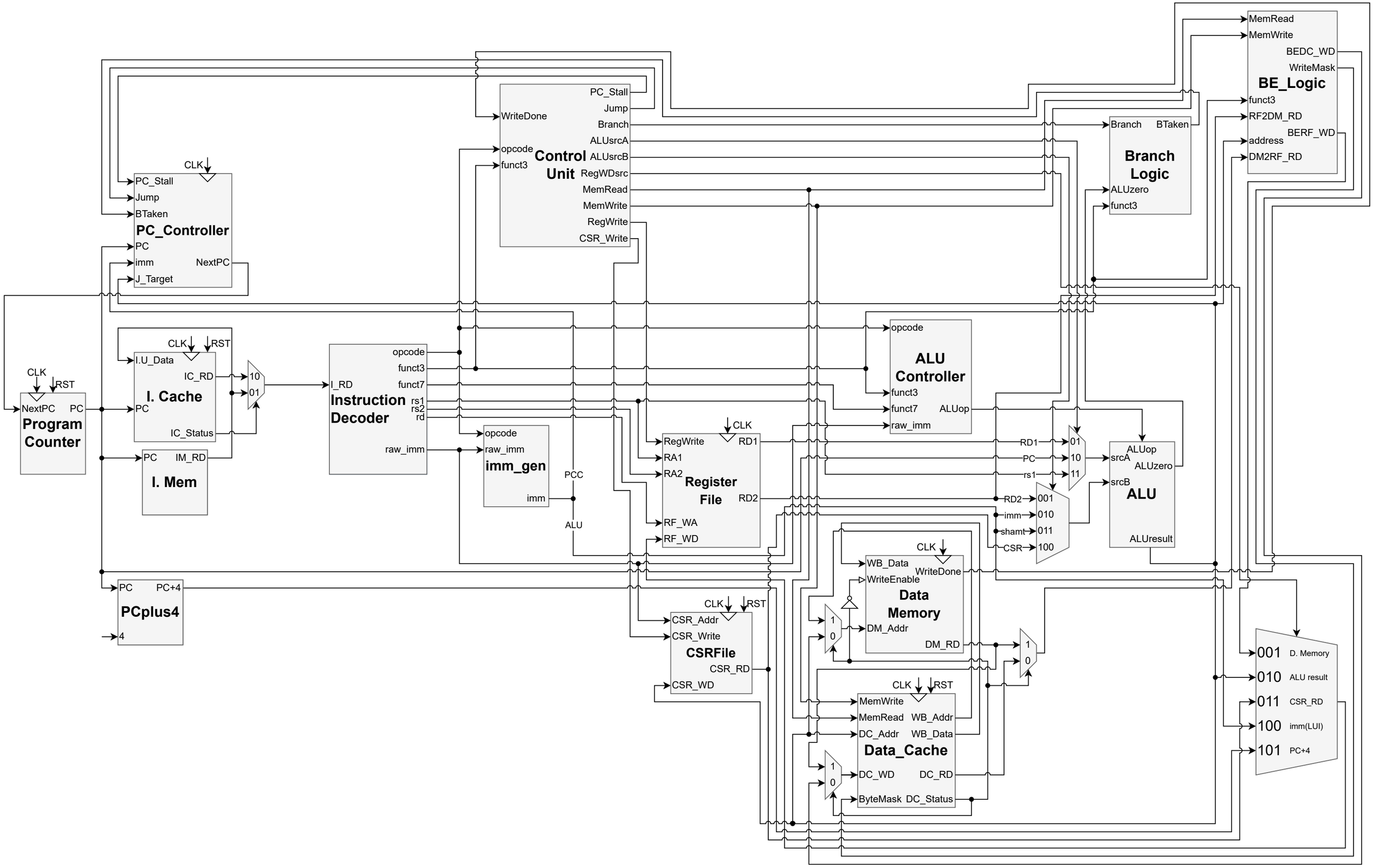

KHWL_RV32I43F_C.R1

One of Final version of milestone; RV32s project.
Memory Controller removed. DC_Status 0 for miss, 1 for hit.
Cache structure implemented based on 43F Architecture.
Supports 43 Instructions with Cache-Memory Structure
Cache is WriteBack, 2 way set-associative, STAA.

14:58 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.22(土)