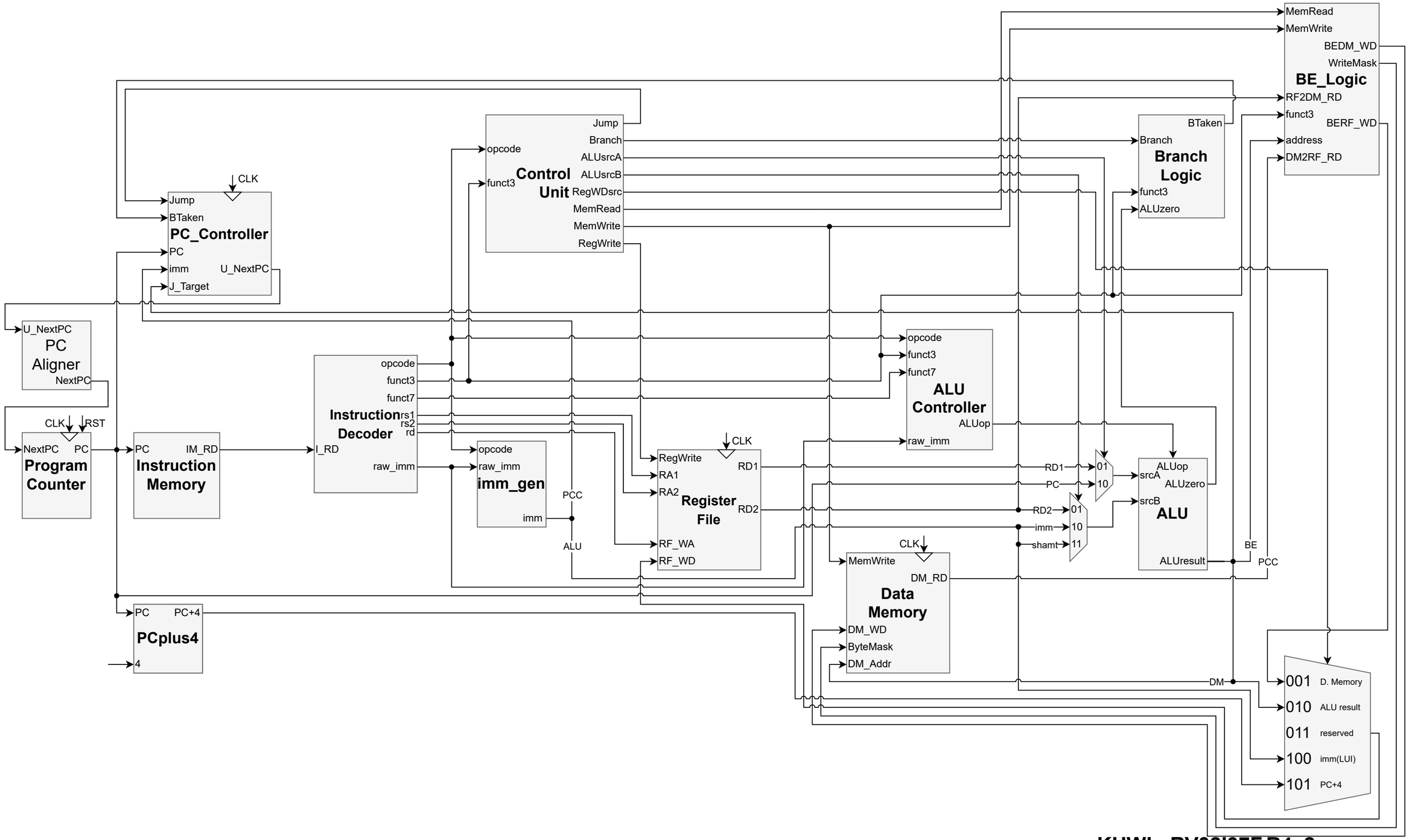

KHWL_RV32I37F.R4v2

Final version of first milestone in RV32s project.
R4v2 **:** PC_Stall signal removed since ReadDone signal is removed.
R4 : Data Memory is Async read. ReadDone, MemRead removed(DM).
Synchronous RW Memory will be back to 5SP.
R3 : Read Done, PC_Stall signal for *Data Memory's Read operation issue.*
PCC's Misalign handling delegated to PC_Aligner.
Misaligned memory write operates as HINT.
R2v2; ReadDone for Data Memory's proper read operation.
R2; ALUsrcB by adding shamt; (32-bit ext,imm) [4:0] for
R&I Type Shift calculations.
Reg_WD_MUX's 011 is reserved for CSR Module.
Supports 37 Instructions with basic modules.

11:02 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.05.03(土)