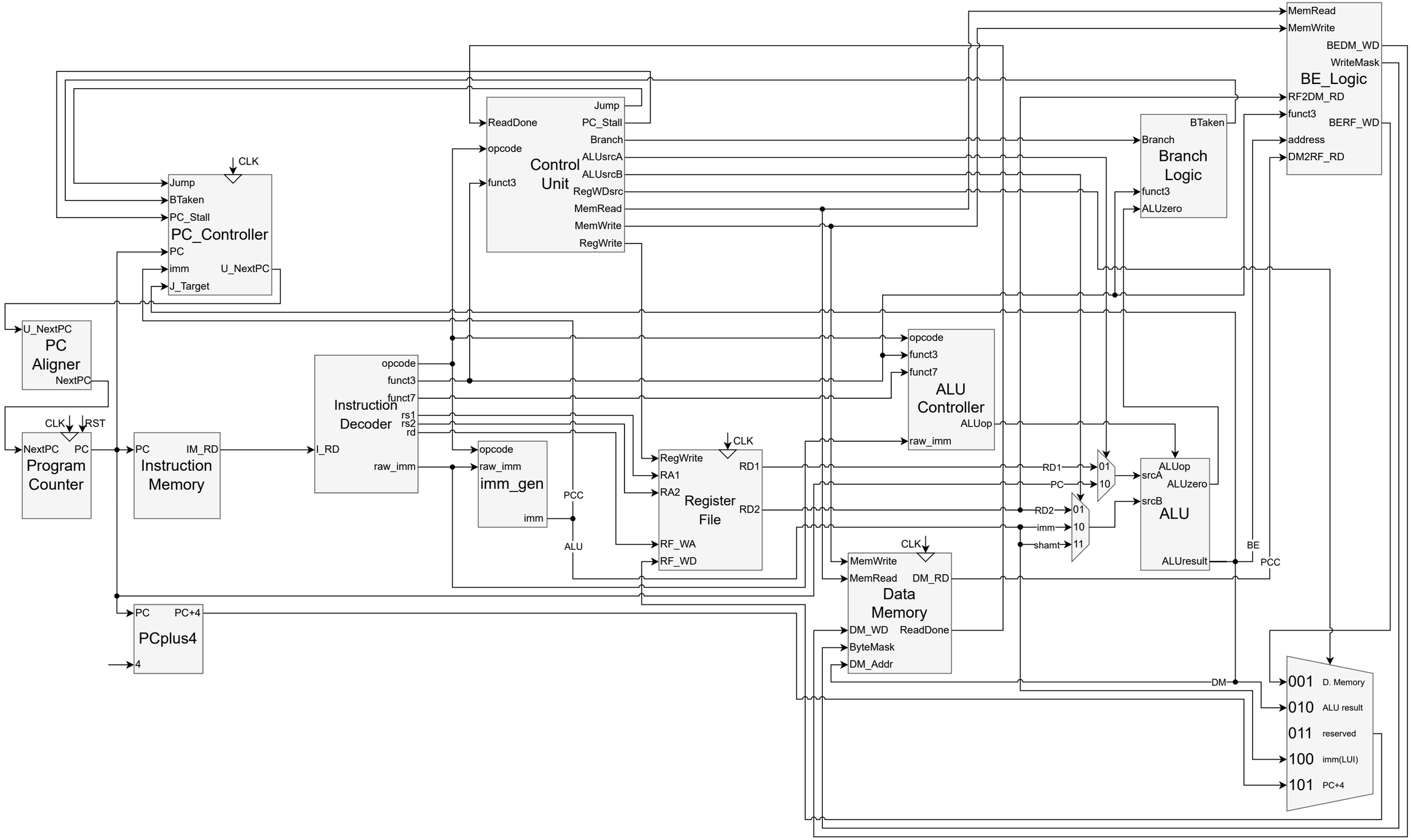

KHWL_RV32I37F.R3

Final version of first milestone in RV32s project.
R3 : Read Done, PC_Stall signal for *Data Memory's Read operation issue*. PCC's Misalign handling delegated to PC_Aligner. Misaligned memory write operates as HINT.
R2v2; ReadDone for Data Memory's proper read operation.
R2; ALUsrcB by adding shamt; (32-bit ext,imm) [4:0] for R&I Type Shift calculations.
Supports 37 Instructions with basic modules.
Misaligned Address access is handled by PC_Aligner by making lower 2 bits 0. (2'b0)
Reg_WD_MUX's 011 is reserved for CSR Module

22:36 **강현우**, KHWL2025.
2024.12.15(日) ~ 2025.03.03(月)