INSTRUCTIONS TO FOLLOW FOR ROCKET CHIP SYNTHESIS AND SUBSEQUENT P&R

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FILES DIRECTORY STRUCTURE TO FOLLOW:

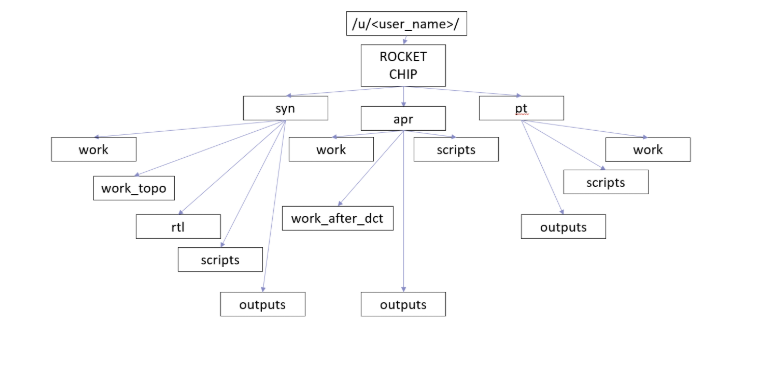


Figure 1: Depicts the file directory structure to maintain for successfully executing synthesis and physical design flow on the Rocket- Chip design.

For “syn”: This is the folder under which all the content of DC and DC -Topographical happens.

1. Put the RTL file (ROCKET\_CORE\_AND\_UNCORE.sv) in the rtl folder, and rest of the (.tcl) files namely (DC.tcl, DCT.tcl, exp\_sdc\_syn.sdc) in scripts folder under syn.
2. For the DC initial synthesis run make sure you have the latest DC version available and run “dc\_shell” from work area of syn.
3. Make sure the output gets a netlist (.vg) file generated in the outputs folder of syn.
4. Make sure to run DC -Topographical from work\_topo folder under syn folder

For “apr”: This is the folder under which all the content of ICC floor planning, ICC placement, ICC CTS and ICC routing happens.

1. Put all the apr related (.tcl) files namely (clock\_optimization\_commands.tcl, exp\_sdc.sdc, floorplan1.tcl, floorplan1\_after\_dct.tcl, icc.tcl, place.tcl, read.tcl, read\_after\_dct.tcl, setup-new.tcl, setup-new\_after\_dct.tcl) in scripts folder under apr folder.
2. Make sure you run initial floor planning in the ICC latest version, from the work folder under apr folder.
3. Make sure all the steps beginning from placement and beyond needs to be run from work\_after\_dct folder under apr folder.
4. If successfully followed, above steps will guide you to smoothly execute all the synthesis and physical design steps on the Rocket- Chip RISC V design.

FIELS AND THEIR ORDER OF EXECUTION:

1. **Synthesis RUN**: In the work area under syn folder open DC, after which you need to source the DC.tcl file which is automatically calls exp\_sdc\_syn.sdc file inside it. After running through the (.tcl) file close the DC session and go onto the next step.
2. **Initial floor planning RUN**: In the work area under apr open ICC, where you need to source the read.tcl file first and then after it need to source the floorplan1.tcl file. After running through the (.tcl) files close the ICC session and go onto the next step.
3. **Physically aware synthesis RUN**: In the work\_topo area under syn folder open DC -Topographical, after which you need to source the DCT.tcl file which automatically calls exp\_sdc\_syn.sdc file inside it. After running through the (.tcl) file close the DC session and go onto the next step.
4. **Placement and beyond RUNs**: In the work\_after\_dct area under apr open ICC, where you need to source the icc.tcl file first and then after it need to source the clock\_optimization\_commands.tcl file. After running through the (.tcl) files in the ICC session all the steps in the physical design flow are completed.

NOTE: Prime Time related folder structure (pt) at this moment can be ignored and need not be created.