Course Introduction

Building a RISC-V CPU Core (LFD111x) has been created by the Linux Foundation and RISC-V International in partnership with the Open Source FPGA Foundation, and is designed for anyone with a technical inclination who is interested in learning more about hardware. Whether you are new to digital logic or are a seasoned veteran, students will take away new skills that can be applied immediately. No prior knowledge of digital logic design is required.

This is a crash course in digital logic design and basic CPU microarchitecture. Using the Makerchip online integrated development environment (IDE), you will implement everything from logic gates to a simple, but complete, RISC-V CPU core. You will be amazed by what you can do using freely-available online tools for open source development. You will familiarize yourself with a number of emerging technologies supporting an open-source hardware ecosystem, including RISC-V, Transaction-Level Verilog, and the online Makerchip IDE.

LFD111x is a hands-on experience with RISC-V and modern circuit design tools. You will walk away with fundamental skills for a career in logic design, and you will position yourself on the forefront by learning to use the emerging Transaction-Level Verilog language extension (even if you don’t already know Verilog).

Before you begin

We strongly recommend that you review the course syllabus before jumping into the content. It provides the most important information related to the course, including:

- course overview;
- instructors biographies and targeted audience;
- course prerequisites and length;
- course learning objectives and the outline;
- edX platform guidelines;
- discussion forums, course timing, and learning aids;
- grading, progress, and course completion;
- professional Certificate Programs, audit and verified tracks;
- The Linux Foundation's history, events, training, and certifications.

Getting help

For any **technical issues** with the edX platform (including login problems and issues with the Verified Certificate), please use the Help icon located on the upper right side of your screen.

One great way to interact with peers taking this course and resolving any content-related issues is via the Discussion Forums. These forums can be used in the following ways:

- to introduce yourselves to your peer learners;
- to discuss concepts, tools, and technologies presented in this course, or related to the topics discussed in the course material;
- to ask questions about course content;
- to share resources and ideas related to RISC-V.

We strongly encourage you not only to ask questions, but to share with your peers opinions about the course content, as well as valuable related resources. The Discussion Forums will be reviewed periodically by the Linux Foundation staff, but it is primarily a community resource, not an 'ask the instructor' service.

Note: *Before starting a thread about your issue, we strongly encourage you to do a quick search to see if your question has already been addressed. It's often the case that there will be one or two threads asking the same question that has been answered.*

To learn more tips on how to use them, read the following article: *"Getting the Most Out of the edX Discussion Forums"*[1].

[1] https://blog.edx.org/getting-most-out-edx-discussion-forums

Meet Your Instructor: Steve Hoover

As founder of Redwood EDA, Steve Hoover is fostering an open-source silicon ecosystem through numerous technologies including the WARP-V CPU core generator with support for RISC-V. His main focus is design methodology and tools enabled by Transaction-Level Verilog (TL-Verilog), available to all at makerchip.com[2]. He is also the lead developer of the 1st CLaaS open-source framework for cloud FPGAs. Steve holds a BS in electrical engineering summa cum laude from Rensselaer Polytechnic Institute and an MS in computer science from the University of Illinois. He has designed numerous components for high-performance server CPUs and network architectures for DEC, Compaq, and Intel.

[2] http://makerchip.com/