RISC-V history

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Chapter overview

This chapter explores everything there is to know about the RISC-V organization – RISC-V International. We will go over the history of RISC-V from its origins as an academic program through its current incarnation as a global non-profit organization, as well as the organizations within RISC-V – technical and non-technical.

Learning objectives

By the end of this chapter, you should be able to:

- explain how the RISC-V Instruction Set Architecture (ISA) was created;
- describe the structure of RISC-V International;
- understand how member organizations work together to develop an open source community.

RISC-V history

How it all started

RISC-V's story begins at UC Berkeley Parallel Computing Lab. To set the stage, we first discuss the importance of open source and open standards, as these directly apply to the development process and open licensing of the RISC-V ISA, plus a small history of RISC processing as well as other open (or semi-open) ISAs.

Importance of open source and open standards

Technology does not persist in isolation, unless we're talking about exceptionally simple unconnected devices like a flashlight – and even there, we rely on international standards to connect the battery to the bulb. As our technical world has become more complex and more connected, global standards ensure that society may realize the profound benefits of interoperability from the inventor to the consumer.

Standards drive innovation at a base platform level from the standard threads on a machine screw to threads connecting silicon on a microprocessor. The setting of voluntary standards in engineering [1] dates back more than a century. In the late 1980s through the 1990s, Tim Berners-Lee[1] led a revolution to standardize the protocols we use on the internet (URL, HTML, HTTP, W3C), easily the biggest advance of technology utility in modern history. There are numerous examples that underpin the technology we rely on every day.

Advances in software and hardware standardization through global collaboration and consensus as well as open source development and delivery of software and hardware design has accelerated technical progress at an unprecedented global scale. The release of RISC-V to the open community, both for standardization and for ongoing improvement through open collaboration, is at the core of RISC-V International. Without collaboration and open access to the RISC-V ISA and open extensions, the community risks fragmentation, forking, and the establishment of multiple standards. Such multiplicity diminishes the strategic value and longevity of the architecture as technology providers rely on global standards to advance partnerships and supply chains as well as participate in global markets for their products and services.

As an Instruction Set Architecture, RISC-V itself is not "open source" in the same way that software is open, as an ISA is not made of source code. It is, however, an open specification, and it is released under

[1] https://en.wikipedia.org/wiki/Tim_Berners-Lee

a Creative Commons license. Other artifacts within RISC-V, such as software and compliance tests, use appropriate licenses (e.g. BSD and MIT) that retain the permissive original intent for RISC-V to be available to everyone.

History of RISC and open ISA

Reduced Instruction Set Computers[2] – RISC – have a long and varied history that begins at the University of California at Berkeley (UCB). In many ways, the history of RISC is bound up with the history of MIPS processors, which began at nearly the same time at Stanford in the 1980s. Both processor architectures have had great commercial success in different ways, although RISC architectures are arguably more likely to be recognized through some very popular designs, including Sun Microsystems' SPARC line, DEC's Alpha line, Intel's i860 and i960 processors, and the ubiquitous ARM processors that inhabit billions of devices today from many silicon manufacturers. RISC-V is the latest iteration of this instruction set architecture.

Many RISC, MIPS, and other designs have been "open" to varying degrees. In 2005, Sun Microsystems opened the SPARC architecture, creating the OpenSPARC project under the GNU Public License (GPL). The OpenRISC project provides 32- and 64-bit cores through the OpenCores community under the Lesser GNU Public License (LGPL), which is somewhat less restrictive than the GPL. The MIPS architecture, owned by Wave Computing, was provided under an "open use" license in a pilot program that closed down in 2019. Even ARM, which previously showed its architecture only to paying licensees, has now partly opened its architecture to changes by its partners. All of these efforts work to balance the needs and aspirations of partners and stakeholders with the realities of the marketplace, international laws around intellectual property, and the historic momentum in the industry that keeps leading inexorably toward open source, open specifications, and open standards.

The takeaway is that opening up an Instruction Set Architecture is both a highly valuable effort and a very difficult task – it requires collaboration among many stakeholders, protection from patent trolls and other lawsuits, and a clear path toward ownership for anyone basing their livelihood on the outcome. RISC-V is succeeding wildly because of its dedication to a fully open architecture, the protection provided and agreed to by all members in its membership agreement and internal regulations, and its full and unceasing commitment to community.

[2] https://ru.wikipedia.org/wiki/RISC

RISC-V origins: UC Berkeley architecture research

Prof. Krste Asanović and graduate students Yunsup Lee and Andrew Waterman started the RISC-V instruction set in May 2010 as part of the Parallel Computing Laboratory[3] (Par Lab) (Par Lab) at UC Berkeley, of which Prof. David Patterson was Director. The Par Lab was a five-year project to advance parallel computing funded by Intel and Microsoft[4] for $10M over 5 years, from 2008 to 2013 1. It also received funding from several other companies and the State of California. The Chisel hardware construction language that was used to design many RISC-V processors was also developed in the Par Lab. You can learn more about the Par Lab in "The Berkeley Par Lab: Progress in the Parallel Computing Landscape" [2], book by Patterson, Gannon and Wrinn.

While the project overall did not have federal funding, Yunsup Lee and Andrew Waterman received some funding from the DARPA POEM photonics project, which funded some of the processor implementation development (but not the RISC-V ISA). The funds were 6.1 basic research[5] via MIT as a prime contract with the International Computer Science Institute [3] as the subcontract.

All the projects in the Par Lab were open source using the Berkeley Software Distribution (BSD) license, including RISC-V and Chisel. The following report of the Par Lab is the first publication that describes the RISC-V instruction set: Waterman, A., Lee, Y., Patterson, D. A., and Asanović, K. (2011). The RISC-V Instruction Set Manual, Volume I: Base User-Level ISA (EECS-2011-62) [4].

For RISC-V, the UC Berkeley ParLab industrial sponsors provided the initial funding that was used to develop RISC-V. They didn't explicitly ask for RISC-V itself – their interest was in parallel processing systems.

Beyond that first publication, major RISC-V milestones include the first tapeout of a RISC-V chip in 28nm FDSOI (donated by ST Microelectronics [5] based in Switzerland) in 2011, publication of a [paper on the benefits of open instruction [6] sets in 2014, the first RISC-V Workshop [7], held in January 2015, and the RISC-V Foundation [8] launch later that year with 36 Founding Members [9].

The ISA specification itself, i.e., the encoding of the instruction set, was released with a permissive license (similar to the language of the BSD license) when the ISA tech reports were published, though the actual tech report text (an expression of the specification) was later put under a Creative Commons license to allow it to be improved by external contributors, including the RISC-V Foundation.

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[3] https://parlab.eecs.berkeley.edu/

[4] https://parlab.eecs.berkeley.edu/sponsors

[5] https://www.rand.org/content/dam/rand/pubs/monograph_reports/MR1194/MR1194.appb.pdf

No patents were filed related to RISC-V in any of these projects, as the RISC-V ISA itself does not represent any new technology. The RISC-V ISA is based on computer architecture ideas that date back at least 40 years [10]. RISC processor implementations—including some based on other open ISA standards—are widely available from various vendors worldwide.

The worldwide interest in RISC-V is not because it is a great new chip technology. The interest is because it is a common free and open standard to which software can be ported, and which allows anyone to freely develop their own hardware to run the software. RISC-V International does not manage or make available any open-source RISC-V implementations, only the standard specifications. RISC-V software is managed by the respective open source software projects.

Also see the original history article titled "RISC-V Genealogy" [11] by Chen and Patterson.

DARPA influence

After the invention of RISC-V, many projects used it, including research programs funded by the Defense Advanced Research Projects Agency [12] (DARPA), in many places and many companies. Open source standards provide great benefits to U.S. taxpayers in reducing the cost of advanced military system development, and also increases security by allowing the government to build their own trusted implementations at low cost. Note that several decades ago, the United States Air Force developed the open standard MIL-STD-1750 16-bit processor ISA[6] for military applications for the same reasons.

The UC Berkeley ASPIRE Lab [13] succeeded the Par Lab, and was led by Krste Asanović. It lasted from 2013 to 2018 and led to the building of several RISC-V compatible microprocessors. It had funding from DARPA as well as from many companies. The DARPA funding was basic research funding (6.1 category)[7].

Basic research funding to universities is largely for unrestricted research with permission to publicly disseminate the results. This contract is the standard model for U.S. federal grants to universities, and allows for results from the funded work to be published in the open literature and made accessible to the public at large, worldwide. The government retains rights to use any technology developed in the research, but, unless explicitly stated, does not restrict the technology.

A related DARPA photonics program predates RISC-V and funded research at MIT in 2006. The research supported the development of integrated silicon photonics. Later stages of funding at MIT and

[6] https://en.wikipedia.org/wiki/MIL-STD-1750A

[7] https://www.rand.org/content/dam/rand/pubs/monograph_reports/MR1194/MR1194.appb.pdf

Berkeley were used to build prototype chips, which included RISC-V cores as infrastructure to demonstrate the photonic links.

The ASPIRE Lab was funded by the DARPA Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) program. The goal of the program was to develop revolutionary approaches as well as the technologies and techniques to provide the power efficiency required to enable embedded computing systems. Researchers used RISC-V based systems to demonstrate the ideas in that program.

In all of these funded projects, the RISC-V ISA specification and RISC-V open-source cores were not a contract deliverable. RISC-V was just the infrastructure separately developed to support the funded research.

While DARPA did not fund the original RISC-V ISA definition, DARPA funding played a significant role in its later development. The linked articles on the SSITH Voting Machine [14] and the US Department of Defense (DoD) presentation by Linton Salmon [15] detail some of the areas where DARPA research continues to support RISC-V.

DARPA funds a large set of programs around open-source hardware technology. RISC-V International has never had DARPA funding, nor pursued or received funding from any government.

Side quest: The RISC-V name

How did RISC-V get its name? The RISC portion is fairly obvious, but why is it number 5, and why is this represented with a Roman numeral? The answer lies in a footnote in the introduction of the ISA spec itself:

The name RISC-V was chosen to represent the fifth major RISC ISA design from UC Berkeley (RISC-I [15], RISC-II [8], SOAR [21], and SPUR [11] were the first four). We also pun on the use of the Roman numeral “V” to signify “variations” and “vectors”, as support for a range of architecture research, including various data-parallel accelerators, is an explicit goal of the ISA design.

RISC-V International

What is RISC-V International?

The RISC-V Foundation [16] was founded in 2015 to build an open, collaborative community of software and hardware innovators based on the RISC-V ISA. The Foundation, a non-profit corporation controlled by its members, directed the development to drive the initial adoption of the RISC-V ISA.

Across 2018-2019, the RISC-V community reflected on the geo-political landscape and heard concerns from around the world that investment in RISC-V must come with IP access continuity to ensure a long-term strategic investment. We first mentioned our intentions to move at the December 2018 summit. Incorporation in Switzerland has the effect of calming concerns of political disruption to the open collaboration model. As a non-profit, membership-based organization, RISC-V International does not maintain any commercial interest in products or services. There have not been any export restrictions on RISC-V in the US and we have complied with all US laws. The move does not circumvent any existing restrictions, but rather alleviates uncertainty going forward.

In March 2020, the RISC-V International Association was incorporated in Switzerland. Along with this, we shifted to a new, more inclusive membership structure. Members of RISC-V International have access to and participate in the development of the RISC-V ISA specification and extensions as well as related hardware and software. RISC-V has a Board of Directors composed of member representatives as well as a Technical Committee of work group leaders.

RISC-V International's decision to incorporate in Switzerland is not based on any one country, company, government, or event. This move is reflective of community concern and managing strategic risk for our community investing in RISC-V for the next 50+ years.

The IP contributed and produced by RISC-V International is held under industry and global standard licenses that are already open to leverage by any company regardless of jurisdiction. This licensing is a common open source approach to foster collaboration that is not tied to any geographic regulation. Open Source IP has not been subject to export control.

We encourage organizations, individuals, and enthusiasts to join our ecosystem and together enable a new era of processor innovation through open standard and open source collaboration.

RISC-V International membership

RISC-V is a non-profit membership-based organization that is driven by its members through representative governance on a Board of Directors, a Technical Steering Committee, and many other working committees.

Membership is offered at various levels, and members receive a wealth of benefits. Most importantly, the membership process provides intellectual property protection for all members as well as provenance and IP security for the RISC-V ISA itself, which is RISC-V International's top priority. All members are able to participate fully in the technical development process as well as in project administration through various working groups and committees. Members are also able to participate in a number of annual events and workshops and to stay on the leading edge of RISC-V development. All benefits are outlined on the membership page [17].

One common question is why RISC-V insists on membership rather than opening contribution and participation to the general public in the manner of the Linux kernel and many other open source software projects. The primary reason for this is the IP protection just mentioned. The RISC-V membership agreement and the Articles of Association provide solid protection, but their scope is limited to members who actually sign the agreement.

While active participation is limited to members for this reason, RISC-V does make the entire technical process transparent (in read-only fashion) to non-members, and provides a wealth of learning opportunities as well as a set of public discussion lists where experienced RISC-V developers often contribute.

Membership in RISC-V is free for individual people, academic institutions, and non-profit organizations. For-profit companies have three membership levels available with annual dues, which support the ongoing collective support, facilitation, and advocacy of RISC-V as well as the following programs to foster the technical development, academic inclusion, market adoption, and industry visibility of our RISC-V community and members.

Members become **Premier Members** in order to have a seat at the table for the governance of RISC-V itself. Premier TSC members get a seat on the Technical Steering Committee, which governs the technical process, while full Premier level members earn a seat on the Board of Directors as well as the TSC.

Strategic Members make up the largest proportion of RISC-V membership, and include companies from dozens of industries as well as a number of academic institutions who want to support RISC-V

financially. Strategic members pay dues according to their organizational size, with four tiers available. Strategic members elect three representatives to the Board of Directors annually.

Community Organizations include academic and non-profit organizations, many of whom also participate in the Academia & Training Special Interest Group to exchange ideas and educational materials. Community Organizations pay no dues, although many of them choose to sponsor RISC-V events. Community Organizations elect one representative annually to the Board of Directors for their group.

All Organizational members – Premier, Strategic, and Community Organization – have access to the RISC-V Trademark, which includes the RISC-V name and logo.

Community Individuals are some of the most active members of the RISC-V community. There are active Individuals in all technical and non-technical working groups and special interest groups. Community Individuals pay no dues, and they elect one representative annually to the Board of Directors for their group. Individuals do not have access to the RISC-V trademark, but many of them are able to convince their employers or other organizations they are affiliated with to join RISC-V as an organization.

RISC-V International Governance

RISC-V International is governed by its Board of Directors. The Board is composed of Directors elected to represent all classes of membership to ensure we offer a strategic voice at all levels. In addition, the Technical Steering Committee (TSC) provides leadership to our technical initiatives in setting long term strategy, forming tactical committees and work groups, and approving technical deliverables for ratification or release.

RISC-V International also supports and drives technical working groups – committees, task groups, and special interest groups – to pursue specific industry, geographic, and strategic interest through a variety of constructs. Working groups are chaired by community members who drive developers toward consensus. Our aim is to guide and facilitate the broadest and most effective collaboration for the benefit of our member community.

RISC-V community working model

Community development is core to RISC-V International – there is no single company behind the scenes, and without the active community of architects and developers, there would be no RISC-V.

You will learn more about the practicalities of community-based specification development in Chapter 3 of this series. What we'd like to describe here is what the community looks like and how each part of the community contributes to making RISC-V the holistic, heterogeneous, vibrant community that it is.

Specification development teams – whom we call the "tech" community – are composed of RISC-V International members, including both individuals and organizations. Although each member participates at their own level, we welcome everyone's voice in the development process. Working groups and committees are chaired by member organizations, but it is possible for a sufficiently enthusiastic and skilled individual member to help lead a working group if they earn support from the community and the TSC.

All members are welcome to participate and contribute in technical groups through mailing lists, meetings and workshops, webinars and conferences, and in many other ways. The technical working groups are publicly visible so that non-members can also follow discussions and progress.

In addition, there are three public forums where anyone may participate:

- the RISC-V public mailing lists, particularly ISA-Dev [18] and SW-Dev [19], which date back to the earliest days of RISC-V;
- the Exchange forums [20], which provide a focused discussion point for items that appear on the RISC-V Exchange;
- the RISC-V Slack channel [21] for live chat.

RISC-V's relationship with the Linux Foundation

In November 2018, the RISC-V Foundation announced a joint collaboration with the Linux Foundation. As part of this collaboration, the Linux Foundation provides operational, technical, and strategic support for RISC-V International, including member management, accounting, training programs, infrastructure tools, community outreach, marketing, legal, and other open source services and expertise.

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