Ministry of Electronics & Information Technology, Government of India

IITM PRAVARTAK
CATALYSING INNOVATION

Digital India RISC-V Symposium - A Tech Showcase For India's Future Electronics

Sharat D. Kaul
6 August 2023

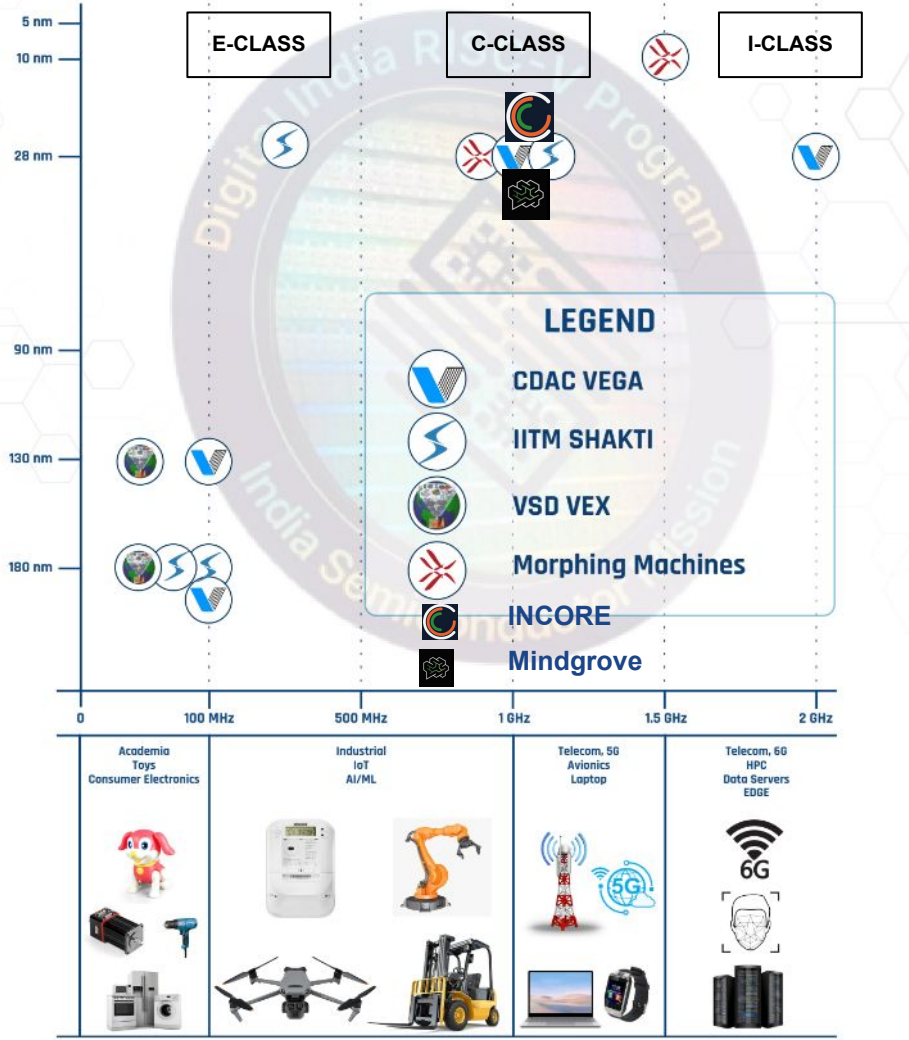
DIR-V: 27th April 2022

India launches Digital India RISC-V (DIR-V) program for next generation Microprocessors to achieve commercial silicon & Design wins by December 2023

- DIR-V Will Catalyze India's Semiconductor Startups, it is a part of PM Narendra Modi ji's Mission of making India a Semiconductor Nation: Rajeev Chandrasekhar
- DIR-V will see partnerships between Startups, Academia & Global Majors, and prove to be a RISC-V Talent Hub for World
- India through MeitY set to take Premiere Board Membership of RISC-V International to collaborate, contribute and advocate India's expertise with the RISC-V leaders of the world

Agenda

- DIR-V Semiconductor Landscape
- DIR-V → Mission Mode 2030
  - Core Teams
  - Innovation → Startup → ChipIN
  - Acceleration → Exits
- RISC-V International
- Observations, Recommendations
- Q&A



DIR-V Semiconductor Landscape

- Bodhi Computing, Bangalore
  - Tenstorrent RISC-V
  - Chiplets, 4 nm
  - HPC, Data Server
- Calligo Tech, Bangalore
  - POSIT-based Coprocessor
  - BlueSpec Flute 8-core RISC-V
  - FPGA, DDR, DMA, Ethernet
- Aheessa Digital, Chennai
  - CDAC VEGA Vihaan RISC-V
  - 28 nm, 1.5 GHz+ (Planned)
- Maxvy, Bangalore
  - SiFive RISC-V
  - 320 MHz
  - Autonomous GPS Drones
- Signoff Semiconductor, Bangalore
  - PICORV32 RISC-V
  - AHB3 Lite
  - 100 MHz, FPGA

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DIR-V → Mission Mode 2030

- India to develop Products based on its own Proprietary RISC-V Architectures
- India to emerge as the leading Country driving an Open Source platform
- Define the Roadmap for both **IPs and Products**
  - Lead Global Open Source Consortiums (Silicon, Software, Platforms/ IP, and Systems)
  - Collaborate with Universities
  - Drive Innovation
  - Nurture Startups
  - Sponsor Technical and Business Events
  - Mentor and Train Students
  - Collaborate with Companies Worldwide
  - Deliver India based competitive Products and Technologies
- '*Leap-frog*' and '*Stay Ahead*' of China (CRVA and CRVIC)

Arm Flexible Access Mainstream Package

Cortex Processors

Cortex-A
- Cortex-A55*
- Cortex-A53*
- Cortex-A35*
- Cortex-A34*
- Cortex-A32*
- Cortex-A7
- Cortex-A5

Cortex-R
- Cortex-R52
- Cortex-R52+
- Cortex-R8
- Cortex-R5

Cortex-M
- Cortex-M55
- Cortex-M33
- Cortex-M23
- Cortex-M7
- Cortex-M4
- Cortex-M3
- Cortex-M0+
- Cortex-M0

Mali Multimedia Processing

- Mali-G52 GPU
- Mali-G31 GPU
- Mali-C52 ISP
- Mali-C32 ISP
- Frame Buffer Compression

Ethos Machine Learning Processors

- Ethos-U65
- Ethos U55

CoreLink Interconnect

- CoreLink NIC-450
- CoreLink NIC-400
- CoreLink CCI-550
- CoreLink CCI-500
- CoreLink CCI-400
- CoreLink PCK-600
- CoreLink DPE-400
- CoreLink SIE-300
- CoreLink SIE-200
- CoreLink ADB-400
- CoreLink XHB-500 AXI5-AHB5
- CoreLink XHB-400 AXI-AHB

Corstone Reference Systems

- Corstone-1000
- Corstone-500
- Corstone-300
- Corstone-201
- Corstone-102
- Corstone-101

CoreLink System Controllers

- CoreLink GIC-600
- CoreLink GIC-500
- CoreLink GIC-400
- CoreLink TZC-400
- CoreLink L2C-310
- CoreLink MMU-600
- CoreLink MMU-500
- CoreLink DMA-350
- CoreLink DMA-330
- CoreLink DMA-230
- PL192 VIC
- BP140 Mem. Interface
- BP141 TrustZone MW
- AHB Cache

Safety Packages

- Cortex-A55, A53
- Cortex-A35, A34, A32
- Cortex-R52, R5
- Cortex-M55, M33, M23
- Cortex-M7, M4, M3, M0+

Peripheral Controllers

- PL011 UART
- PL022 SPI
- PL031 RTC

CoreSight Debug and Trace

- CoreSight SoC-600
- CoreSight SoC-600M
- CoreSight SoC-400
- CoreSight SDC-600
- CoreSight ELA-600
- CoreSight ELA-500
- CoreSight STM-500
- CoreSight STM
- CoreSight TMC

Artisan Physical IP**

Processor Implementation Kits
- Artisan PIK for Cortex-M33, TSMC 22ULL
- Artisan PIK for Cortex-M55, TSMC 22ULL
- Artisan PIK for Ethos-U55, TSMC 22ULL

Artisan Free Library Program
- Thousands of Physical IP Libraries

Tools & Models	• Access the latest tools & models in Success Kits to accelerate and improve development
Support	• Global technical support • On-demand Training

** Crypto extensions of Cortex-A55, A53, A35, A34 and A32 may require Arm's trade compliance team to obtain an export license before we can enable download. This process can take several weeks to complete so please send the request as early as possible.*

*** Additional logic IP, standard cell, embedded memory compilers and interface IP across many foundry nodes also available without a license fee.*

arm

Workgroups - Prof. Kamakoti, Chief Architect

1. Lead Global Open Source Consortiums a. Silicon b. Software c. Platforms (incl. IP) d. Systems	1. Sambit Sahu, Krishnakumar a. Sambit Sahu b. (Sharat), Lavanya c. Neel, Shashwath d. Vikas, Kunal, Narahari
2. Collaborate with Universities	2. Sharat, Kunal, Vikas, CDAC
3. Drive Innovation	3. All
4. Nurture Startups → Pravarthank, Startups	4. Sharat
5. Sponsor Technical and Business Events	5. Sambit Sahu, IIT Madras
6. Mentor and Train Students	6. Kunal, Vikas, Signoff Semi
7. Collaborate with Companies Worldwide	7. Sharat, CDAC
8. Deliver India based competitive Products and Technologies	8. All
9. India HPC and AI	9. CDACs, Sambit, Deepak
10. '*Leap-frog*' and '*Stay Ahead*' of China (CRVA and CRVIC)	10. Sambit Sahu, Sharat Kaul

Silicon - Charter

Establish RISC-V as the foundation CPU IP with India instruction set for all silicon products owned by India.

Silicon - Smart Goals

• Develop an architecture portfolio for all product types owned by India (ranging MCU, IOT, Client, Edge, Mobility, HPC, networking, AI/ML Servers) with a common baseline architecture.

• Deliver India oriented instruction set (baseline and extensions) for the architecture portfolio mentioned above • Develop a reference suite : tools/flows/methodologies, design, testbench, dft, implementation recipe, prototype for the different architectures mentioned above.

• Establish an ecosystem that can help a design/product house to efficiently take the product from concept to silicon.

• Be the innovative power house for RISC-V innovations in terms of new product types, new applications, new extensions, and new technologies.

• Ensure that India inc has the necessary skills/expertise in silicon design to be the RISC-V power house in the world.

• Be acknowledged as a leader of RISC-V agenda in consortiums and communities worldwide.

Software - Charter

Make India as the clear leader of RISC-V software stack worldwide.

Software - Smart Goals

- Deliver world-class reference SW stacks for the architectures. India instructions, and product types defined above.
- Be the leading open source SW contributor. Lead in at least 50% of the open source RISC-V SW worldwide consortiums.
- Accelerate the deployment of RISC-V products (cut down to one third of the time taken by ARM).
- Be the lead innovator in “software defined architectures” (e.g software defined vehicles, software defined AI/M etc.).
- Deliver RISC-V SW at the highest velocity and volume, and lowest cost worldwide.

Systems - Charter

Ensure all digital systems built by India are RISC-V based, delivering the most optimal power/performance/cost.

Systems - Smart Goals

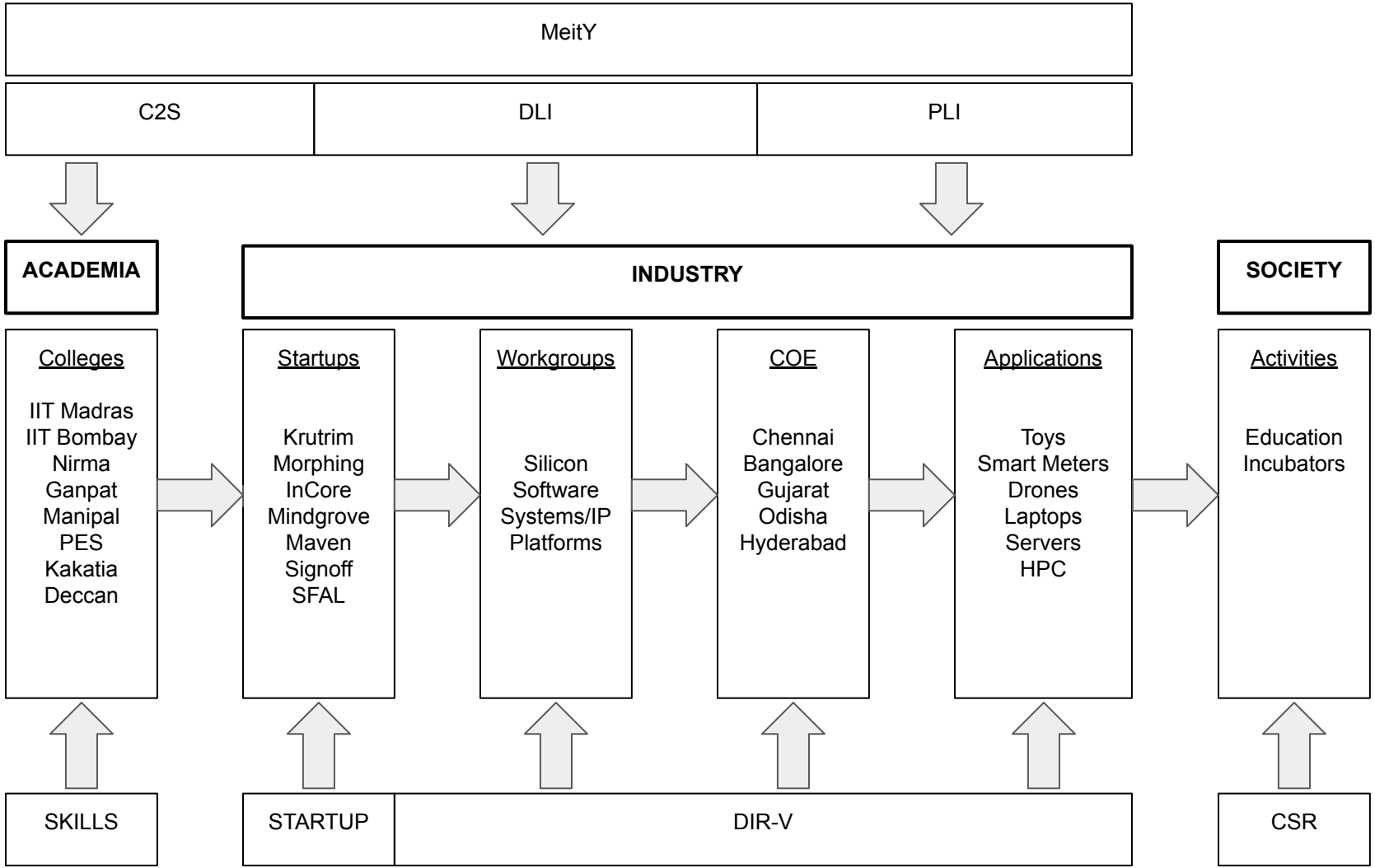
- Deliver reference systems, flows, and recipes for the products defined above.
- Deliver a framework on which new systems can be easily innovated, evaluated, and decisions made.
- Deliver a framework of tight HW-SW collaboration during the design cycle and multiple levels of prototyping.
- Define and implement an architecture for easy applications development, outstanding User Experience and Developer Experience (UX/DX).
- Establish a framework by which different stakeholders (startups, academics, Govt, application developers) of India inc can efficiently and effectively collaborate.

Platforms - Charter

Establish an India platform (with global platform as a baseline) for the architectures and product types adopted by India.

Platforms - Smart Goals

- Deliver reference platforms for the products defined above.
- Be the leading driver, contributor, and deployer of RISC-V platforms worldwide.
- Establish a platform architecture to enable different stakeholders of India inc to efficiently and effectively collaborate.
- Take aspirational goals : be the CO2 emission reduction champion, be the TCO champion.
- Strive towards being complete indigenous : entire platform, all its components, all material, end-to-end production.


MeitY
C2S
DLI
PLI
ACADEMIA
INDUSTRY
SOCIETY
Colleges
IIT Madras
IIT Bombay
Nirma
Ganpat
Manipal
PES
Kakatia
Deccan
Startups
Krutrim
Morphing
InCore
Mindgrove
Maven
Signoff
SFAL
Workgroups
Silicon
Software
Systems/IP
Platforms
COE
Chennai
Bangalore
Gujarat
Odisha
Hyderabad
Applications
Toys
Smart Meters
Drones
Laptops
Servers
HPC
Activities
Education
Incubators
SKILLS
STARTUP
DIR-V
CSR

MeitY ChipIN at C-DAC

MeitY has set up **ChipIN Centre** at C-DAC Bangalore to dedicate its services to semiconductor design community of the country.

- The facility acts as one-stop centre to provide semiconductor design tools, fab access, virtual prototyping hardware lab access to fabless chip designers from Startups and Academia.
- It is a common dedicated centralised cloud-supported design facility, not only hosting the most advanced EDA tools for the entire chip design cycle, but also provide aggregate services for fabrication of design at Indian foundries, for example, SCL foundry & overseas foundries and packaging.
- https://www.youtube.com/watch?v=gtf4CXt_8mc

What is included in Arm Flexible Access?

Tier	DesignStart	Entry	Standard
	Ideal for smaller semiconductor design teams doing no more than 1 tape out per year		Ideal for larger semiconductor development teams with multiple concurrent projects
IP portfolio	DesignStart CPU Package: Cortex-M0, Cortex-M23, Cortex-M3 and related Corstone example systems	Mainstream Package: Broad portfolio of Cortex CPUs, Mali GPUs, Corstone IP, CoreLink and CoreSight System IP	
DesignStart Physical IP (Free Library Program)	√	√	√
Support from Arm expert engineers	Forum support Paid support option available	√	√
Number of tape-outs per year	1 (Unlimited for Physical IP)	1+ * (Unlimited for Physical IP)	Unlimited
Online training	2 Seats	Unlimited on-demand training seats	
Tools and models	1 Hardware Success Kit User License (90 day)	1 Hardware Success Kit User License 3 Software Success Kit User Licenses	3 Hardware Success Kit User Licenses 9 Software Success Kit User Licenses
Membership Fee	$0	$0 for qualifying startups or $80k per annum	$212k per annum

* Entry Tier: Up to 3 tape outs where any of Cortex-M0/M0+/M23/M3/M4 is the main processor, or 1 tape out per year

Artisan Physical IP – Free Library Program

For details of the thousands of Physical IP libraries included in the Artisan Physical IP - Free Library Program see https://www.arm.com/products/silicon-ip-physical

	5 nm	7 nm	12 nm	14 nm	22 nm	28 nm	40 nm	45 nm	55 nm	65 nm	80 nm	90 nm	110 nm	130 nm	150 nm	152 nm	160 nm	180 nm	250 nm
TSMC		●	●		●	●	●		●	●	●	●	●	●	●	●	●	●	●
Samsung	●	●		●		●		●		●									
Global Foundries/ IBM			●	●		●	●	●	●	●		●	●	●				●	●
UMC					●	●	●		●	●	●	●		●	●			●	●
SMIC						●	●			●		●	●	●	●			●	
XMC									●										
SK hynix												●							
Silterra													●	●	●				
HHGrace													●	●				●	
DB HiTek													●	●				●	
Vanguard													●					●	●
MagnaChip														●				●	
CSMC														●					
TowerJazz														●					
HeJian																	●	●	
1st Silicon																		●	●
HHNEC																		●	

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SemiconIndia FutureDESIGN

Stimulate the next-gen Semiconductor Designers, Promote the culture of Co-development and joint ownership of IPs with active industry participation and Indigenously Develop Semiconductor Chips for Automobile, Mobility, Communication & Computing.

- Innovate semiconductor designs for automobile, mobility, and compute.
- Stimulate the next-gen semiconductor design startups.
- Catalyze development of Indian IP cores in semiconductors.
- Catalyze co-development and joint ownership of IPs with active industry participation.
- Availability of incentives for next wave of design startups.

RISC-V Arduino Kits : Impact on Academia

If introduced in the academic sphere, can **catalyze numerous transformative changes**.

1. Enhanced Practical exposure to RISC-V and Embedded Systems
2. Comprehensive Skill development in RISC-V Architecture
3. Stimulate Research and Development Activities
4. Facilitating Multidisciplinary Projects
5. Augmenting Industry-Relevant Education

Enriching Academic Courses

1. Practical Hardware Design
2. Embedded Systems Course
3. IoT/AI Applications
4. Operating Systems Course
5. Capstone Projects

Workshops based on these dev-kits

1. Introduction to RISC-V and Arduino Development Kit
2. Hardware Designing with Arduino Dev-Kits
3. Embedded Systems Workshop
4. Concept to Silicon to Application - VSD
5. Capstone Projects

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RISC-V® International India Members

Premier (1)	Strategic (6)	Community (11)

सत्यमेव जयते
Ministry of Electronics & Information Technology
Government of India

AISemiCon
Applied Intelligence Semiconductors

MAVEN SILICON
Centre of Excellence in VLSI

FERMIONIC

incore

SignOff semiconductors

Valtrix SYSTEMS

सी डैक CDAC

DECCAN COLLEGE OF ENGINEERING AND TECHNOLOGY

GANPAT UNIVERSITY
॥ विद्यया समाजोत्कर्षः ॥

INDIAN INSTITUTE OF TECHNOLOGY MADRAS
FOUNDING

MANIPAL ACADEMY of HIGHER EDUCATION
(Institution of Eminence Deemed to be University)

NIRMA UNIVERSITY
INSTITUTE OF TECHNOLOGY
NAAC ACCREDITED 'A' GRADE

PES UNIVERSITY

SFAL

కాకతీయ విశ్వవిద్యాలయం
KAKATIYA UNIVERSITY
Warangal - 506009, Telangana, India.

- 13 out of the 25 RISC-V International Premier members are from China

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

AUG
6

All day

Digital India RISC-V Symposium - A Tech Showcase For India's Future Electronics


RISC-V
SUMMIT
SAVE THE DATE
NOVEMBER 7 – 8, 2023
NOVEMBER 6: MEMBER DAY
SANTA CLARA, CALIFORNIA
#RISCVEVERYWHERE
#RISCVSUMMIT

Mar
18

All day

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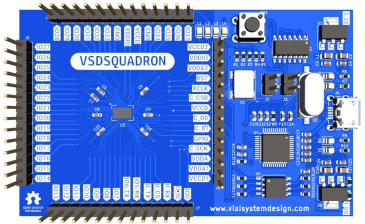
RISC-V India Ecosystem Development

- Objectives
  - Atmanirbhar → Make in India - For the World
  - Processor Replacement and Miniturization
  - Develop the Global Talent Pool - 100,000 by 2030
  - Accessibility (cost and scale) for Academia
- Strategies
  - RISC-V development kits for Academia - 100,000
  - Consumer, Auto, Defence, Space Grade Certifications
  - RISC-V COEs (with State Governments)
- Execution
  - Industry and Academia Tape Outs with a segmented and phased approach
  - International RISC V conference delegations (R&D between IITs and US Colleges)
  - RISC-V Federation of India industry body (Government, Industry, Academia)



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Thank you! Questions?

Sharat D. Kaul
sharatkaul1972@gmail.com
+91 98 4598 0616