NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/02/05

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 3

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda TBD with new time slot) issue

Issue #349/pull #364 – discuss moving CLIC memory mapped registers to indirect CSRs

Issues #158,171,226/pull #369 – CLICINTCTLBITS parameter

Issue #314 – shv==0 requirement for xnxti. more discussion needed. up

Meeting minutes:

Merged 368 to close 367 – clicintip/ie clarification

Is there a way to write CLICINTCTLBITS pull so certain interrupt levels could be hardcoded?

Is level/edge programmability required or can it be hardcoded and WARL?

DTS entry – check plic spec to see example.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

Need spec updates:

Need more discussion:

#158,171,226/pull#369 - CLICCTRLBITS

#314 – shv==0 requirement for xnxti

#349,221 – discuss moving CLIC memory mapped registers to indirect CSRs

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#242 – SPIKE model implementation of CLIC

#360 - Requested Tentative stateen bit (refer to greg email on how to interact with AR).

Issues punted for rev1, keep open for future enhancements/ecosystem development:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#102 - preemptible interrupt handler code (for section 7.2)

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#187 – QEMU CLIC implementation update

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#**329** - support for hw register save.

#348 – discuss location of inhv for future if enabling CLIC per mode. xcause still ok?