NOTE: updated zoom info for next meeting and beyond.

Date: 2023/10/10

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 8

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (10/24/23)

Issue #360 – add v1.0 label so we remember to ask for smstate bit for clic?

Issue #349/pull #364 – discuss moving CLIC memory mapped registers to indirect CSRs

Issue #314 – shv==0 requirement for xnxti. more discussion needed. New CSR?

Issue #308/pull #325/pull #344– xnxti service loop – fix of pull #343 based on discussion.

Meeting minutes:

 Sail status – vector hopefully merged by thursday. after vector do config pull evaluation. use riscv-config (yaml files). Api within sail to get value of whatever config is. if warl field. what are legal values. What's reset value. What are memory maps. Sail is strongly typed. So can do assertions about behavior of code/core. if sail can natively get these values then easier for theorem provers. so this riscv-config to C to sail flow might be intermediate. want to go riscv_config yaml to sail directly.

Issue #358/pull #363 – merged pull. Correcting on the fly in meeting. closing issues 358/357/356/347.

Issue #360 - Request Tentative stateen bit (refer to greg email on how to interact with AR).

Issue #348 – good point. to be addressed post 1.0.

Issue #355 – closed with pull #365.

Issue #307 closed with pull #362.

Issue #303 – mtvec tells you clic or clint mode. if in clint mode, should be as if clic didn't exist so behavior is just reserved.

Issue #349 - For indir accessing – think about as a struct. don't do packed vs. Unpacked. so better to do all by byte instead of some by bit and some by byte. so instead do both views.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#308/pull #325 – xnxti service loop behavior

#314 – shv==0 requirement for xnxti

#349 – discuss moving CLIC memory mapped registers to indirect CSRs

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – SPIKE model implementation of CLIC

#360 - Request Tentative stateen bit (refer to greg email on how to interact with AR).

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#329 - support for hw register save.

#348 – discuss location of inhv for future if enabling CLIC per mode. xcause still ok?