NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/12/19

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 4

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda TBD with new time slot)

Issue #349/pull #364 – discuss moving CLIC memory mapped registers to indirect CSRs

Issue #314 – shv==0 requirement for xnxti. more discussion needed. New CSR?

Meeting minutes:

If have two columns in one table, rather than two tables. combine ip with ie.

Not a big fan of overlaying index spaces for interrupt trigger. make clicintip RW not R or RW. register is RW but if level, writes are ignored.

Merged pull #366 for issue 303. CSR behavior when switching from CLIC/CLINT/CLIC added recommendation. #303 closed.

#308 – add nxti CSRRS to nxti form. applied pull. change pseudo code from uimm[4:0] to rs1, change 0 to x0. may need more checking of the pseudo-code.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#308/pull #325 – xnxti service loop behavior

#314 – shv==0 requirement for xnxti

#349 – discuss moving CLIC memory mapped registers to indirect CSRs

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – SPIKE model implementation of CLIC

#360 - Requested Tentative stateen bit (refer to greg email on how to interact with AR).

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#**329 -** support for hw register save.

#348 – discuss location of inhv for future if enabling CLIC per mode. xcause still ok?