NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/04/01

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 4

Meetings Disclaimers Video:

https://drive.google.com/file/d/1y XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:

https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

CLIC status:

[RVS-1017] Fast Interrupts (CLIC) - RISC-V Jira (riscv.org)

Meeting minutes:

ARC review starting. Krste will be reading through the whole spec. Expect it may take a couple weeks.

CLIC task group at June RISC-V Summit in Europe – Jean-Baptiste will be there and we received a 30 minute slot on the Monday task group day. We hope that CLIC will be nearing the ratification stage, so this might be a useful time to discuss Ecosystem phase and next steps after CLIC.

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

Need spec updates:

Awaiting feedback from Architecture Committee:

Issue #378 – Require immediate evaluation of clicintie and clicintip

Issue #349 reopened – moving memory mapped CLIC registers to indirect CSR access

Issues need to be worked in frozen stage:

#107 - heritage of features. keep researching and adding references to bibliography.

#376 – How should non-normative text be specified in the clic spec (appendix/in-line commentary?) For chapters 11 - 17.

Issues punted for rev1, keep open for future enhancements/ecosystem development:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#102 - preemptible interrupt handler code (for section 7.2)

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#329 - support for hw register save.

#348 – discuss location of inhy for future if enabling CLIC per mode. xcause still ok?

Ecosystem development phase

#185 – SAIL model implementation of CLIC – Pull created. Ecosystem phase of getting accepted

#186 – CLIC architecture tests – Pull created. Ecosystem phase of getting accepted

#187 – QEMU CLIC implementation update

#242 – SPIKE model implementation of CLIC