NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/03/04

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 3

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Clic spec moved to stable state. Goal is to start Frozen process by 4/1/2024. Please review the spec.

CLIC ACT tests:
Draft: Add m-mode, s-mode CLIC interrupt testcases by dansmathers · Pull Request #436 · riscv-non-isa/riscv-arch-test (github.com)
CLIC SAIL implementation:
Add unratified Smclic, Ssclic, Smclicshv extensions by dansmathers · Pull Request #420 · riscv/sail-riscv (github.com)
CLIC ratification JIRA flow:

[RVS-1017] Fast Interrupts (CLIC) - RISC-V Jira (riscv.org)

Next meeting agenda TBD with new time slot) issue

Issue #378 – Require immediate evaluation of clicintie and clicintip

Meeting minutes:

Implemented pull #370 closing #314 – xnxti now also returns SHV trap-handler entries. Note: this was reverted 3/5/24 because it was noticed this broke the SW interface. SW interrupt handler uses ret to return but HW vectored interrupt handlers use xret. Note: this was backed out shortly after the meeting. Issues #379/#381 pointed out that this change broke software interface.

Implemented pull #372 closing #371 – clicinttrig enable for signaling interrupts claimed by xnxti

Discussed pull #364 – has merge conflicts. fix and implement.

Implemented pull #373 – add xpil to mandatory reset state.

Implemented pull #369 – closed #158, #171, #226. Parameter definition change.

CLIC task group – JB will be at the June RISC-V Europe Summit. Should we try to organize a member discussion?

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

Need spec updates:

Need more discussion:

Issues need to be worked in frozen stage:

#107 - heritage of features. keep researching and adding references to bibliography.

#376 – How should non-normative text be specified in the clic spec (appendix/in-line commentary?) For chapters 11 – 17.

Issues punted for rev1, keep open for future enhancements/ecosystem development:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#102 - preemptible interrupt handler code (for section 7.2)

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#**329 -** support for hw register save.

#348 – discuss location of inhv for future if enabling CLIC per mode. xcause still ok?

Ecosystem development phase

#185 – SAIL model implementation of CLIC – Pull created. Ecosystem phase of getting accepted

#186 – CLIC architecture tests – Pull created. Ecosystem phase of getting accepted

#187 – QEMU CLIC implementation update

#242 – SPIKE model implementation of CLIC