NOTE: updated zoom info for next meeting and beyond.

Meeting link: https://zoom.us/j/95666422067

Passcode: 174425

Join link: https://zoom.us/j/95666422067?pwd=aHM1ZEJDcFJ3cGE0UWdTRmtaUXhsQT09

Date: 2023/08/29

Task Group: Fast Interrupts

Chair: Dan Smathers

Co-Chair: Jean-Baptiste Brelot

Number of Attendees: 4

Meetings Disclaimers Video :
https://drive.google.com/file/d/1y_XWJus8M5ZwSQ2cvEOzCjlOmsmXOnN4/view

Current issues on github: https://github.com/riscv/riscv-fast-interrupt/issues

Previous meeting minutes: https://github.com/riscv/riscv-fast-interrupt/tree/master/minutes

Fast Interrupt DoD (Definition of Done) Status:
https://wiki.riscv.org/display/HOME/Fast+Interrupts+TG

Next meeting agenda (09/12/23)

Issue #355 – mnstatus fields referenced seem wrong. location of latest rnmi spec?

Issue #349 – discuss moving CLIC memory mapped registers to indirect CSRs

Issue #348 – discuss location of inhv for future if enabling CLIC per mode

Issue #347/pull #354 – exception handler pseudocode needs checking

Issue #314 – shv==0 requirement for xnxti. more discussion needed. New CSR?

Issue #308/pull #325/pull #344– xnxti service loop – fix of pull #343 based on discussion.

Issue #307/pull #331 – Parameter cleanup (compare with pull #297?)

Issue #303 – How are CLIC-only CSRs and fields handled in CLINT mode

Meeting minutes:

Issue #351/pull #352 – fix documentation of reserved areas in memory map.

Discussed #351 – accepted pull. Closed.

Issue #350/pull #353 – clarify when mscratchcsw is required.

Discussed #350 – accepted pull. Closed.

Discussing #339 – do we need to document debug mode not affecting mcause.mpil? fix text that says xcause.pil is updated to match xstatus.il. should be xintstatus.il. debug spec describes how to catch interrupts. in debug, ebreak enters debug mode. if don't have debug enabled, break should jump to exception handler. if go to debug mode, goes to interrupt level 0 debug mode. typo fixed. Closed.

For #347 – create a new signal masked_xepc and have both check fetch_permissions and mem_read use that masked_xepc and get rid of ~1 in that section. fix then bracket. clog2(XLEN/8) bits. keep working on pseudo-code.

For issue #345 – actually want to trap when smstateen0 is 0. don't just appear hardwired to 0. fix pull. Pull accepted but text updated during task group. Closed.

Discussed #349 – big change. try to discuss more via email before next fast-interrupt TG meeting.

SAIL pulls discussion: how to create multiple pulls from a github fork.

Create a fork. then branch at root of my fork:get hash number and create a fork and give it a name, then make changes there and do pull request. command line switch if supports extension – c file: c_emulator/riscv_sim.c

Github updates since last minutes:

Specification updates since last minutes:

Open issue status:

Issues that can be closed?

#307/pull #331 – NUM_INTERRUPT listed in two sections (text cleanup)

Need spec updates:

#158 – change CLICCTRLBITS to CLICMLPBITS. (resolve #226 first?)

#171 – CLICCFGLBITS parameter - related to #80, #158. (resolve #226 first)

Pull #286 – text update fix for #96/158/171/226/49 - allow multiple implementations for priv mode/level.

Need more discussion:

#102 - preemptible interrupt handler code (for section 7.2)

#226 – replace clicintattr.mode with xcliccfg.xlvl proposal (formerly #96)

#303 - How are CLIC-only CSRs and fields handled in CLINT mode?

#308/pull #325 – xnxti service loop behavior

#314 – shv==0 requirement for xnxti

#355 – mnstatus fields referenced seem wrong. location of latest rnmi spec?

#349 – discuss moving CLIC memory mapped registers to indirect CSRs

#348 – discuss location of inhv for future if enabling CLIC per mode

#347/pull #354 – exception handler pseudocode needs checking

Issues need to be worked:

#91 – DTS entry – have linux group review DTS example. If add CLINT compatibility option, just use same DTS entry as clint?

#107 - heritage of features. keep researching and adding references to bibliography.

#185 – SAIL model implementation of CLIC

#186 – CLIC architecture tests

#187 – QEMU CLIC implementation update

#221 – compressed clicintip/clicintie status registers (1-bit per interrupt) similar to AIA eip0-eip63? Add justification and create a pull with a proposal. Pull #270. add prior art reference.

#242 – SPIKE model implementation of CLIC

Issues punted for rev1, keep open for future enhancements:

#92/Pull #281 – hypervisor compatibility. still punted for rev1?

#99 – horizontal interrupt window. punted for rev1

#101 - xnxti to trigger on equal level. punted for rev1

#106 – allow level change. Punted for rev1

#108 – pushint/popint? defer to broader discussion on providing hardware stacking of interrupt contexts. Punted for rev1

#192 – allow mix of CLIC/CLINT at different priv modes punted for rev1

#248 – CLIC hypervisor mode (related to #92).

#**329** - support for hw register save.