RN0197

MIV_RV32IMA_L1_AXI V2.0 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300197-1/3.18

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for MIV_RV32IMA_L1_AXI v2.0.

Contents

2 MIV_RV32IMA_L1_AXI v2.0 Release Notes

2.1 Overview

These release notes accompany the production release of MIV_RV32IMA_L1_AXI v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

MIV_RV32IMA_L1_AXI has the following features:

- Designed for low power ASIC microcontroller and FPGA soft-core implementations
- Integrated 8Kbytes instructions cache and 8 Kbytes data cache
- A Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupt with a single priority level
- Supports the RISCV standard RV32IMA ISA
- On-Chip debug unit with a JTAG interface
- Two external interfaces for IO and memory

2.3 Delivery Types

No License is required to use MIV_RV32IMA_L1_AXI. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

MIV_RV32IMA_L1_AXI v2.0 requires Libero® System-on-Chip (SoC) v11.8 or later.

2.6 Installation Instructions

The MIV_RV32IMA_L1_AXI CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *MIV_RV32IMA_L1_AXI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

No testbench is provided with MIV_RV32IMA_L1_AXI.

The MIV_RV32IMA_L1_AXI RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

2.9 Resolved History

Table 1 lists the release history for MIV_RV32IMA_L1_AXI.

Table 1 • **Release History**

Version	Date	Changes
2.0	March 2018	Initial release.

2.10 Known Limitations and Workarounds

There are no known limitations and workarounds for MIV_RV32IMA_L1_AXI.