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MIV_RV32IMA_L1_AHB v2.1
Release Notes

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated for MIV_RV32IMA_L1_AHB v2.1. Added cache with ECC, Debug reset, and external debug halt features.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for MIV_RV32IMA_L1_AHB v2.0.

Contents

3 MIV_RV32IMA_L1_AHB v2.1 Release Notes

3.1 Overview

These release notes accompany the production release of MIV_RV32IMA_L1_AHB v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, known issues, and workarounds.

3.2 Features

- Designed for FPGA soft-core implementation.
- Integrated 8Kbytes instructions cache and 8Kbytes data cache.
- A Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupts with a single priority level.
- Supports the RISC-V standard RV32IMA ISA.
- On-Chip debug unit with a JTAG interface.
- Two external AHB interfaces for IO and memory.
- External HALT signal can halt processor execution during a debug session.
- Support for Error-Correcting Code (ECC) caches on RTG4 and PolarFire.

3.3 Delivery Types

MIV_RV-32IMA_L1_AHB does not require license. Complete RTL source code is provided for the core.

3.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3.5 Supported Tool Flows

MIV_RV-32IMA_L1_AHB requires Libero® System-on-Chip (SoC) software v11.8 or later. For RTG4 designs with ECC Libero System-on-Chip (SoC) software v11.8 SP4 or later is recommended.

3.6 Installation Instructions

The MIV_RV-32IMA_L1_AHB CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the *MIV_RV-32IMA_L1_AHB Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

No testbench is provided with MIV_RV32IMA_L1_AHB.

The MIV_RV32IMA_L1_AHB RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

3.9 Known Limitations and Workarounds

There are no known limitations and workarounds for MIV_RV-32IMA_L1_AHB.