

Compressed-decoder-SV

This file implements RV for RV32C, explained in chapter 16
of RISC-Spec see pg 123 for info, 112 for instruction set listing !!

1) BLACK BOX

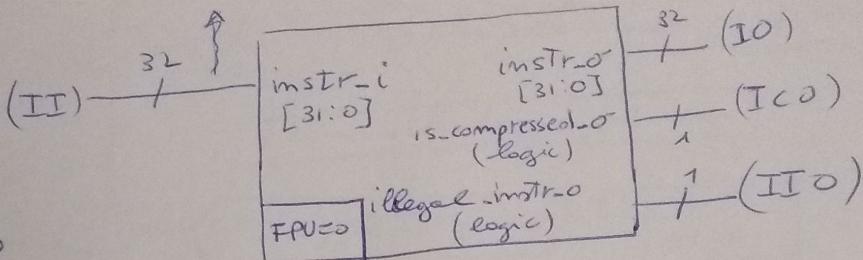
ABBREVIATION

instr-i \Rightarrow II.

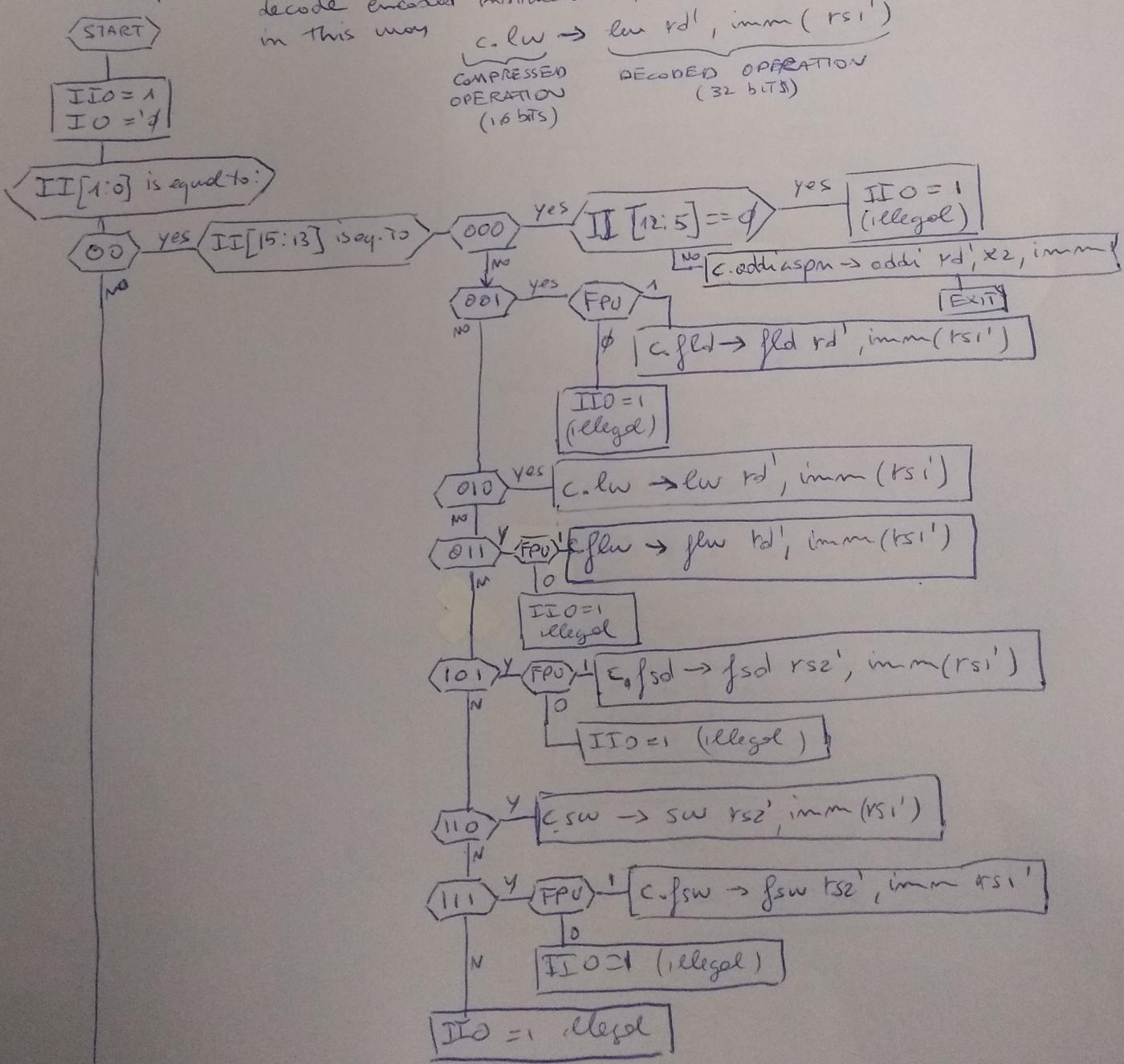
instr-o \Rightarrow IO

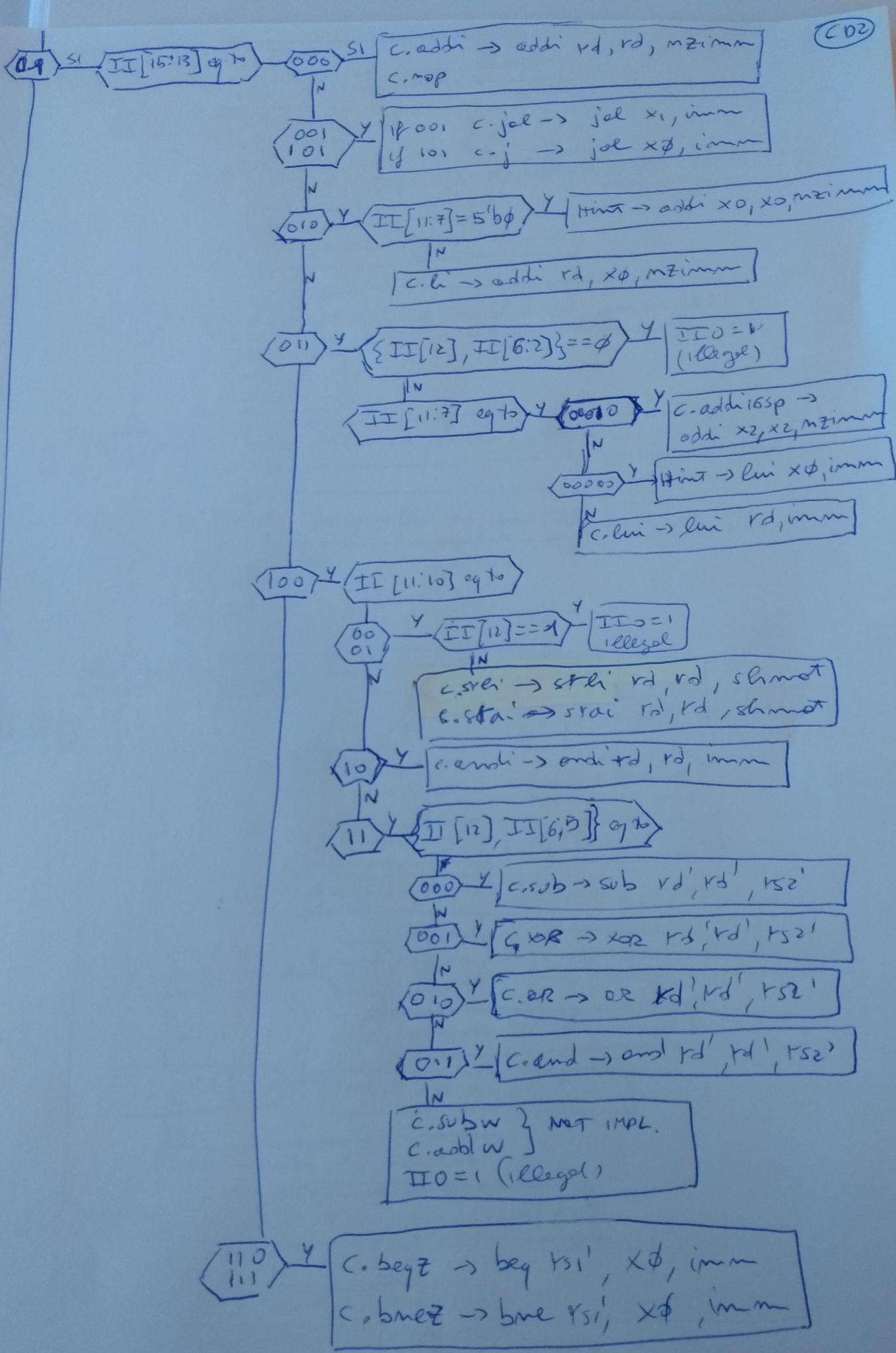
is-compressed-o \Rightarrow ICO

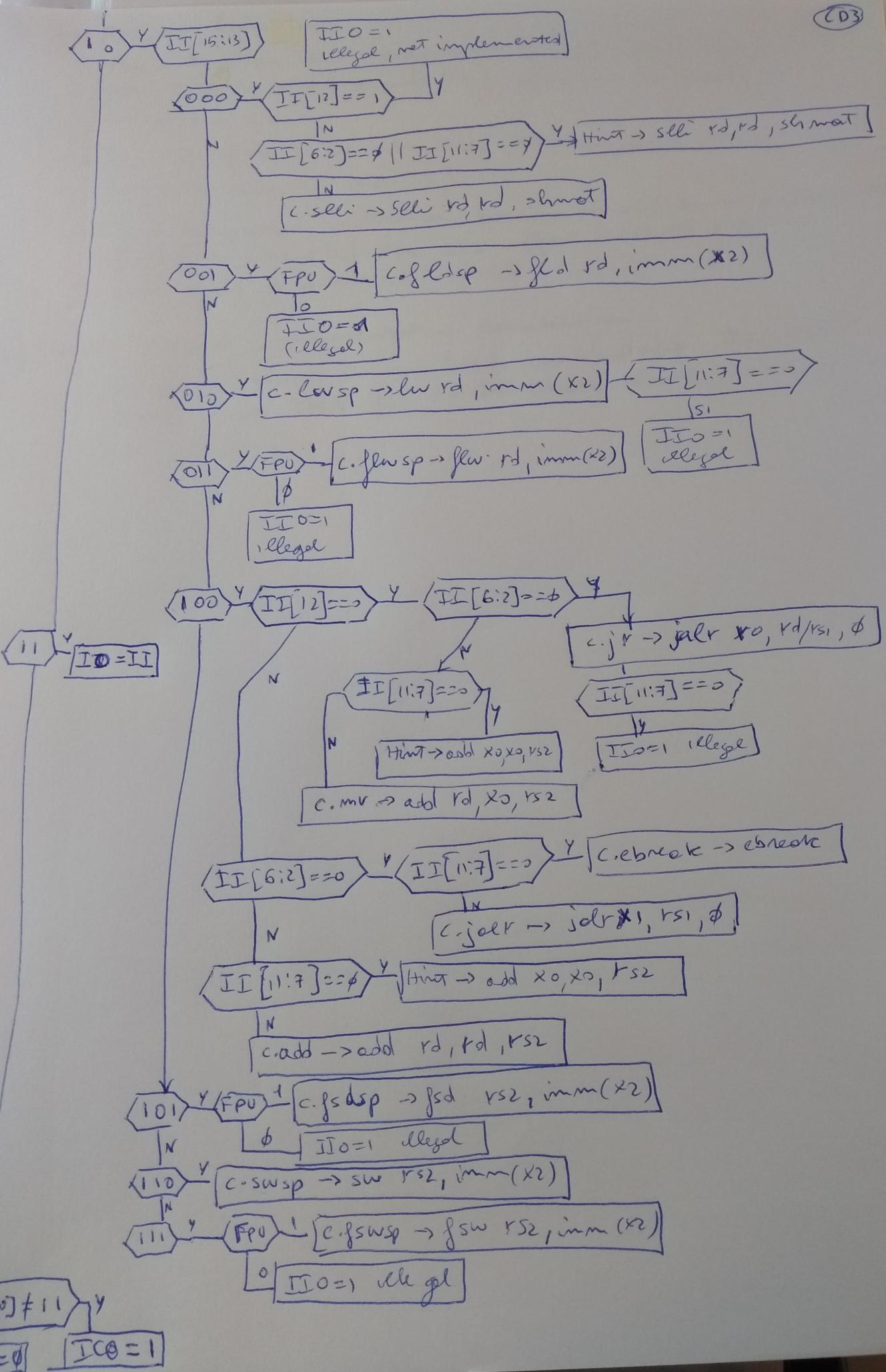
illegal-instr-o \Rightarrow IIO



2) flow diagram of System Verilog code, this flow diagram is implemented in a completely combinatory block. This block decode encoded instruction, this conversion is represented in this way







3) flow diagram description:

- The instruction is compressed only if $II[1:0] \neq 11$, in this case $IC\oplus$ is set to 1 and The \oplus instruction is decoded and saved in IO
- If $II[1:0] = 11$ The instruction isn't compressed and is copied to output ($FO = II$) .
- If a compressed instruction ~~is~~ an invalid or non implemented funct code ($II[15:13]$) The IIO output is asserted and The instruction is considered invalid

4) Fault tolerant implementation consideration :

- Since the block is completely combinatoric the easiest way is use TMR for the ~~the~~ whole block probably.