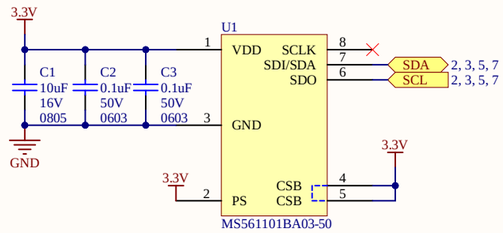


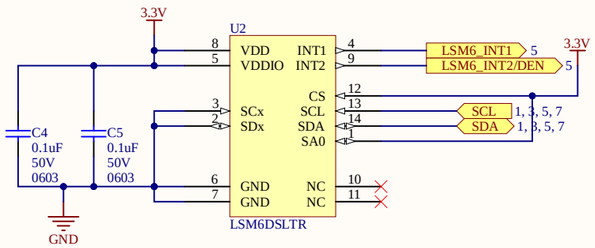
COMMANDS

Each I²C communication message starts with the start condition and it is ended with the stop condition. The MS5611-01BA address is 111011Cx, where C is the complementary value of the pin CSB. Since the IC does not have a microcontroller inside, the commands for I²C and SPI are quite similar.

Address: 1110110 0x76

SHEET NAME: MS5611.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Sam Larson	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

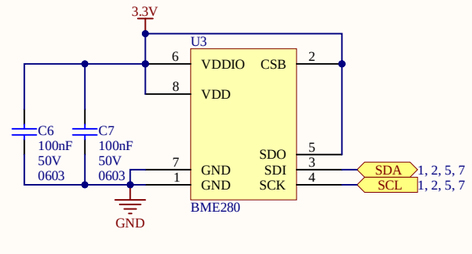


Address: 1101011 : 0x6B

SHEET NAME: LSM6DSL.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Mary Dertinger	DATE: 5/19/2024

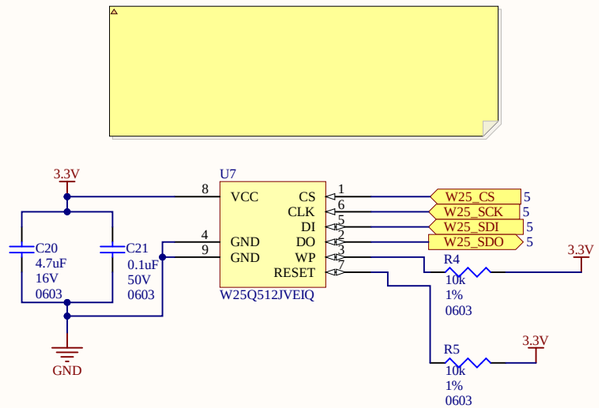
RIT LAUNCH INITIATIVE

Address: 1110111
0x77



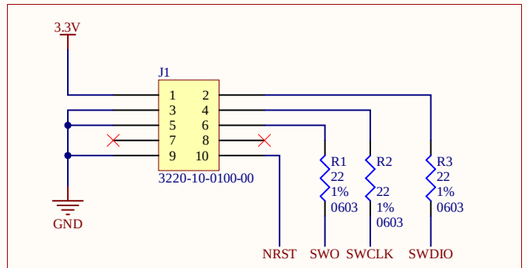
SHEET NAME: BME280.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Alex Moczarski	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

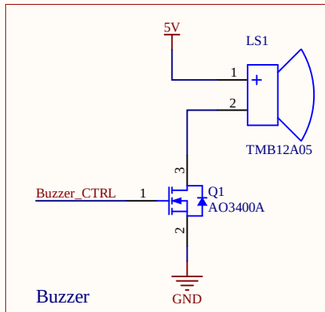


SHEET NAME: W25Q128JVSIQ.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Alex Moczarski	DATE: 5/19/2024

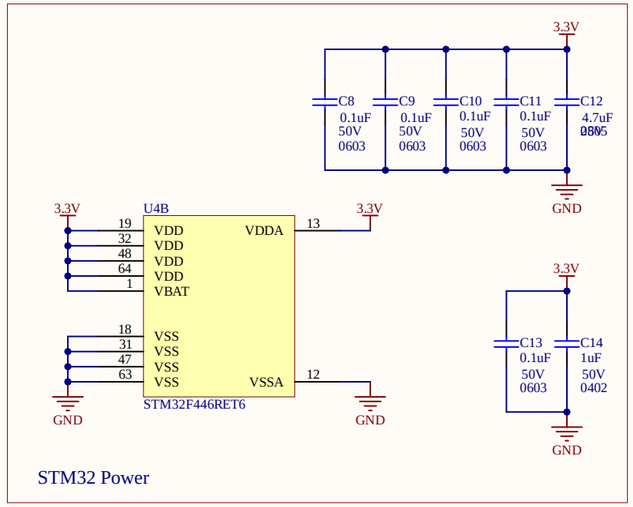
RIT LAUNCH INITIATIVE



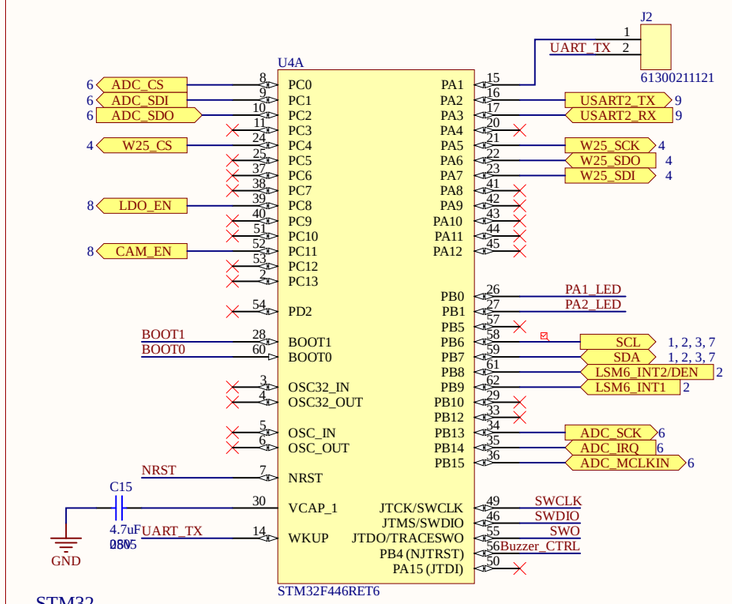
SWD Connector



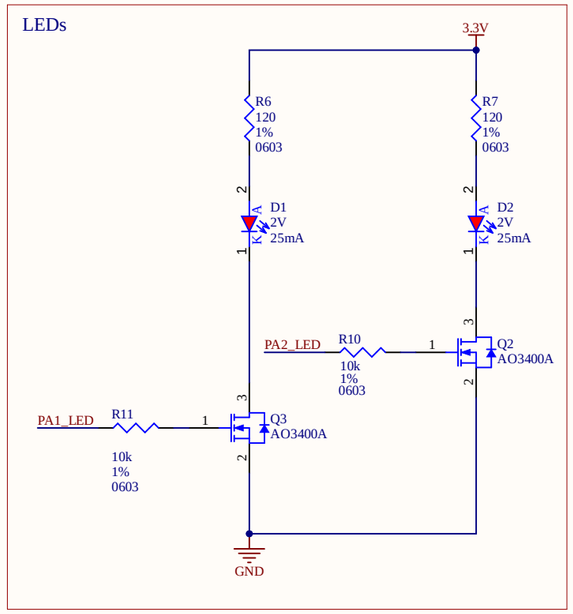
Buzzer

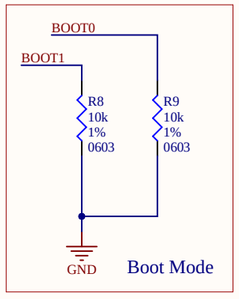


STM32 Power

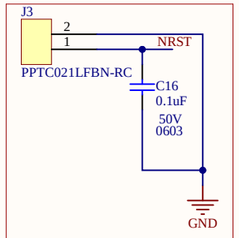


STM32

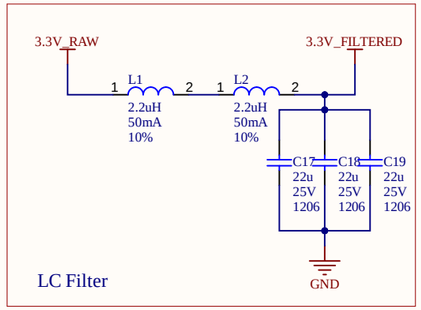




Boot Mode



Reset Header

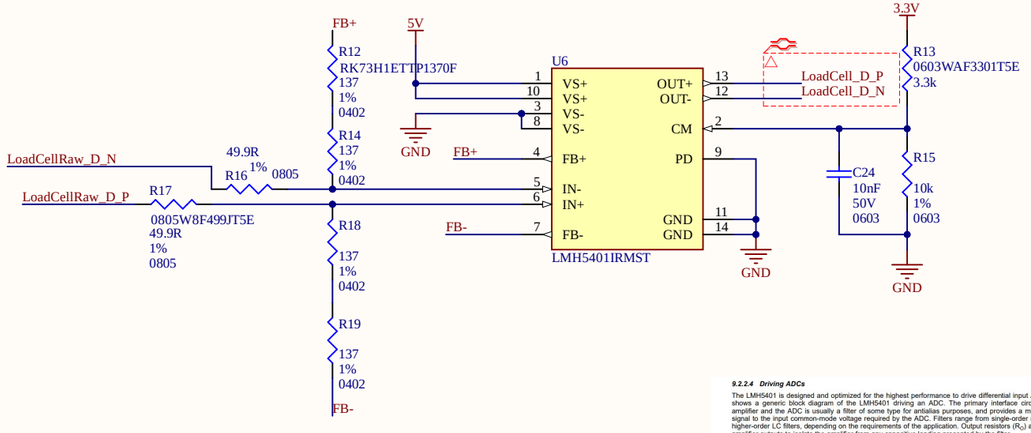


LC Filter

SHEET NAME: STM32.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Alex Moczarski	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

Differential Op Amp



8.3.4 Output Common-Mode Voltage

The CM input controls the output common-mode voltage. CM has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. The CM input impedance is very high and bias current is not critical. The CM input has no internal reference and must be driven from an external source. Using a bypass capacitor is required. A capacitor value of 0.01 µF is recommended. For best harmonic distortion, maintain the CM input within ±1 V of the midsupply voltage using a 5-V supply and within ±0.5 V when using a 3.3-V supply. The CM input voltage can operate outside this range if a lower output swing is used or distortion degradation is allowed. For more information, see Figure 21 and Figure 22.

9.2.2.4 Driving ADCs

The LMH5401 is designed and optimized for the highest performance to drive differential input ADCs. Figure 68 shows a generic block diagram of the LMH5401 driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter of some type for antialias purposes, and provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

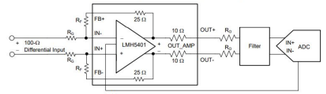


Figure 68. Differential ADC Driver Block Diagram

Pin Functions

PIN NAME	PIN NO.	TYPE	DESCRIPTION
CM	2	I	Input pin to set amplifier output common-mode voltage
FB–	7	O	Negative output feedback component connection
FB+	4	O	Positive output feedback component connection
GND	11, 14	P	Power down ground. See Power Down and Ground Pins
IN–	5	I	Negative input pin
IN+	6	I	Positive input pin
OUT–	12	O	Negative output pin
OUT+	13	O	Positive output pin
PD	9	I	Power-down (logic 1 = power down). See Power Down and Ground Pins
VS–	3, 8	P	Negative supply voltage
VS+	1, 10	P	Positive supply voltage

Frequency Response (continued)

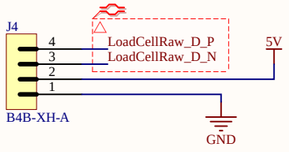
For tests with differential inputs, the same setup for single-ended inputs is used except all four connectors are connected to a network analyzer port. Measurements are made in true differential mode on the Rohde & Schwarz® network analyzer or in calculated differential mode. In each case, the differential inputs are each driven with a 50-Ω source. Table 1 and Table 2 lists the resistor values used in frequency response sweeps.

Table 1. Differential Input/Output

A_V (V/V)	R_{G1}, R_{G2} (Ω)	R_F (TOTAL / EXTERNAL, Ω)	R_T (Ω)
2	100	199 / 174	100
4	49.9	199 / 174	N/A
6	49.9	300 / 274	N/A
8	49.9	400 / 375	N/A
10	49.9	500 / 475	N/A

LoadCell Connector

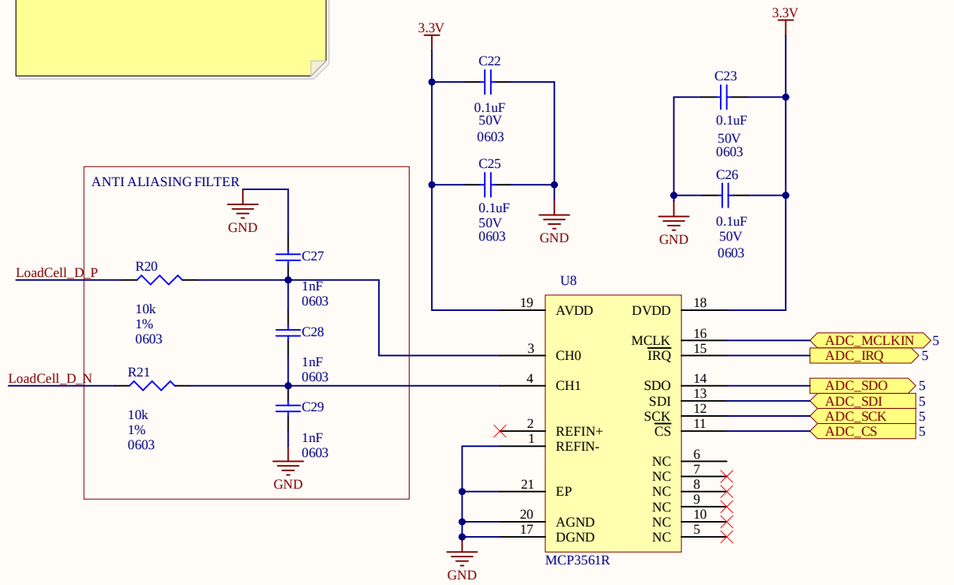
Load Cell Signals:
EXC+ = 5V
EXC- = GND
SIG - = LoadCell Raw-
SIG + = LoadCell Raw+



Wiring	EXC+: Red, EXC-: Black, SIG+: Green, SIG-: White

ADC

Anti aliasing filter cut off at 5.3 Khz. CM volatge is 2.4V



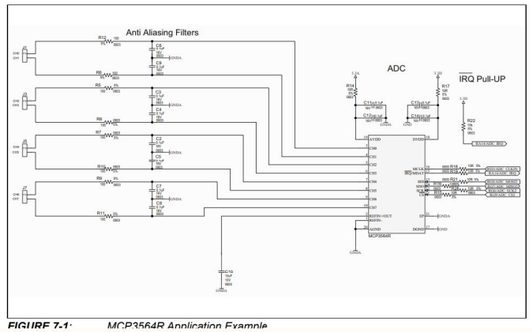


FIGURE 7-1: *MCP3564R Application Example*

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN FUNCTION TABLE

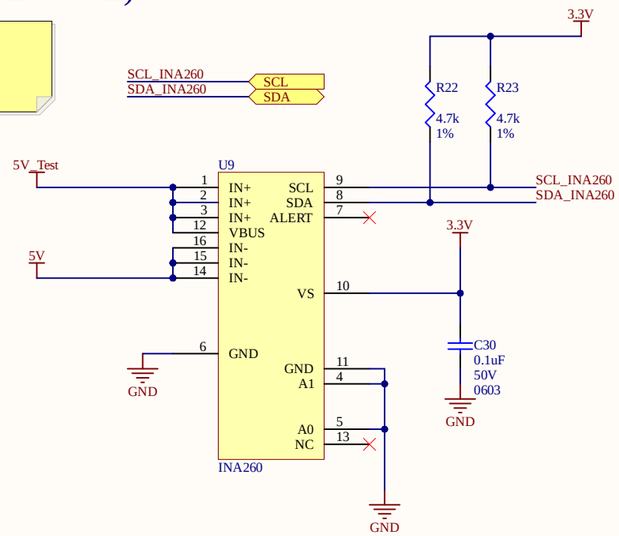
MCP3561	MCP3562	MCP3564	MCP3561	MCP3563	MCP3564	Symbol	Description
20-Lead UQFN			20-Lead TSSOP				
1			3			REFIN-	Inverting Reference Input Pin
2			4			REFIN+	Noninverting Reference Input Pin
3			5			CH0	Analog Input 0 Pin
4			6			CH1	Analog Input 1 Pin
—	5	5	—	7	7	CH2	Analog Input 2 Pin
—	6	6	—	8	8	CH3	Analog Input 3 Pin
—	—	7	—	—	9	CH4	Analog Input 4 Pin
—	—	8	—	—	10	CH5	Analog Input 5 Pin
—	—	9	—	—	11	CH6	Analog Input 6 Pin
—	—	10	—	—	12	CH7	Analog Input 7 Pin
11			13			$\overline{CS}$	Serial Interface Chip Select Digital Input Pin
12			14			SCK	Serial Interface Digital Clock Input Pin
13			15			SDI	Serial Interface Digital Data Input Pin
14			16			SDO	Serial Interface Digital Data Output Pin
15			17			$\overline{IRQ}$/MDAT	Interrupt Output Pin or Modulator Output Pin
16			18			MCLK	Master Clock Input or Analog Master Clock Output Pin
17			19			D_{GND}	Digital Ground Pin
18			20			DV_{DD}	Digital Supply Voltage Pin
19			1			AV_{DD}	Analog Supply Voltage Pin
20			2			A_{GND}	Analog Ground Pin
5, 6, 7, 8, 9, 10		—	7, 8, 9, 10, 11, 12		—	NC	Not Connected
21			—		—	EP	Exposed Thermal Pad, internally connected to A_{GND}

SHEET NAME: MCP3561R_ADC.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Mary Dertinger	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

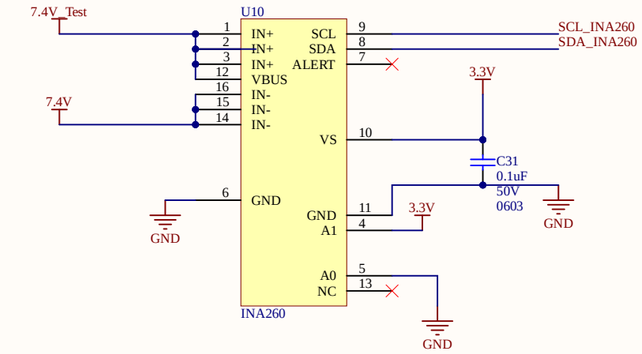
5V Rail (LDO to Loadcell)

Slave address 1000000 : 0x40



7.4V (Battery)

Slave address 1000100 : 0x44



3.3V Rail (Buck to grim)

Slave address 1000001 : 0x41

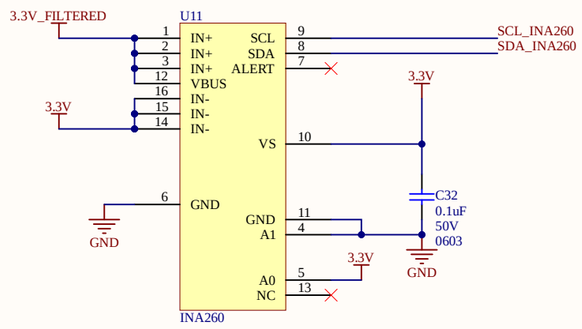


Table 2. Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

9.2 Typical Application

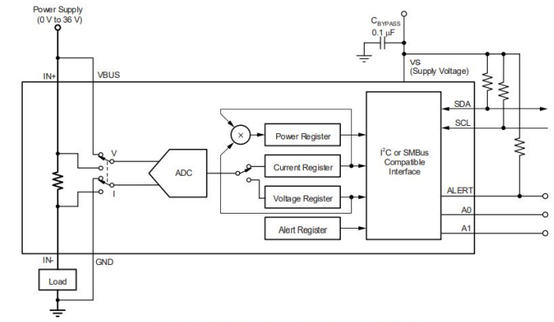


Figure 38. Typical Circuit Configuration, INA260

If ALERT is not being used it can be left floating. NC can be grounded or left floating

8.5.3 Communications Bus Overview

The INA260 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another.

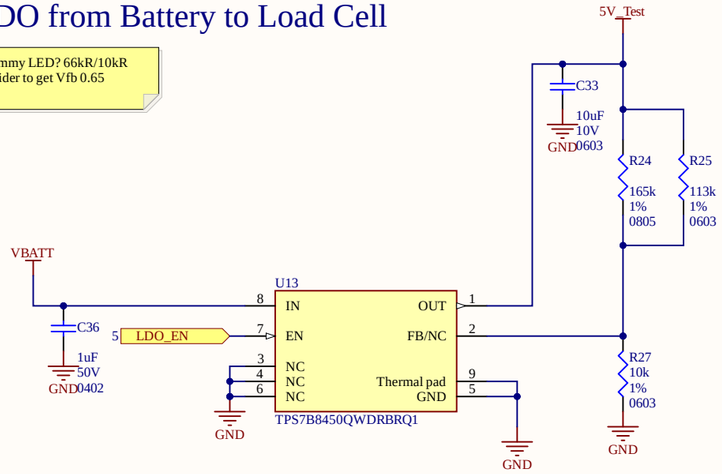
The I²C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two lines, SCL and SDA, connect the device to the bus. Both SCL and SDA connect to the bus and require external pullup resistors.

SHEET NAME: INA260.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Mary Dertinger	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

LDO from Battery to Load Cell

Dummy LED? 66kR/10kR divider to get Vfb 0.65



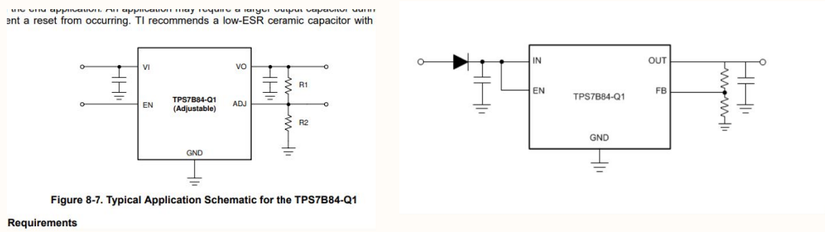
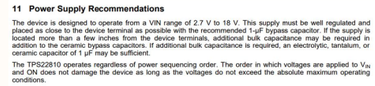


Figure 8-7. Typical Application Schematic for the TPS7B84-Q1

Requirements

Battery Rail @ 7.4V goes to Cameras

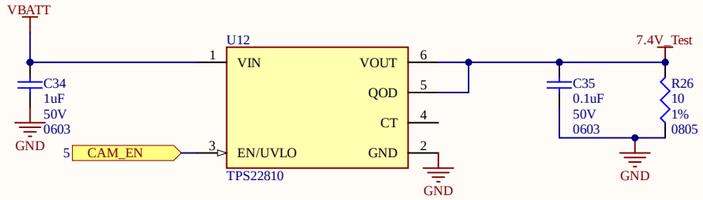
Cin to Cout 10:1 ratio, suggested 1 uF for Cin. CT is switch slew rate control and can be left floating. NOTE should be near power. Also sould I stick with 11.1V port or is that confusing?



11 Power Supply Recommendations

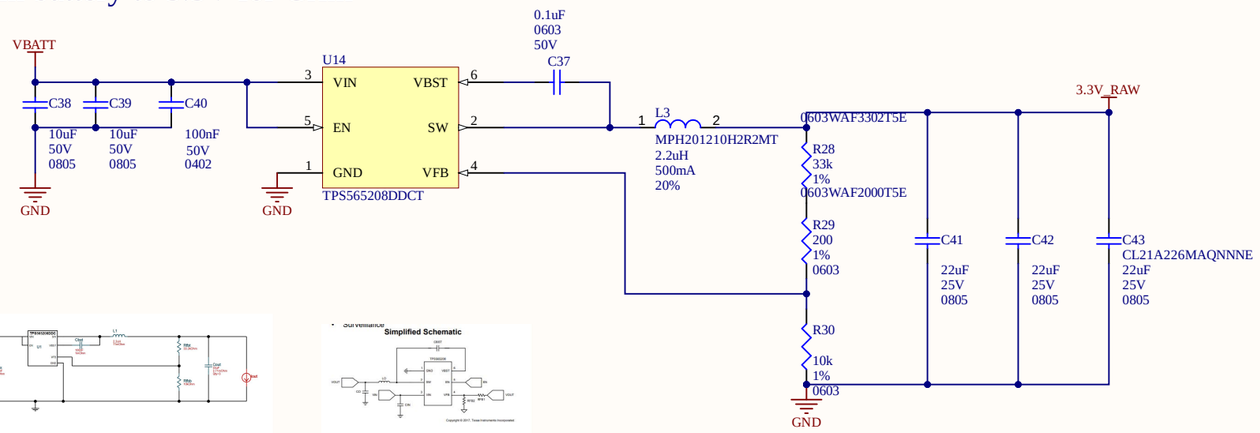
The device is designed to operate from a VIN range of 2.7 V to 18 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

The TPS22810 operates regardless of power sequencing order. The order in which voltages are applied to V_{IN} and ON does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions.

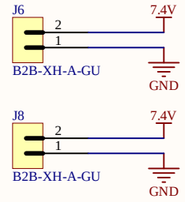


Screw Switch --> to Battery

Buck from battery to 3.3V for Grim



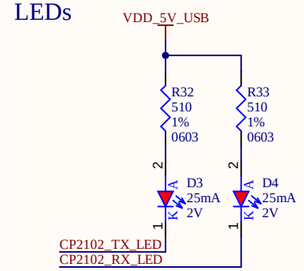
JSTXH Goes to Camera



SHEET NAME: Power.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Mary Dertinger	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

LEDs



USB to UART

Connect RSTb to VIO via 1k resistor

Connect TXD and RXD to other device

Create differential pair routing design rule for USB and apply it to the USB diff pair net class (90ohm characteristic differential impedance)

SHEET NAME: USB.SchDoc	PROJECT: GRIM_Reefer.PrjPcb
ENGINEER: Ben Hyman	DATE: 5/19/2024

RIT LAUNCH INITIATIVE