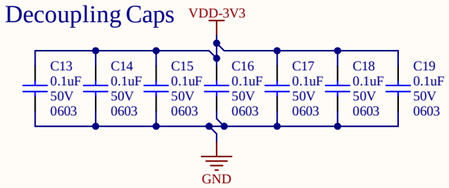
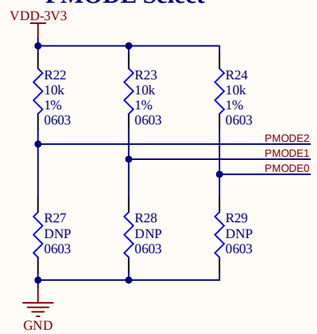
Decoupling Caps

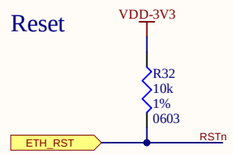


PMODE Select

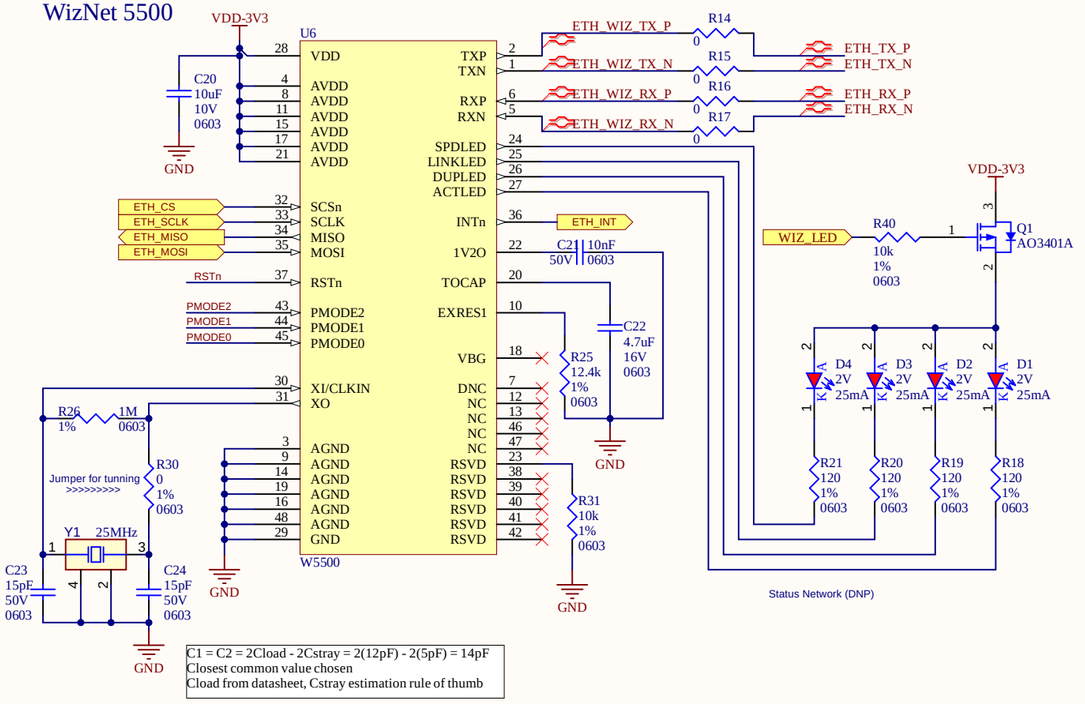
PMODE [2:0]			Description
2	1	0	
0	0	0	10BT Half-duplex, Auto-negotiation disabled
0	0	1	10BT Full-duplex, Auto-negotiation disabled
0	1	0	100BT Half-duplex, Auto-negotiation disabled
0	1	1	100BT Full-duplex, Auto-negotiation disabled
1	0	0	100BT Half-duplex, Auto-negotiation enabled
1	0	1	Not used
1	1	0	Not used
1	1	1	All capable, Auto-negotiation enabled



Reset



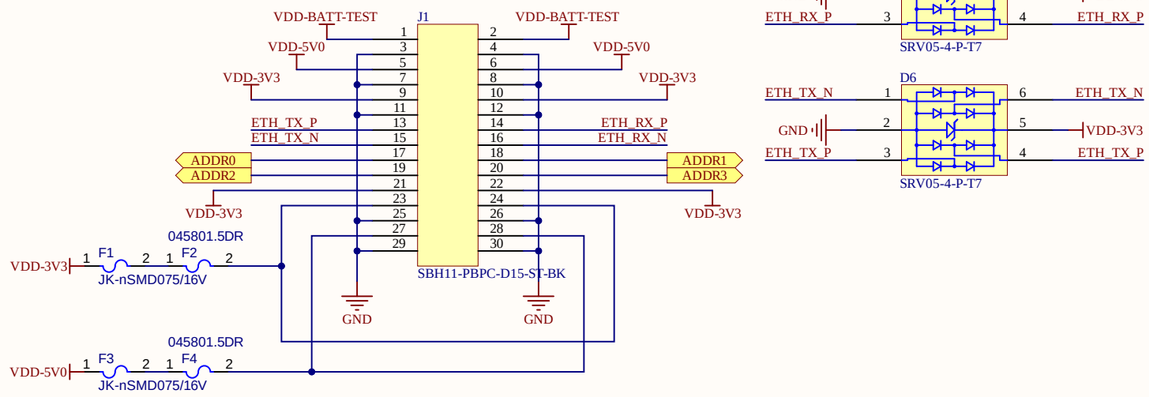
WizNet 5500



Backplane Connector Pinout

Pinout

Description	PIN		Description
Battery Voltage	1	2	Battery Voltage
GND	3	4	GND
5v	5	6	5v
GND	7	8	GND
3v3	9	10	3v3
GND	11	12	GND
TX+	13	14	RX+
TX-	15	16	RX-
ADDR 0 (LSB)	17	18	ADDR 1
ADDR 2	19	20	ADDR 3 (MSB)
Power LED	21	22	Status LED
GPIO 0	23	24	GPIO 1
GPIO 2	25	26	GPIO 3
GPIO 4	27	28	GPIO 5
GPIO 6	29	30	GPIO 7



Backplane Connector

SHEET NAME: Backplane_Interface.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

Switchers
Switchers.SchDoc

Backplane_Interface
Backplane_Interface.SchDoc

ETH_SCLK
ETH_RST
ETH_MOSI
ETH_MISO
ETH_INT
ETH_CS
ADDR3
ADDR2
ADDR1
ADDR0
WIZ_LED

MCU
MCU.SchDoc

ETH_SCLK
ETH_RST
ETH_MOSI
ETH_MISO
ETH_INT
ETH_CS
ADDR3
ADDR2
ADDR1
ADDR0
WIZ_LED
VIN_VOLTAGE_SENSE
SENSE_SCL
SENSE_SDA
MEM_CS
MEM_SCLK
MEM_MISO
MEM_MOSI

Voltage_Current_Sense
Voltage_Current_Sense.SchDoc

VIN_VOLTAGE_SENSE
SENSE_SCL
SENSE_SDA

Memory
Memory.SchDoc

MEM_CS
MEM_SCLK
MEM_MISO
MEM_MOSI

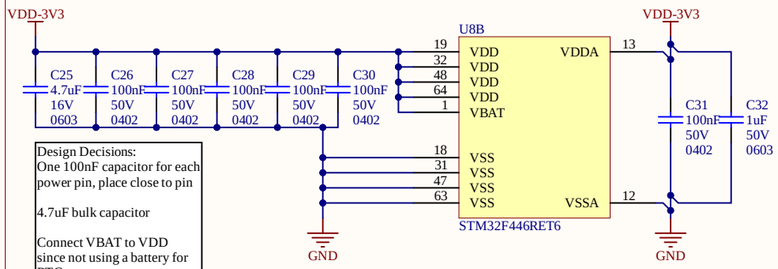
MH1
Mounting_Hole_3mm_PT
MH2
Mounting_Hole_3mm_PT
MH3
Mounting_Hole_3mm_PT
MH4
Mounting_Hole_3mm_PT

Mounting Holes

SHEET NAME: Main.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

STM32 Power



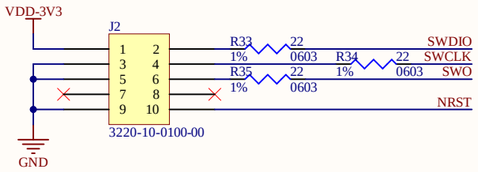
Design Decisions:
One 100nF capacitor for each power pin, place close to pin

4.7uF bulk capacitor

Connect VBAT to VDD since not using a battery for RTC

Don't need separate analog and digital domains, so connect VDDA and VSSA to regular power

SWD Connector



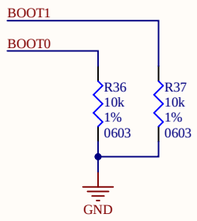
Design Decisions:
1.27mm header for SWD flashing + debugging

22ohm series termination resistors on each data line to reduce reflections

Boot Mode

Table 2. Boot modes

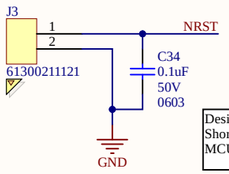
Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as the boot area
0	1	System memory	System memory is selected as the boot area
1	1	Embedded SRAM	Embedded SRAM is selected as the boot area



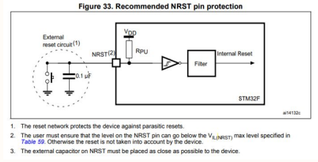
Design Decisions:
Connect both BOOTx pins to GND for booting from flash

Don't foresee needing to boot from elsewhere

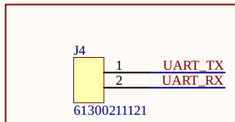
Reset



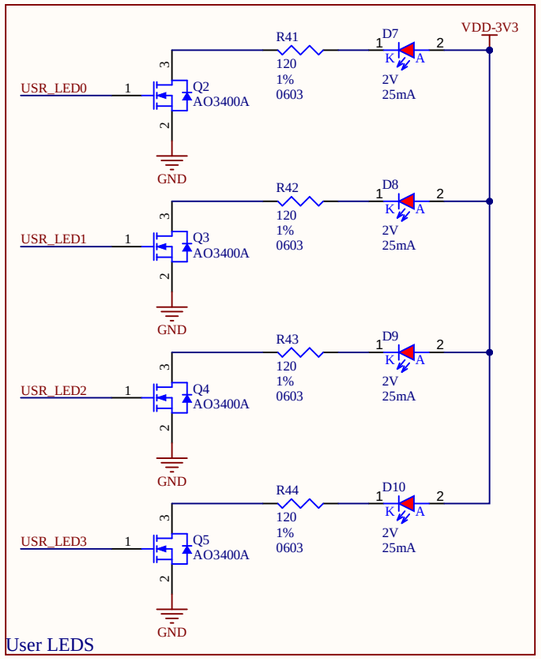
Design Decisions:
Short jumper to reset MCU, as per datasheet



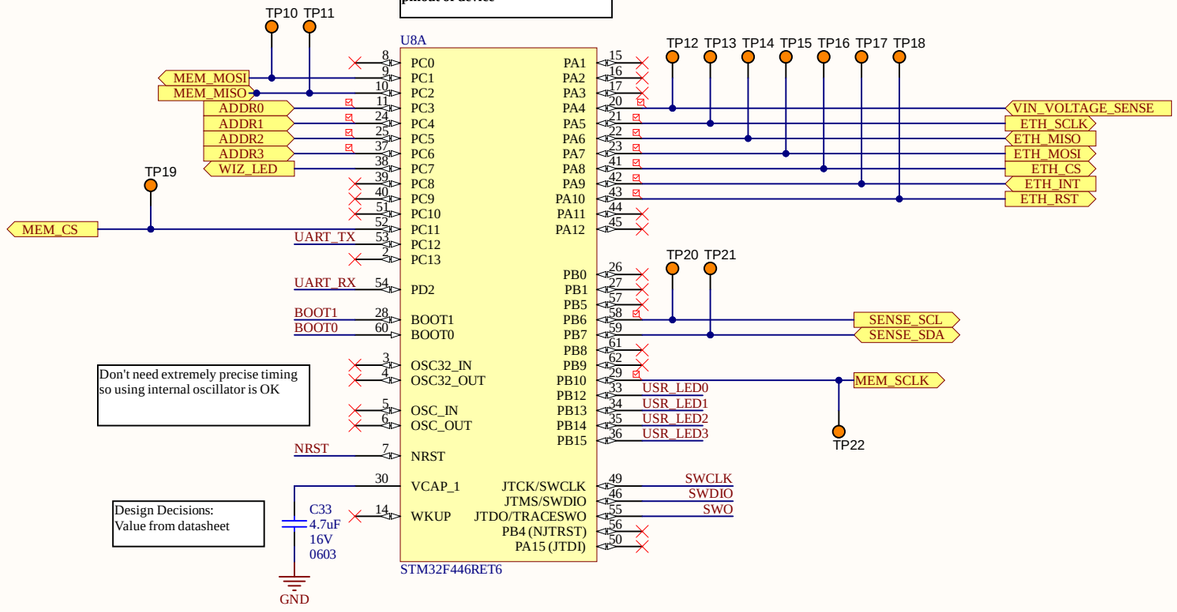
Debug UART



User LEDS



Make a project in STM32CubeIDE and use the GUI to determine pinout of device

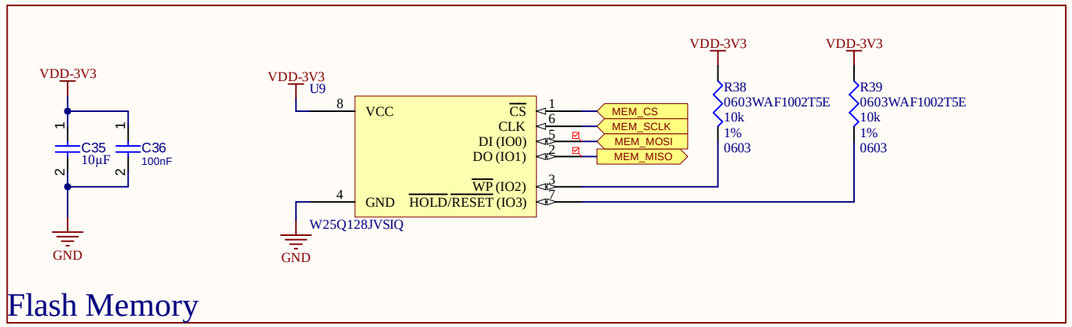


Don't need extremely precise timing so using internal oscillator is OK

Design Decisions:
Value from datasheet

SHEET NAME: MCU.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE



Flash Memory

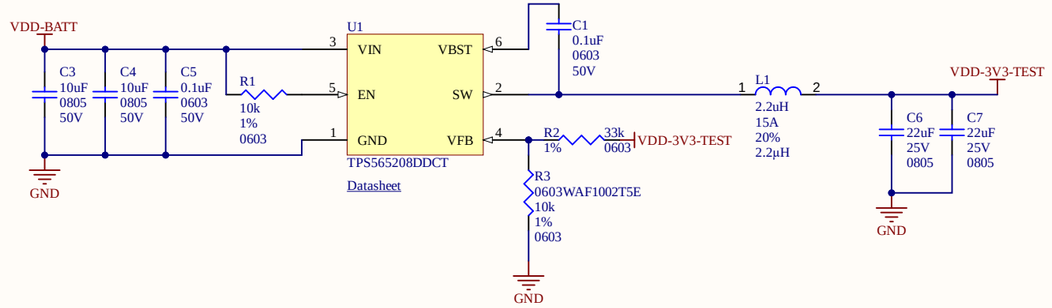
SHEET NAME: Memory.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE

Protections:
-UVLO: shutdown if VIN < 3.6 (non-latching)
-OCL: shutdown if IOUT > 6.7A
-VOUT: shutdown if VOUT +-65% nominal
-Thermal: shutdown if T > 172C

Switching Frequency: 550 kHz

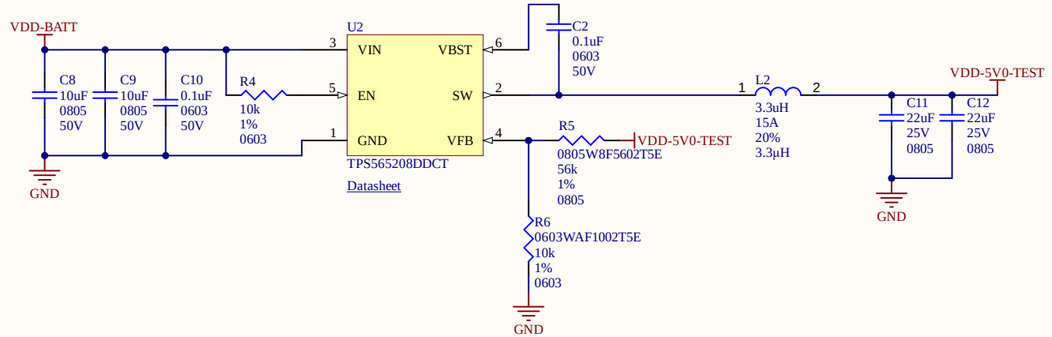
Simulation



3V3 Switcher

Switching Frequency: 550 kHz

Simulation



5V Switcher

- 5-A Maximum Output Current
- Integrated 31-mΩ and 16-mΩ FETs
- D-CAP2™ Mode Control with Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Continuous Current Mode
- 500-kHz Switching Frequency
- Low Shutdown Current of Less than 1 µA
- 1% Feedback Voltage Accuracy
- Startup from Pre-biased Output Voltage
- Cycle-by-Cycle Current Limit
- Hiccup-mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms

8.2 Typical Application

The application schematic in Figure 14 shows the TPS565208 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 5-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

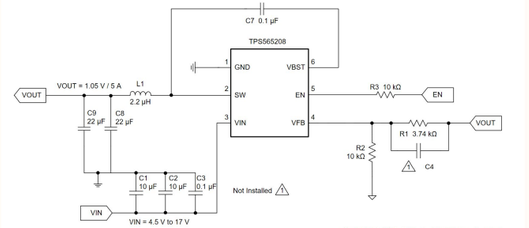
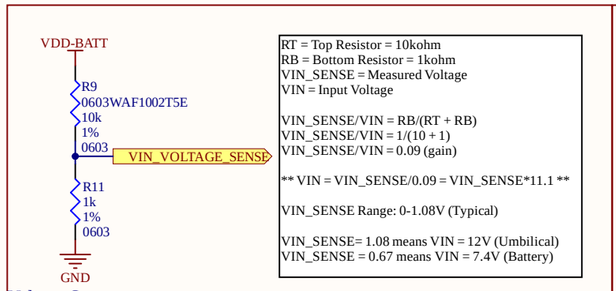


Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1	2.2	4.7	20 to 68
1.05	3.74	10.0	1	2.2	4.7	20 to 68
1.2	5.76	10.0	1	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

SHEET NAME: Switchers.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE



RT = Top Resistor = 10kohm
RB = Bottom Resistor = 1kohm
VIN_SENSE = Measured Voltage
VIN = Input Voltage

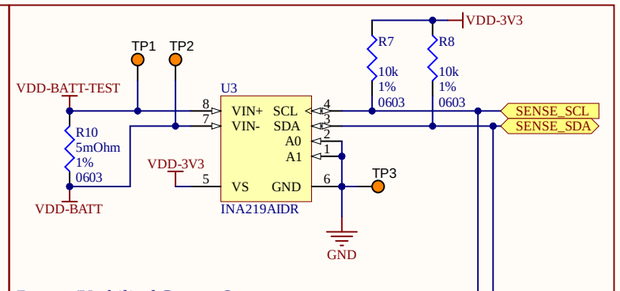
VIN_SENSE/VIN = RB/(RT + RB)
VIN_SENSE/VIN = 1/(10 + 1)
VIN_SENSE/VIN = 0.09 (gain)

** VIN = VIN_SENSE/0.09 = VIN_SENSE*11.1 **

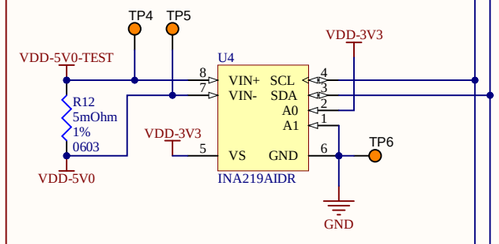
VIN_SENSE Range: 0-1.08V (Typical)

VIN_SENSE= 1.08 means VIN = 12V (Umbilical)
VIN_SENSE = 0.67 means VIN = 7.4V (Battery)

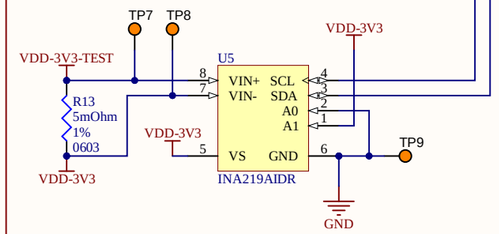
Voltage Sense



Battery/Umbilical Current Sense



5V Rail Current Sense



3V3 Rail Current Sense

Table 1. INA219 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V_{S+}	GND	1000100
V_{S+}	V_{S+}	1000101
V_{S+}	SDA	1000110
V_{S+}	SCL	1000111
SDA	GND	1001000
SDA	V_{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

```
i2c Slave Addresses:

Battery/Umbilical Address: 1000000 0x40
          3V3 Rail Address: 1000100 0x44
          5V0 Rail Address: 1000001 0x41
```

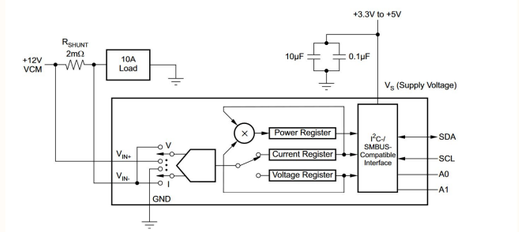


Figure 29. Example Circuit Configuration

SHEET NAME: Voltage_Current_Sense.SchDoc	PROJECT: Power_Module_Rev2.PrjPcb
ENGINEER: James May	DATE: 5/19/2024

RIT LAUNCH INITIATIVE