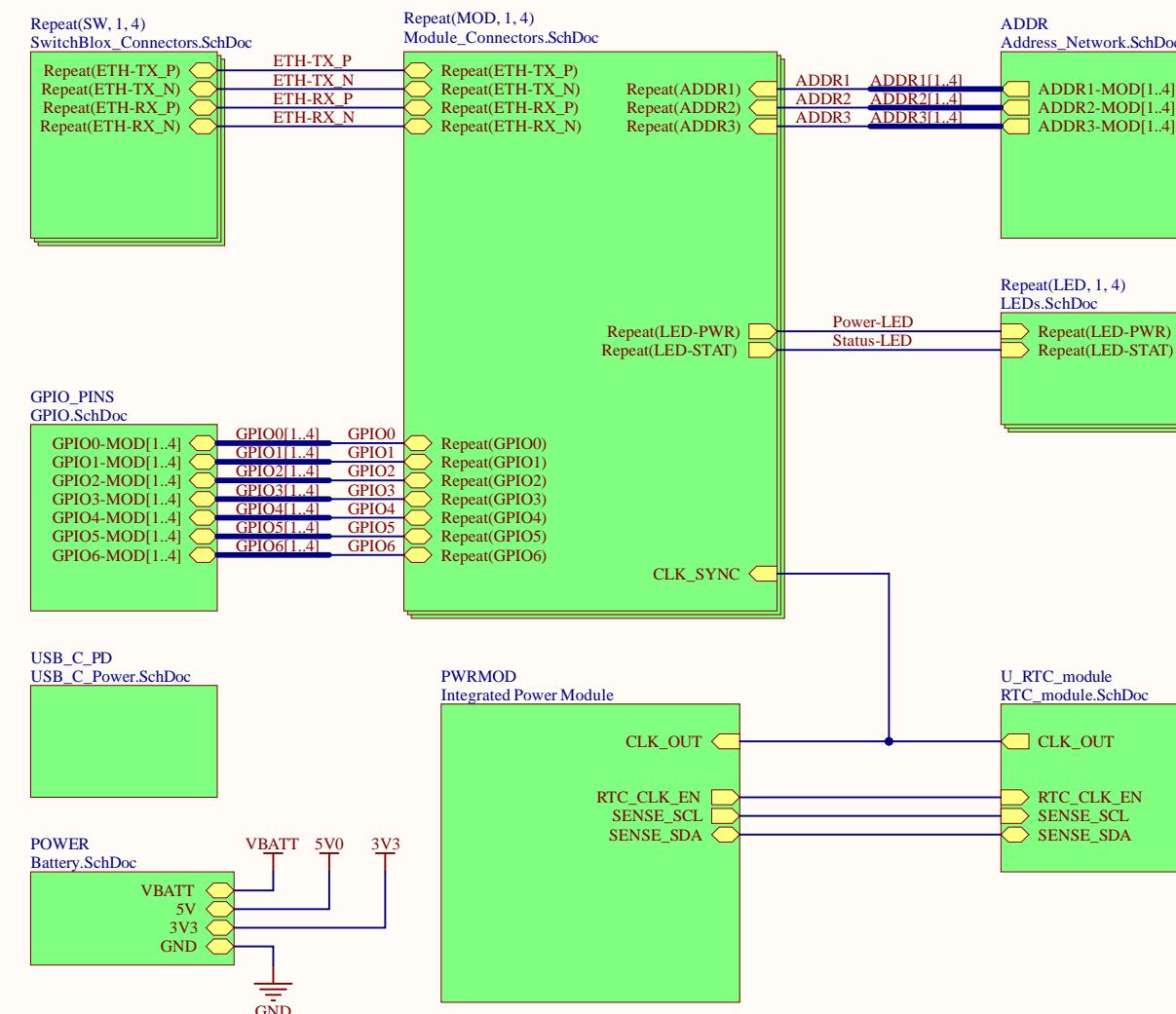


A  
TODO:  
VDD-3V3 Net changed in power mod, possible conflict with backplane hierarchy?



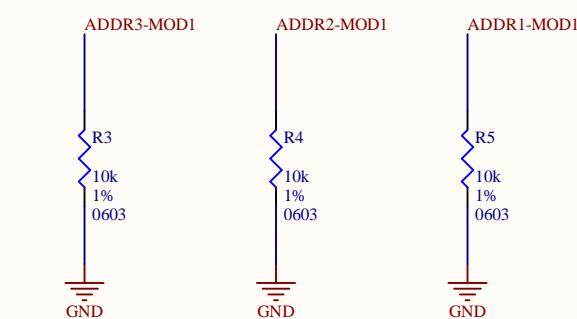
### MOD1-3 Mounting Holes

MH5	SMTSO3060CTJ
MH6	SMTSO3060CTJ
MH7	SMTSO3060CTJ
MH8	SMTSO3060CTJ

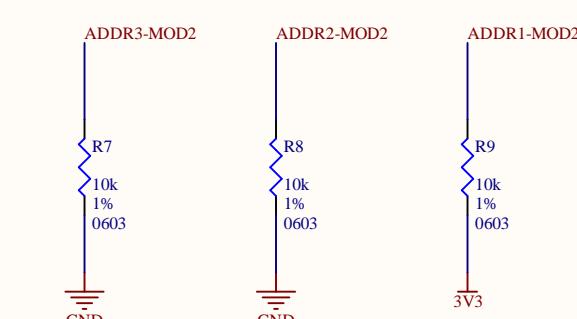
### MOD2-4 Mounting Holes

MH9	SMTSO3060CTJ
MH10	SMTSO3060CTJ
MH11	SMTSO3060CTJ
MH12	SMTSO3060CTJ

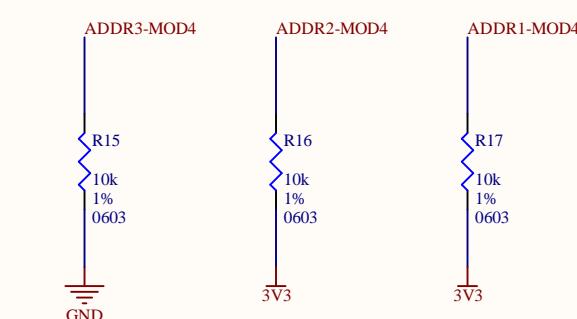
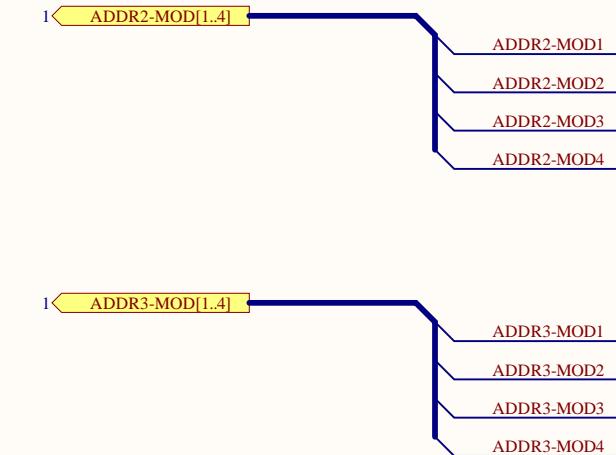
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B

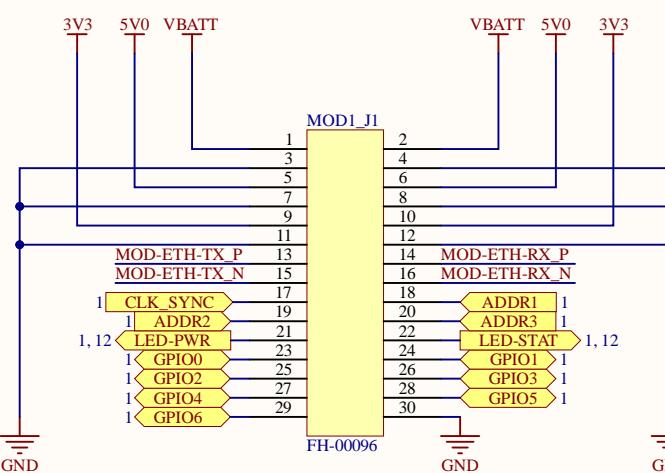


C

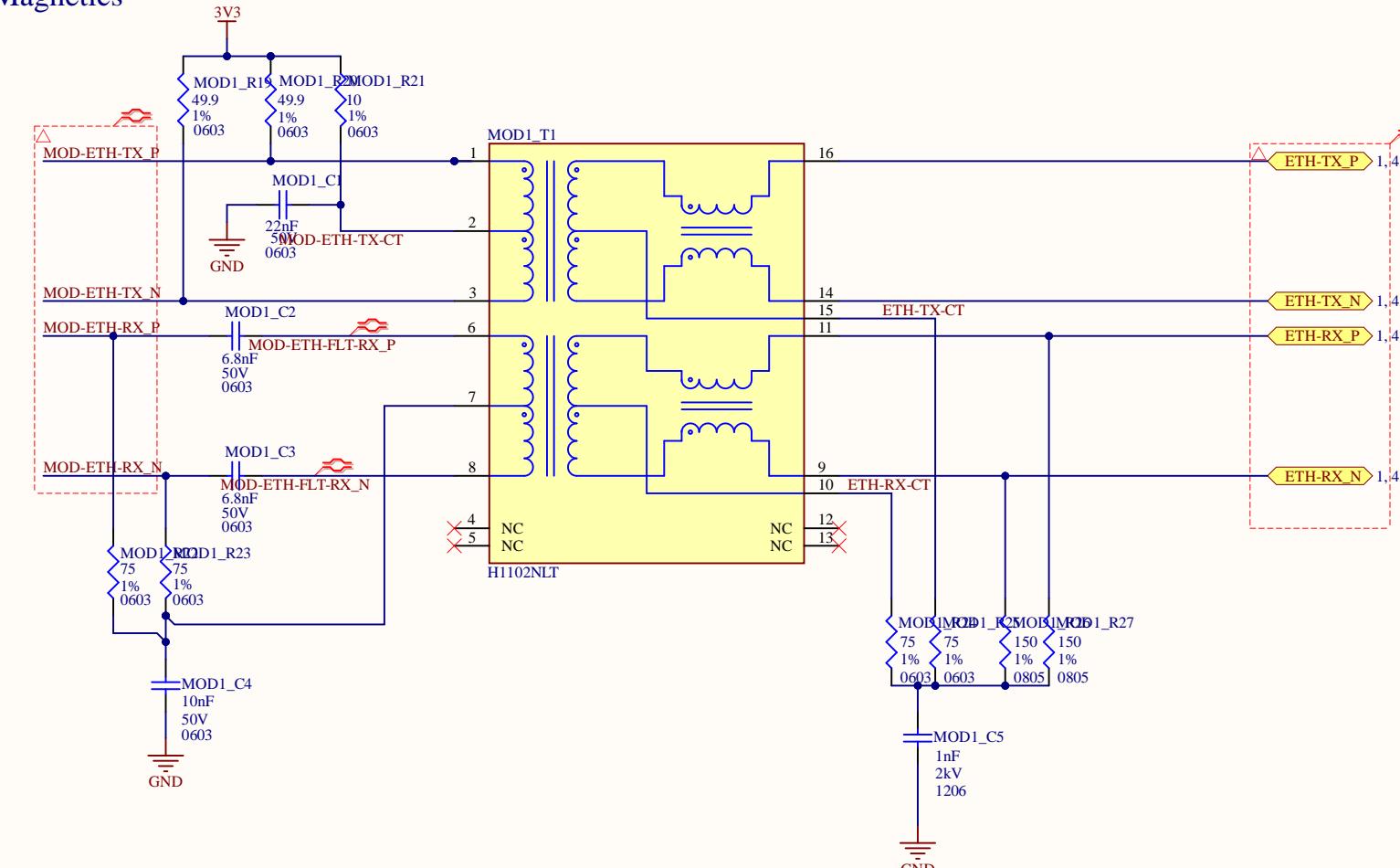


## Module Connector

Description	PIN#	Description
Battery Voltage	1	2
GND	3	4
5v	5	6
GND	7	8
3v3	9	10
GND	11	12
TX+	13	14
TX-	15	16
Clock Sync	17	18
ADDR 2	19	20
Power LED	21	22
GPIO 0	23	24
GPIO 2	25	26
GPIO 4	27	28
GPIO 6	29	30
GPIO 7		

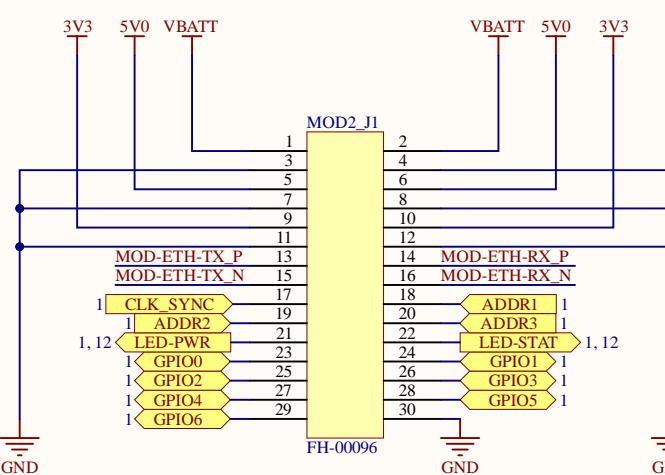


## Ethernet Magnetics

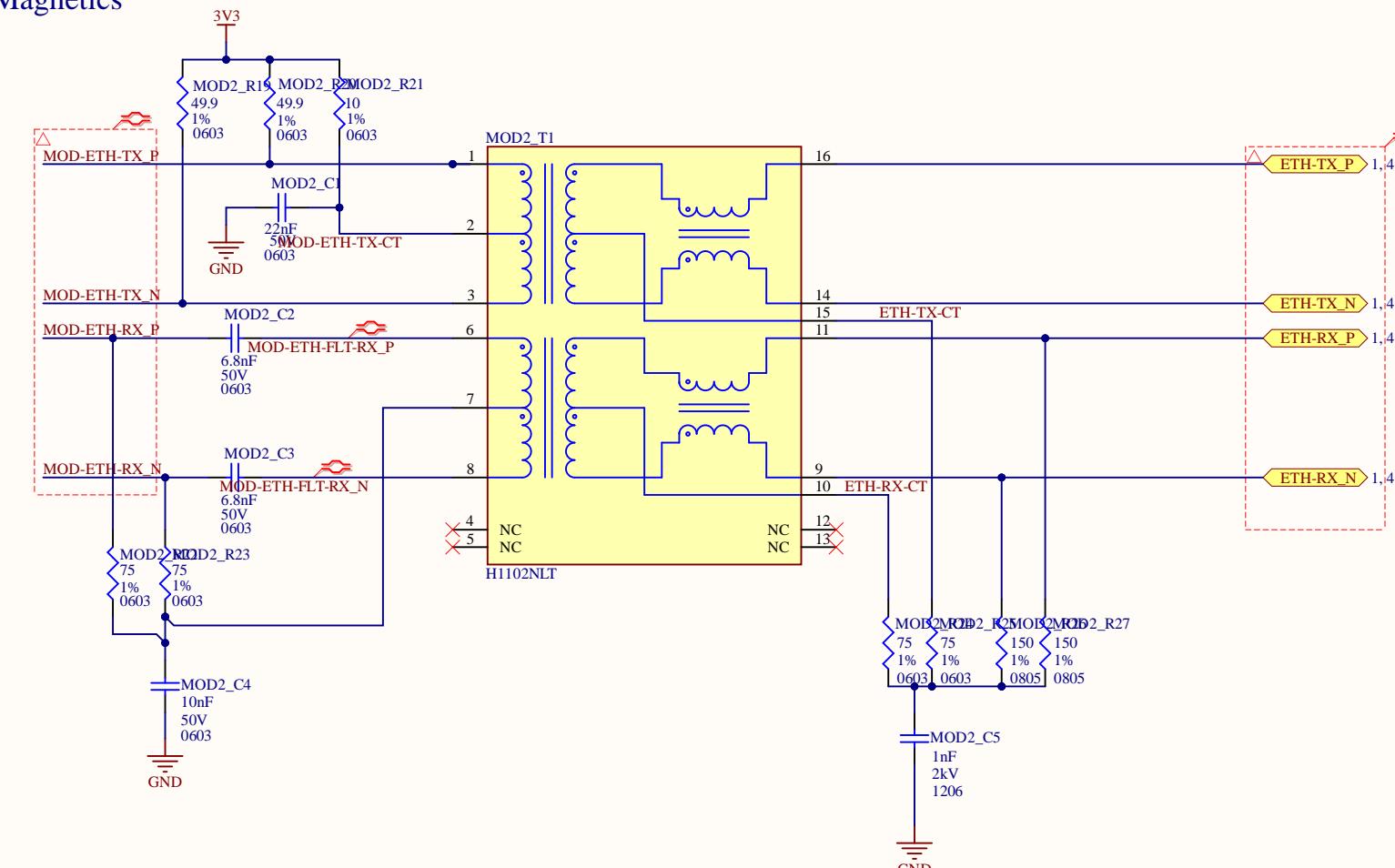


### Module Connector

Description	PIN#	Description
Battery Voltage	1	2
GND	3	4
5v	5	6
GND	7	8
3v3	9	10
GND	11	12
TX+	13	14
TX-	15	16
Clock Sync	17	18
ADDR 2	19	20
Power LED	21	22
GPIO 0	23	24
GPIO 2	25	26
GPIO 4	27	28
GPIO 6	29	30
GPIO 7		

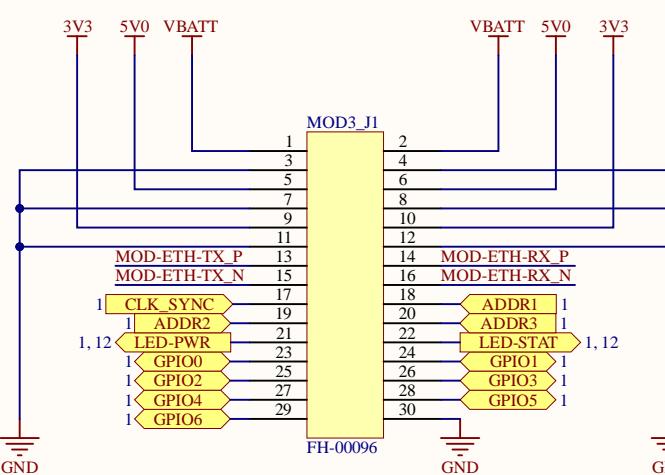


### Ethernet Magnetics

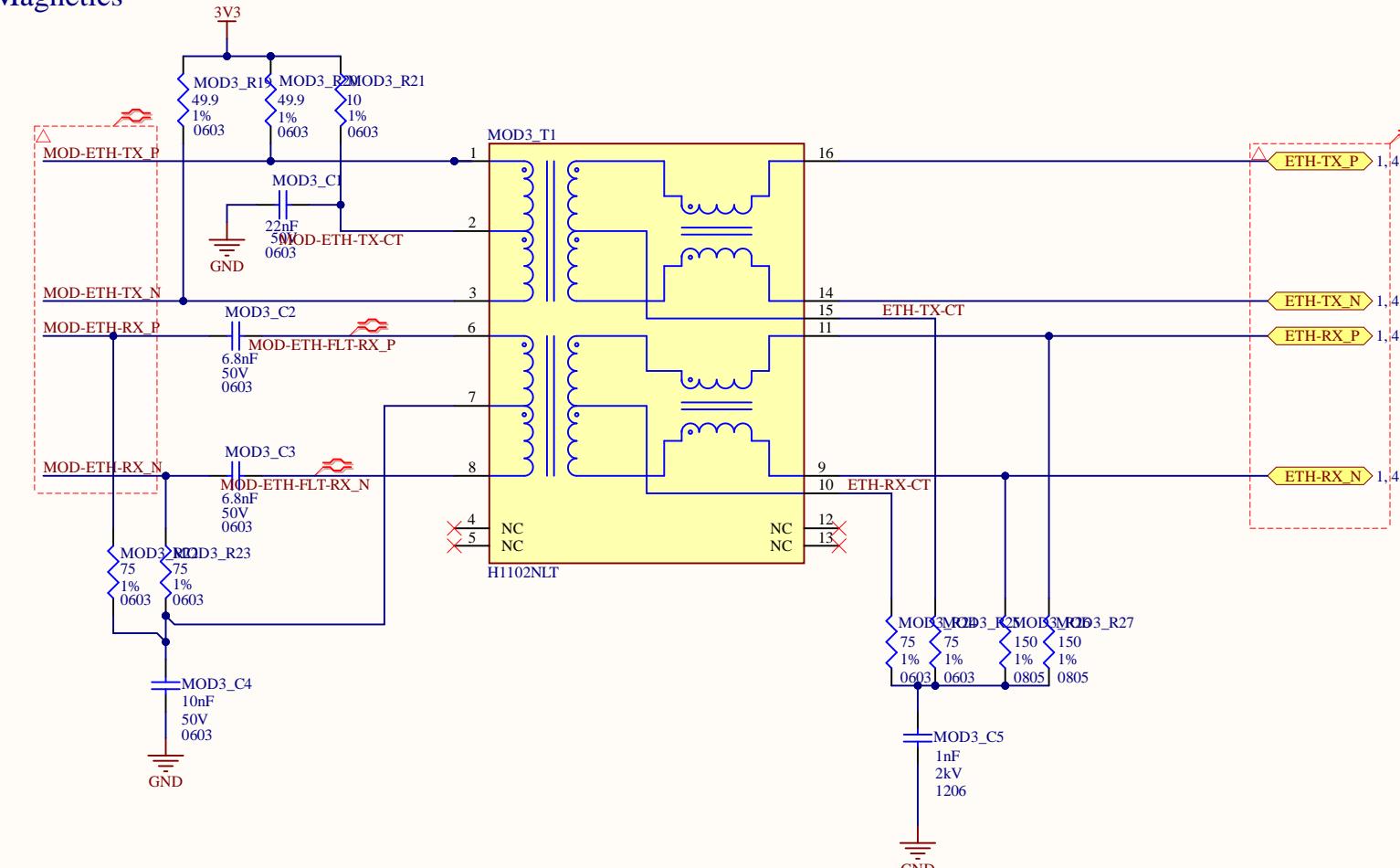


## Module Connector

Description	PIN#	Description
Battery Voltage	1	2
GND	3	4
5v	5	6
GND	7	8
3v3	9	10
GND	11	12
TX+	13	14
TX-	15	16
Clock Sync	17	18
ADDR 2	19	20
Power LED	21	22
GPIO 0	23	24
GPIO 2	25	26
GPIO 4	27	28
GPIO 6	29	30
GPIO 7		

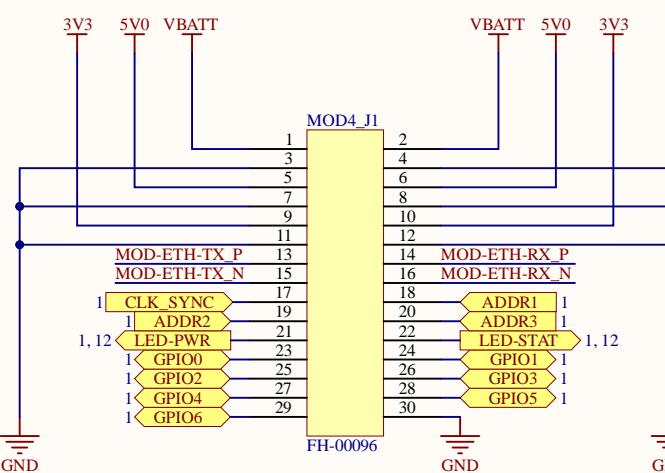


## Ethernet Magnetics

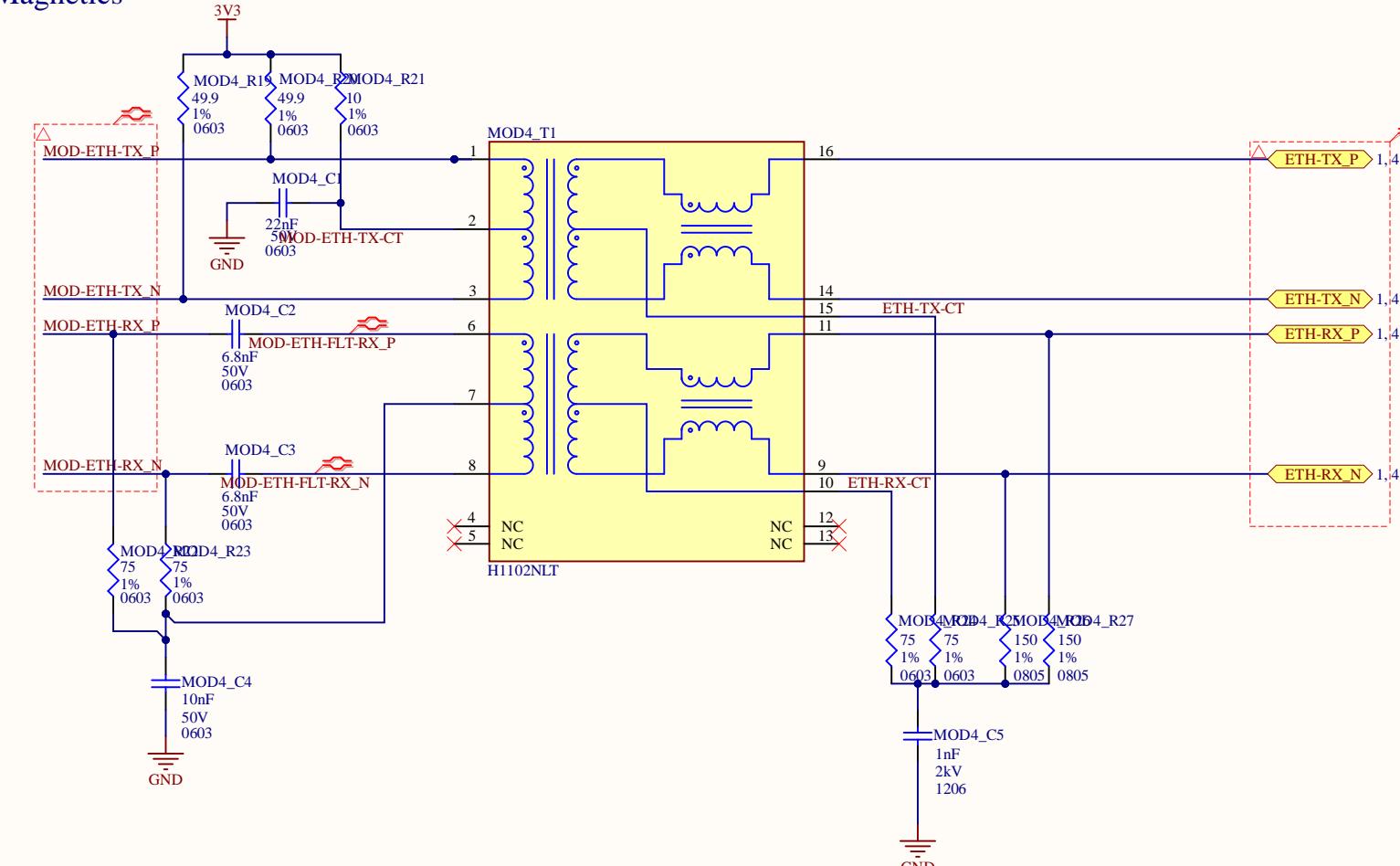


### Module Connector

Description	PIN#	Description
Battery Voltage	1	2
GND	3	4
5v	5	6
GND	7	8
3v3	9	10
GND	11	12
TX+	13	14
TX-	15	16
Clock Sync	17	18
ADDR 2	19	20
Power LED	21	22
GPIO 0	23	24
GPIO 2	25	26
GPIO 4	27	28
GPIO 6	29	30
GPIO 7		

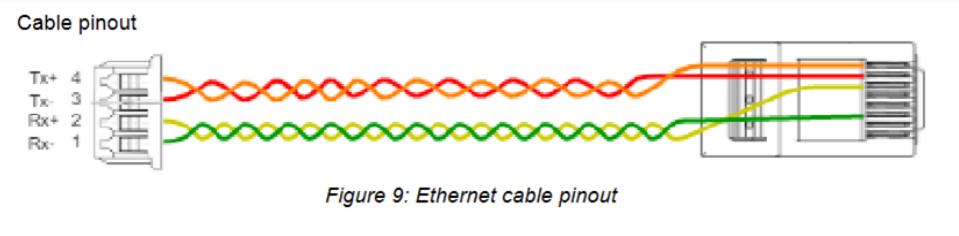
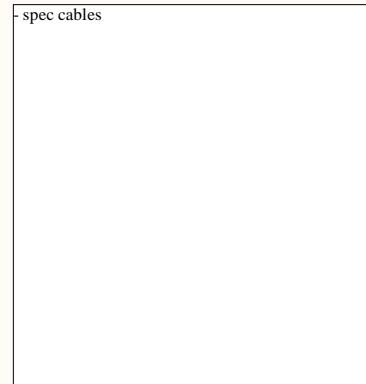


### Ethernet Magnetics

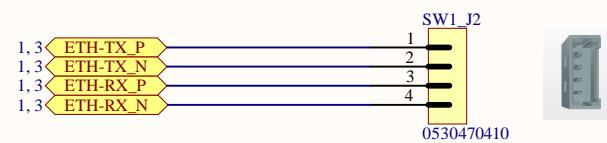


A

A

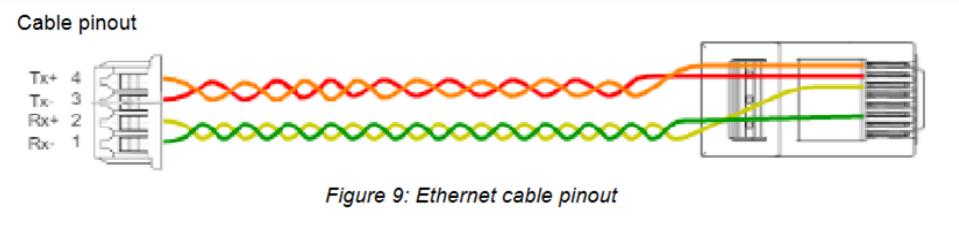
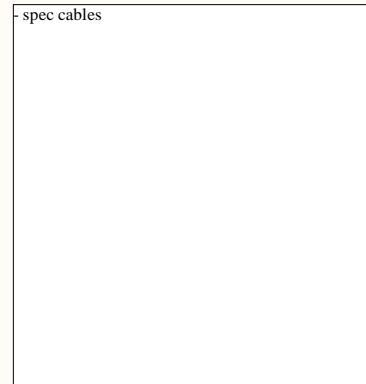
*Figure 9: Ethernet cable pinout*

Ethernet net names are from the perspective of the modules.  
The Switchblox supports Auto-MDIX crossover so it is okay that TX goes to TX and RX to RX  
Pinout is flipped as the cables cross over signals

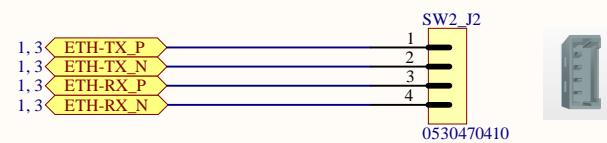


A

A

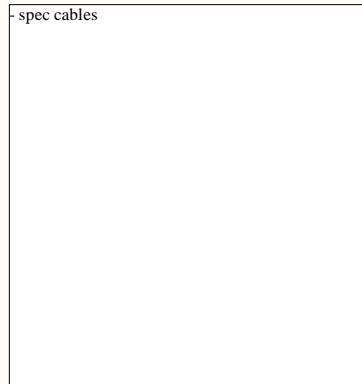
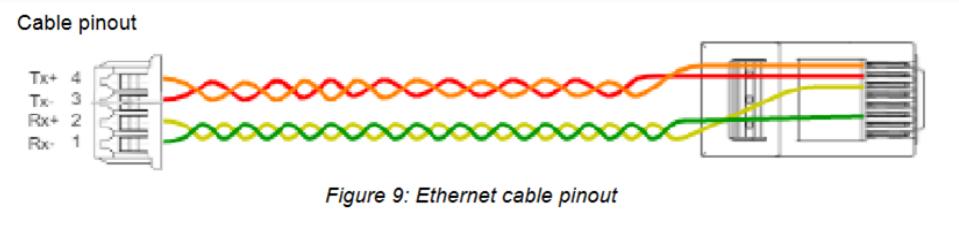
*Figure 9: Ethernet cable pinout*

Ethernet net names are from the perspective of the modules.  
The Switchblox supports Auto-MDIX crossover so it is okay that TX goes to TX and RX to RX  
Pinout is flipped as the cables cross over signals

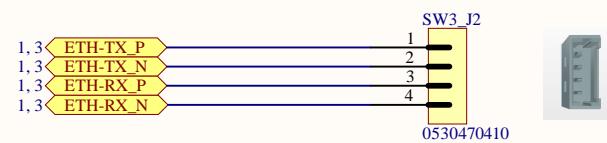


A

A



Ethernet net names are from the perspective of the modules.  
The Switchblox supports Auto-MDIX crossover so it is okay that TX goes to TX and RX to RX  
Pinout is flipped as the cables cross over signals



B

B

C

C

D

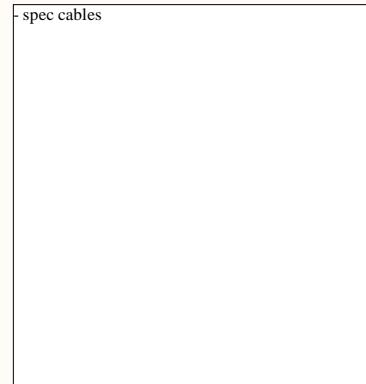
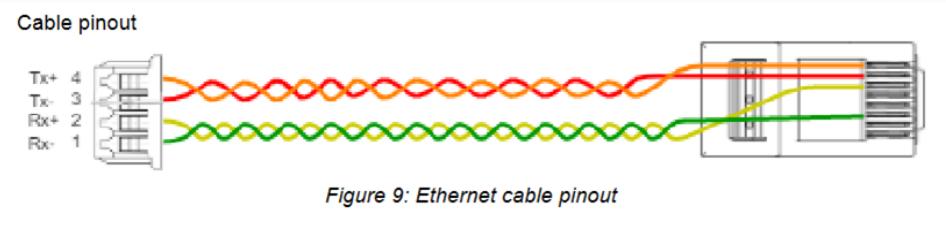
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SHEET NAME: SwitchBlox_Connectors.SchDoc	PROJECT: BLTPLANE_v1.0.PrjPcb
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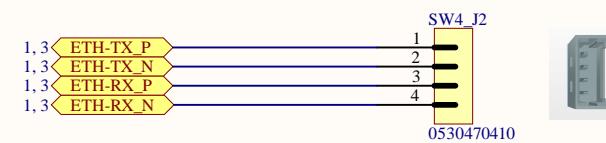
ENGINEER: *	DATE: 10/1/2025
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A

A



Ethernet net names are from the perspective of the modules.  
The Switchblox supports Auto-MDIX crossover so it is okay that TX goes to TX and RX to RX  
Pinout is flipped as the cables cross over signals



B

B

C

C

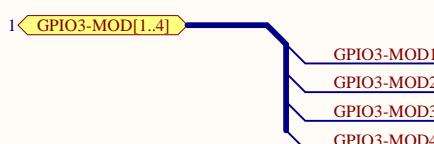
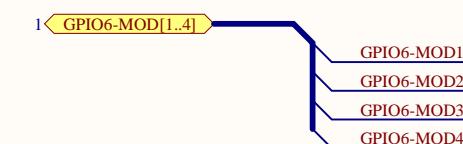
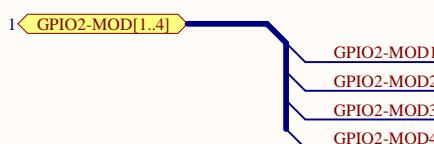
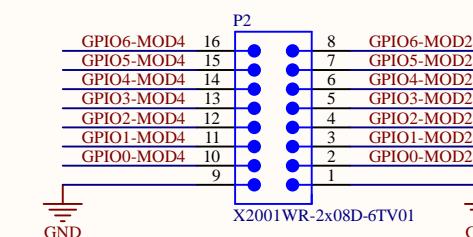
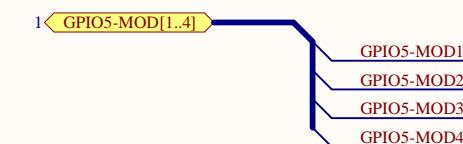
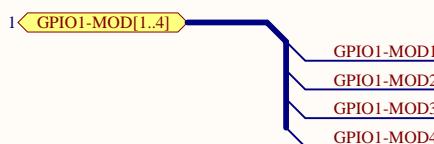
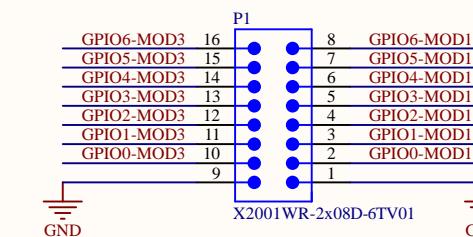
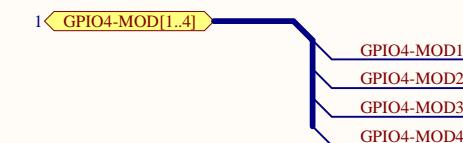
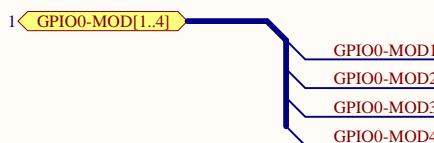
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D

SHEET NAME: SwitchBlox_Connectors.SchDoc	PROJECT: BLTPLANE_v1.0.PrjPcb
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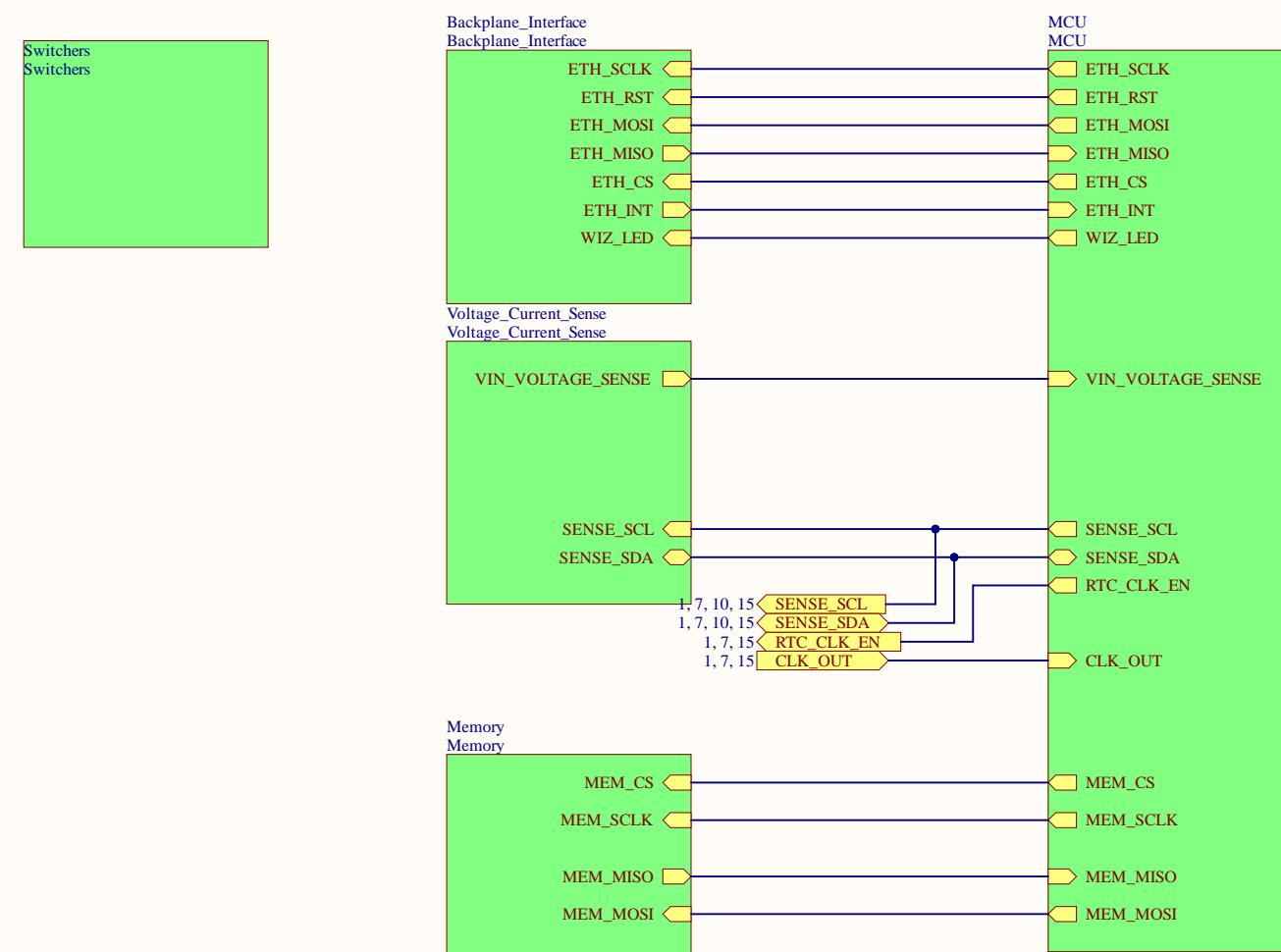
ENGINEER: *	DATE: 10/1/2025
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A



A

A



B

B

C

C

D

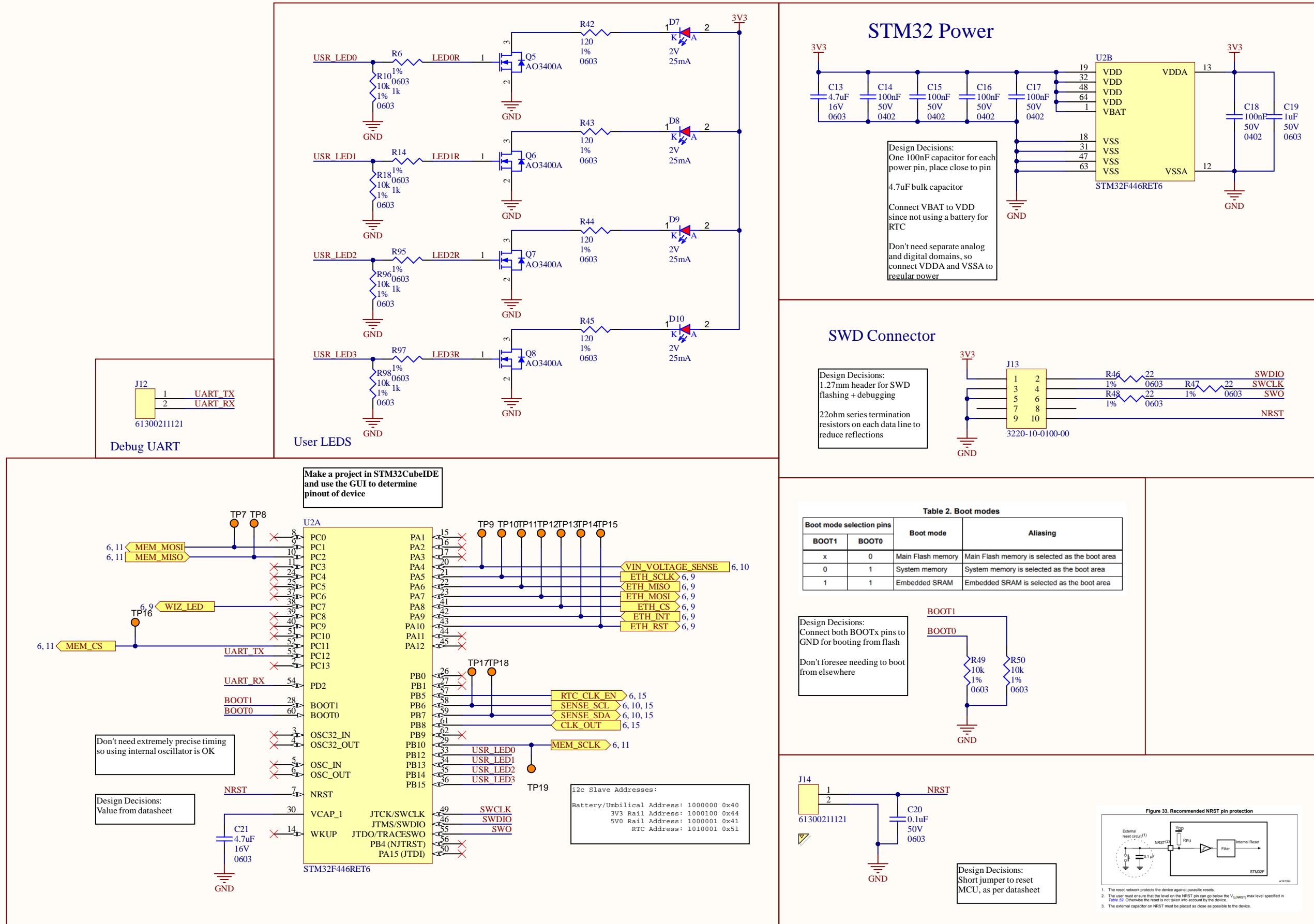
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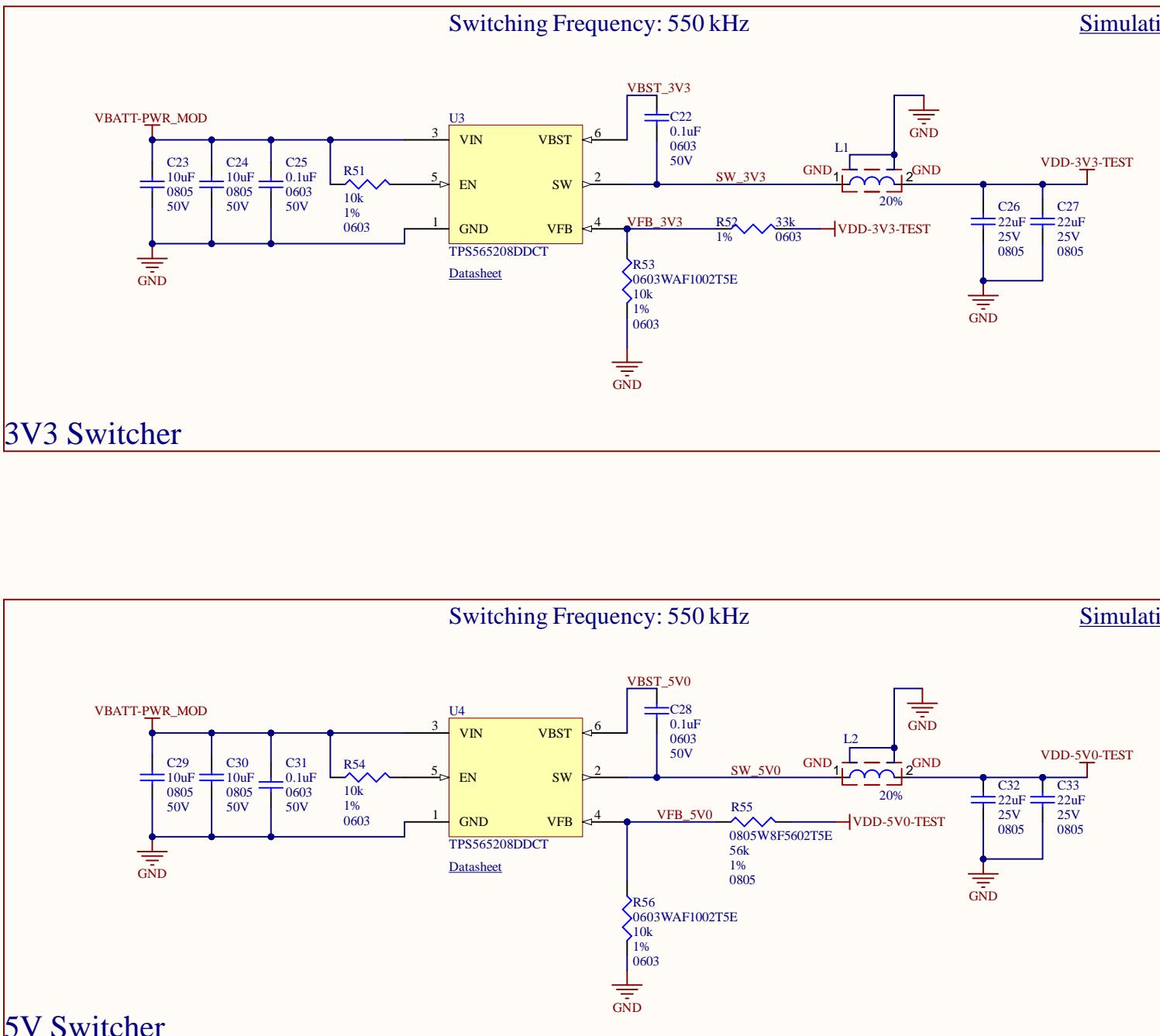
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ENGINEER: \* DATE: 10/1/2025



RIT LAUNCH INITIATIVE

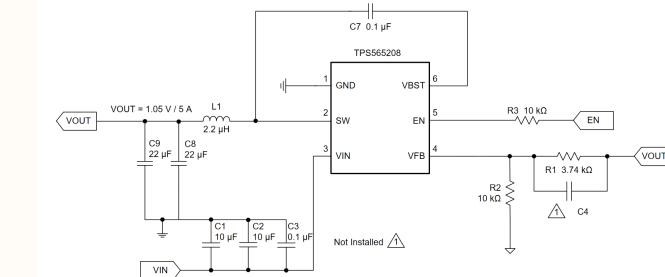




- 5-A Maximum Output Current
- Integrated 31-mΩ and 16-mΩ FETs
- D-CAP2™ Mode Control with Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Continuous Current Mode
- 500-kHz Switching Frequency
- Low Shutdown Current of Less than 1 µA
- 1% Feedback Voltage Accuracy
- Startup from Pre-biased Output Voltage
- Cycle-by-Cycle Current Limit
- Hiccup-mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms

#### 8.2 Typical Application

The application schematic in Figure 14 shows the TPS565208 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 5-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.



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Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1	2.2	4.7	20 to 68
1.05	3.74	10.0	1	2.2	4.7	20 to 68
1.2	5.76	10.0	1	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

SHEET NAME: Switchers.SchDoc

PROJECT: BLTPLANE\_v1.0.PnjPcb

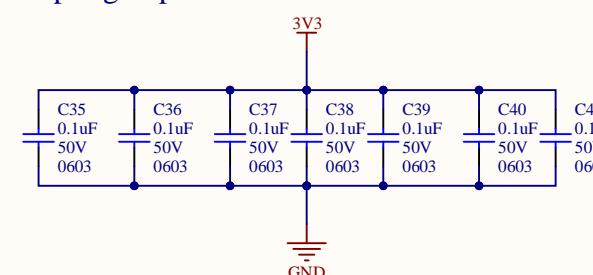
ENGINEER: \*

DATE: 10/1/2025

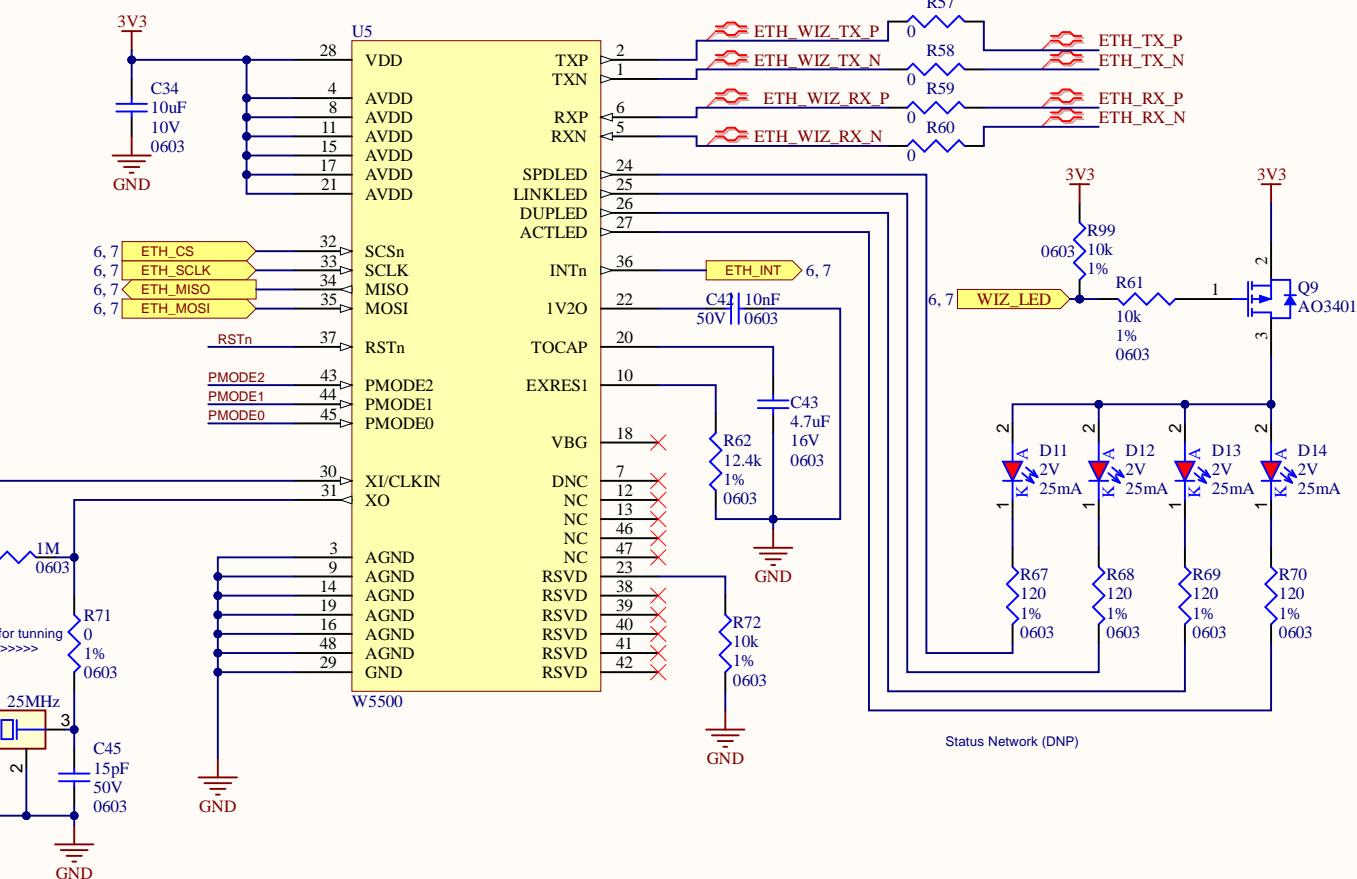


RIT LAUNCH INITIATIVE

### Decoupling Caps

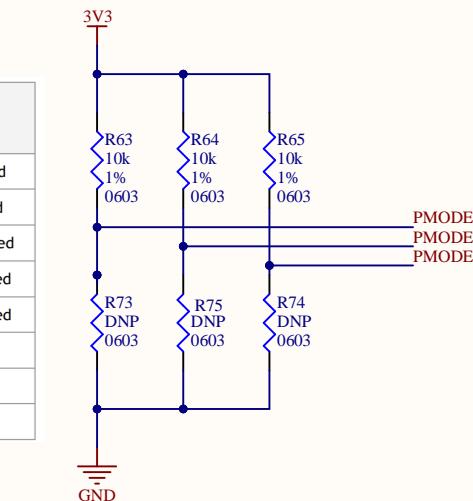


### WizNet 5500

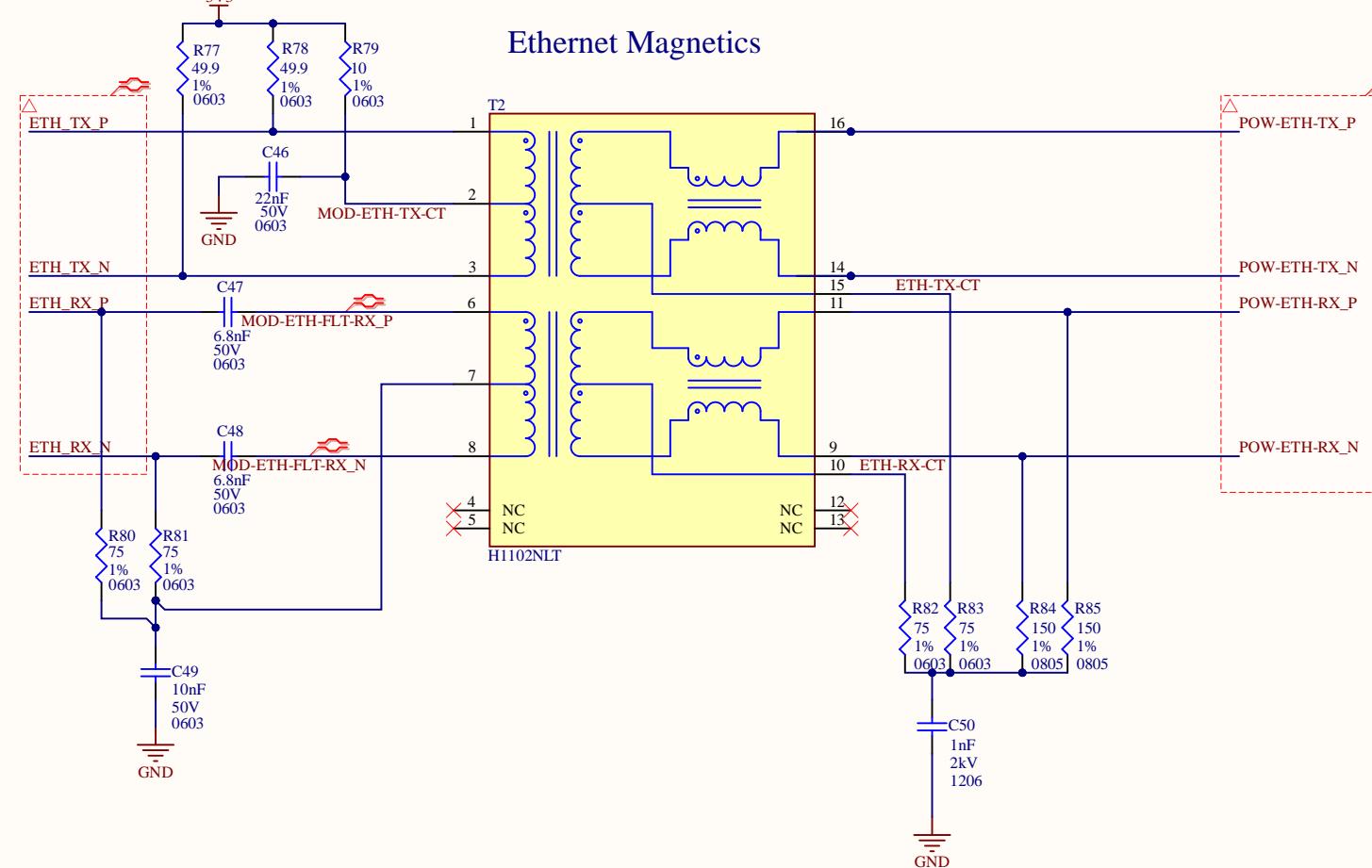


### PMODE Select

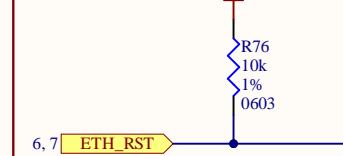
PMODE [2:0]			Description
2	1	0	10BT Half-duplex, Auto-negotiation disabled
0	0	1	10BT Full-duplex, Auto-negotiation disabled
0	1	0	100BT Half-duplex, Auto-negotiation disabled
0	1	1	100BT Full-duplex, Auto-negotiation disabled
1	0	0	100BT Half-duplex, Auto-negotiation enabled
1	0	1	Not used
1	1	0	Not used
1	1	1	All capable, Auto-negotiation enabled



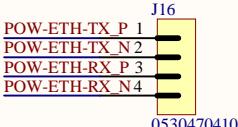
### Ethernet Magnetics



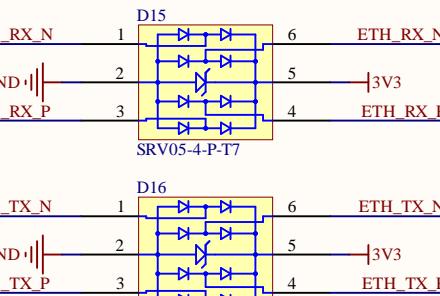
### RESET



### JST Connector for Power Mod



### ESD Protection



SHEET NAME: Backplane\_Interface.SchDoc PROJECT: BLTPLANE\_v1.0.PjPcb

ENGINEER: \* DATE: 10/1/2025

RIT LAUNCH INITIATIVE

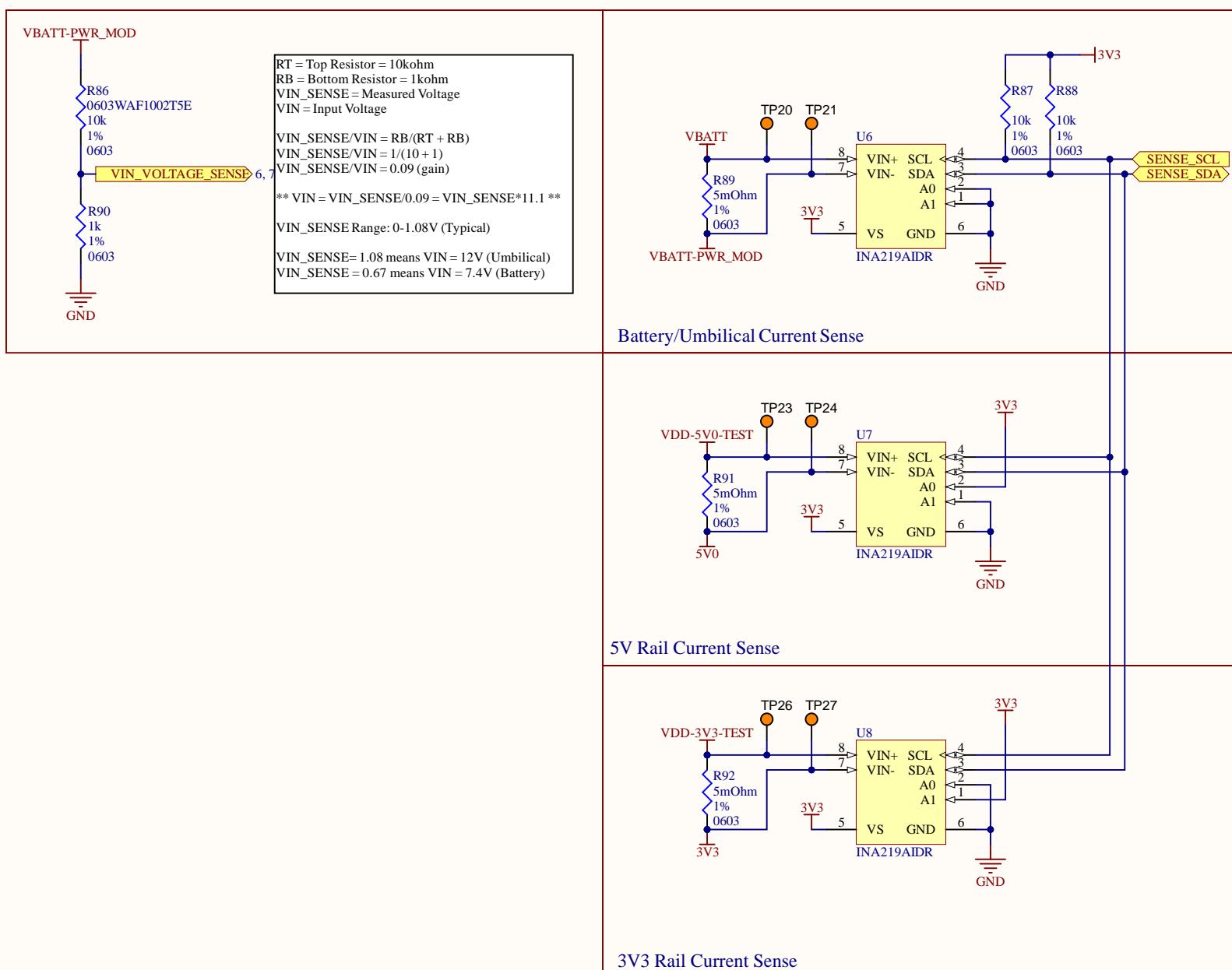


Table 1. INA219 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V <sub>S+</sub>	1000001
GND	SDA	1000010
GND	SCL	1000011
V <sub>S+</sub>	GND	1000100
V <sub>S+</sub>	V <sub>S+</sub>	1000101
V <sub>S+</sub>	SDA	1000110
V <sub>S+</sub>	SCL	1000111
SDA	GND	1001000
SDA	V <sub>S+</sub>	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V <sub>S+</sub>	1001101
SCL	SDA	1001110
SCL	SCL	1001111

i2c Slave Addresses:  
 Battery/Umbilical Address: 1000000 0x40  
 3V3 Rail Address: 1000100 0x44  
 5V0 Rail Address: 1000001 0x41  
 RTC Address: 1010001 0x51

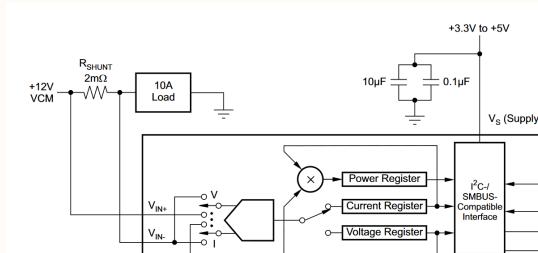


Figure 29. Example Circuit Configuration

SHEET NAME: Voltage\_Current\_Sense.SchDoc PROJECT: BLTPLANE\_v1.0.PrjPcb

ENGINEER: \* DATE: 10/1/2025



RIT LAUNCH INITIATIVE

A

A

B

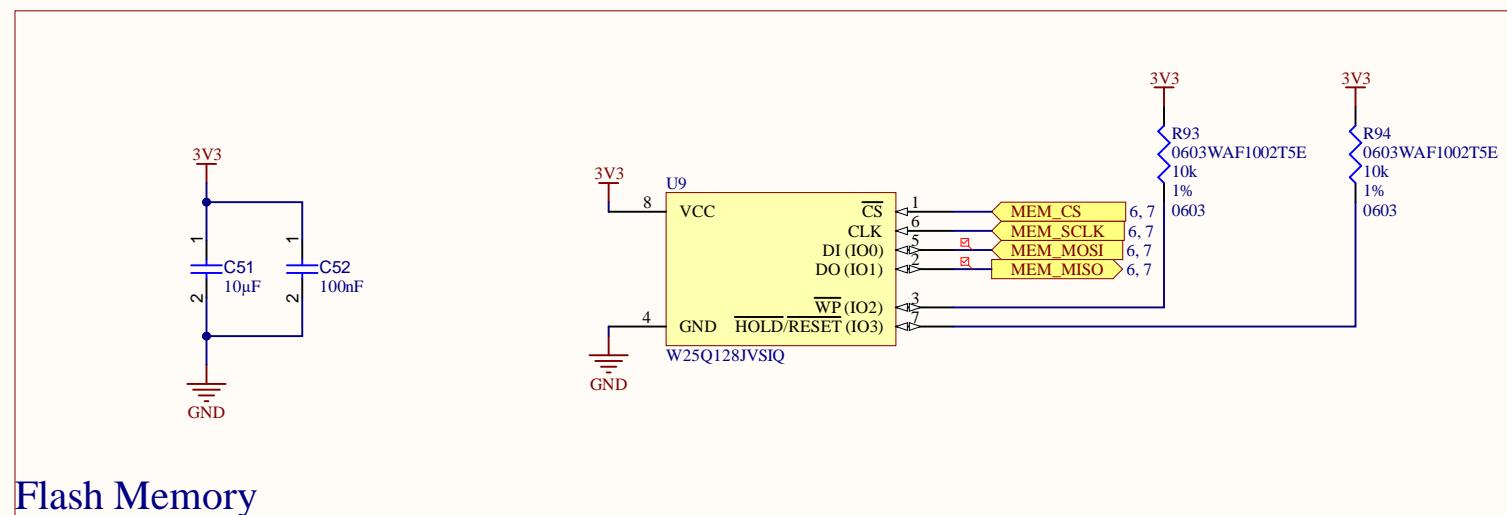
B

C

C

D

D



Flash Memory

SHEET NAME: Memory.SchDoc	PROJECT: BLTPLANE_v1.0.PrjPcb
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ENGINEER: *	DATE: 10/1/2025
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RIT LAUNCH INITIATIVE

A

A

B

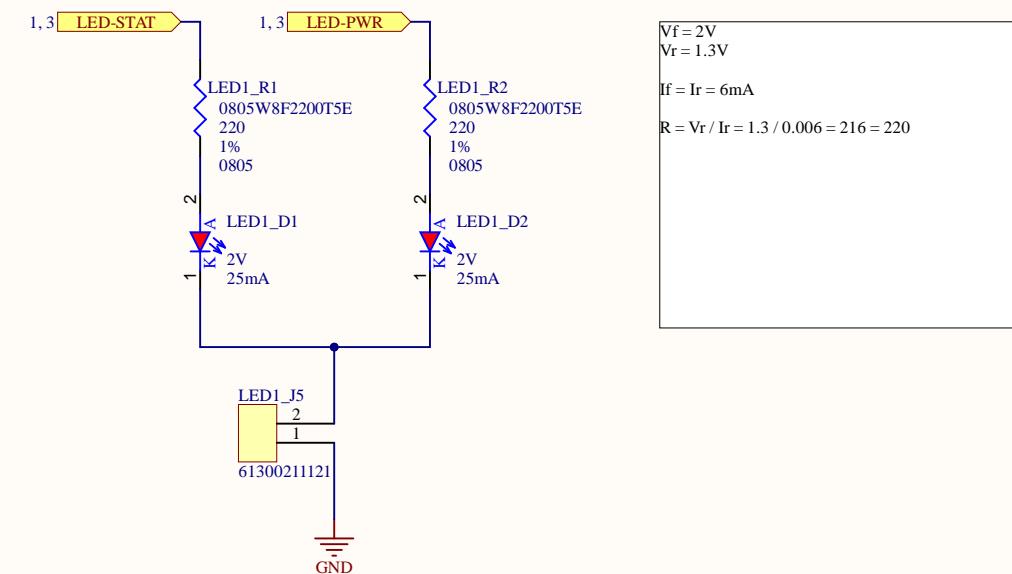
B

C

C

D

D



A

A

B

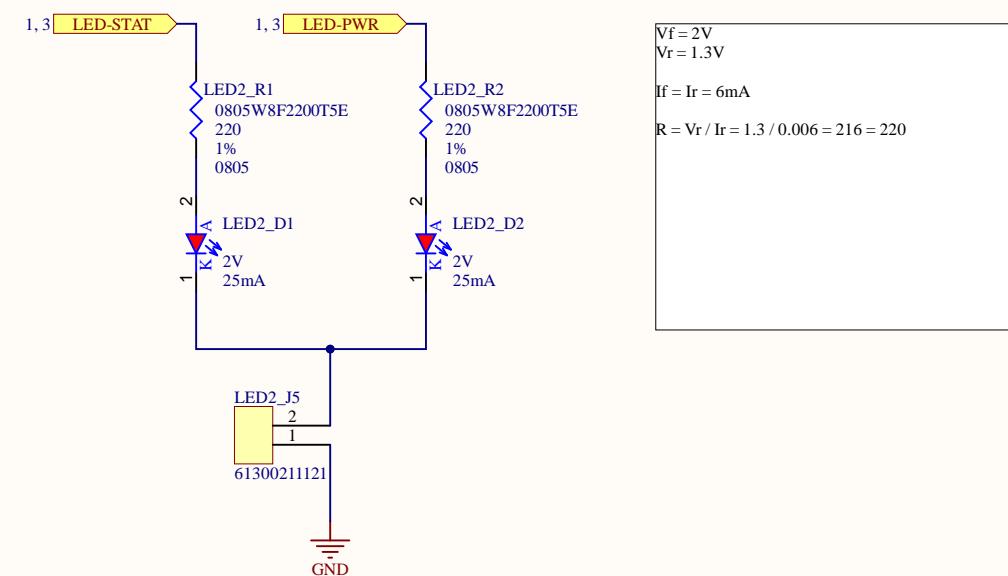
B

C

C

D

D



SHEET NAME: LEDs.SchDoc	PROJECT: BLTPANE_v1.0.PrjPcb
ENGINEER: *	DATE: 10/1/2025
 RIT LAUNCH INITIATIVE	

A

A

B

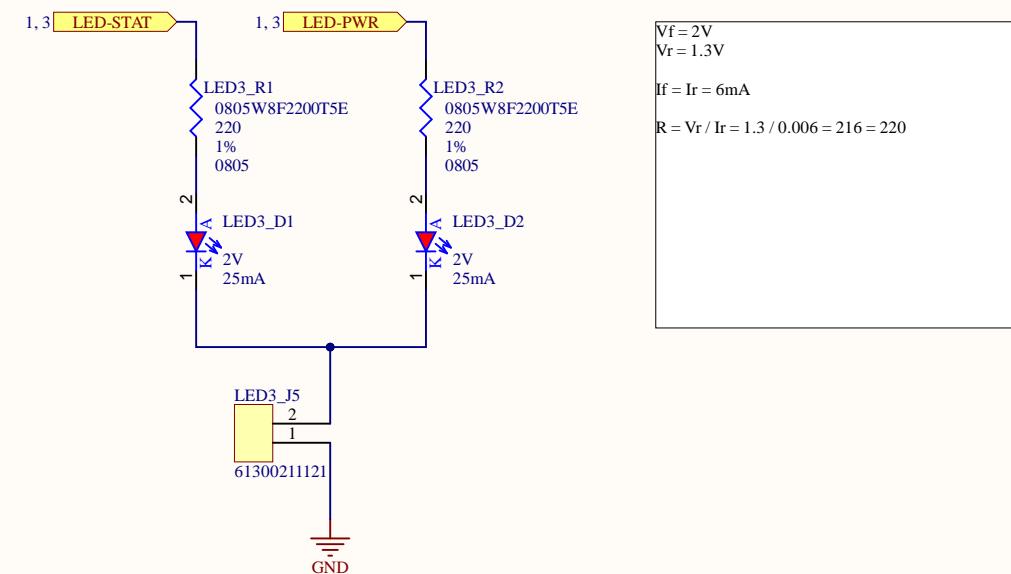
B

C

C

D

D



A

A

B

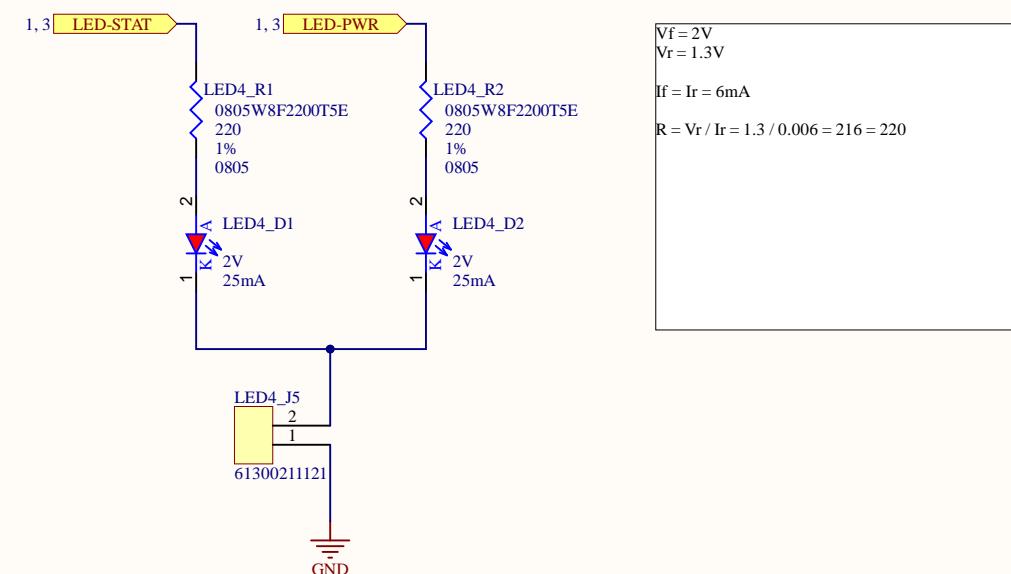
B

C

C

D

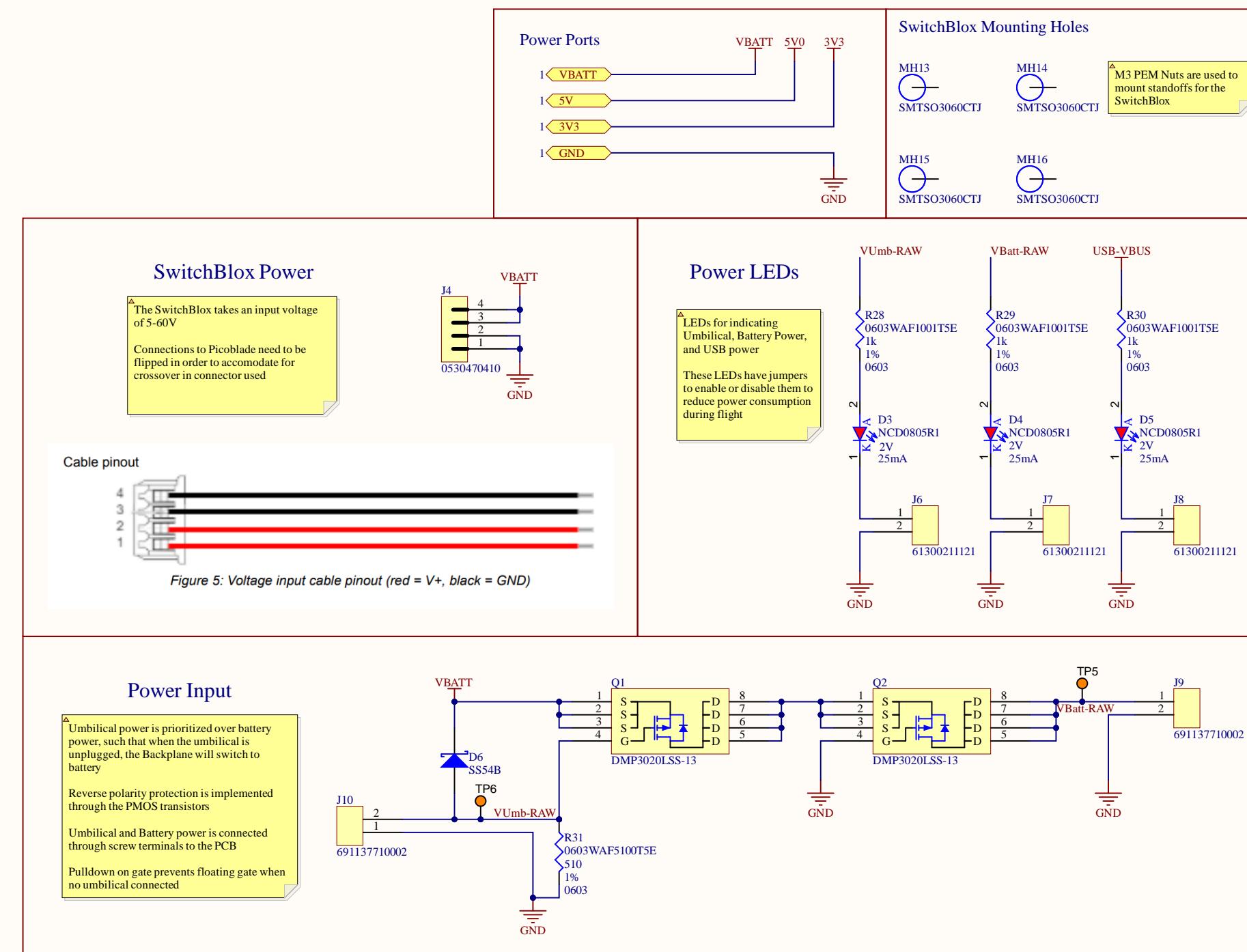
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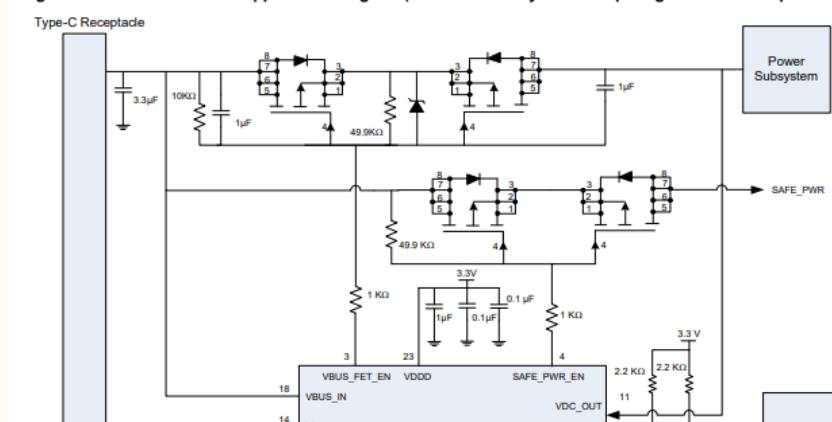
SHEET NAME: LEDs.SchDoc	PROJECT: BLTPLANE_v1.0.PrjPcb
ENGINEER: *	DATE: 10/1/2025
 RIT LAUNCH INITIATIVE	

A

A



**Figure 3. EZ-PD BCR based Application Diagram (for Electronic Systems Requiring 12 V to 15 V Input at 2 A)**



**Table 2. Resistor Divider Values for Minimum or Maximum Voltage Requested on V<sub>out</sub>**

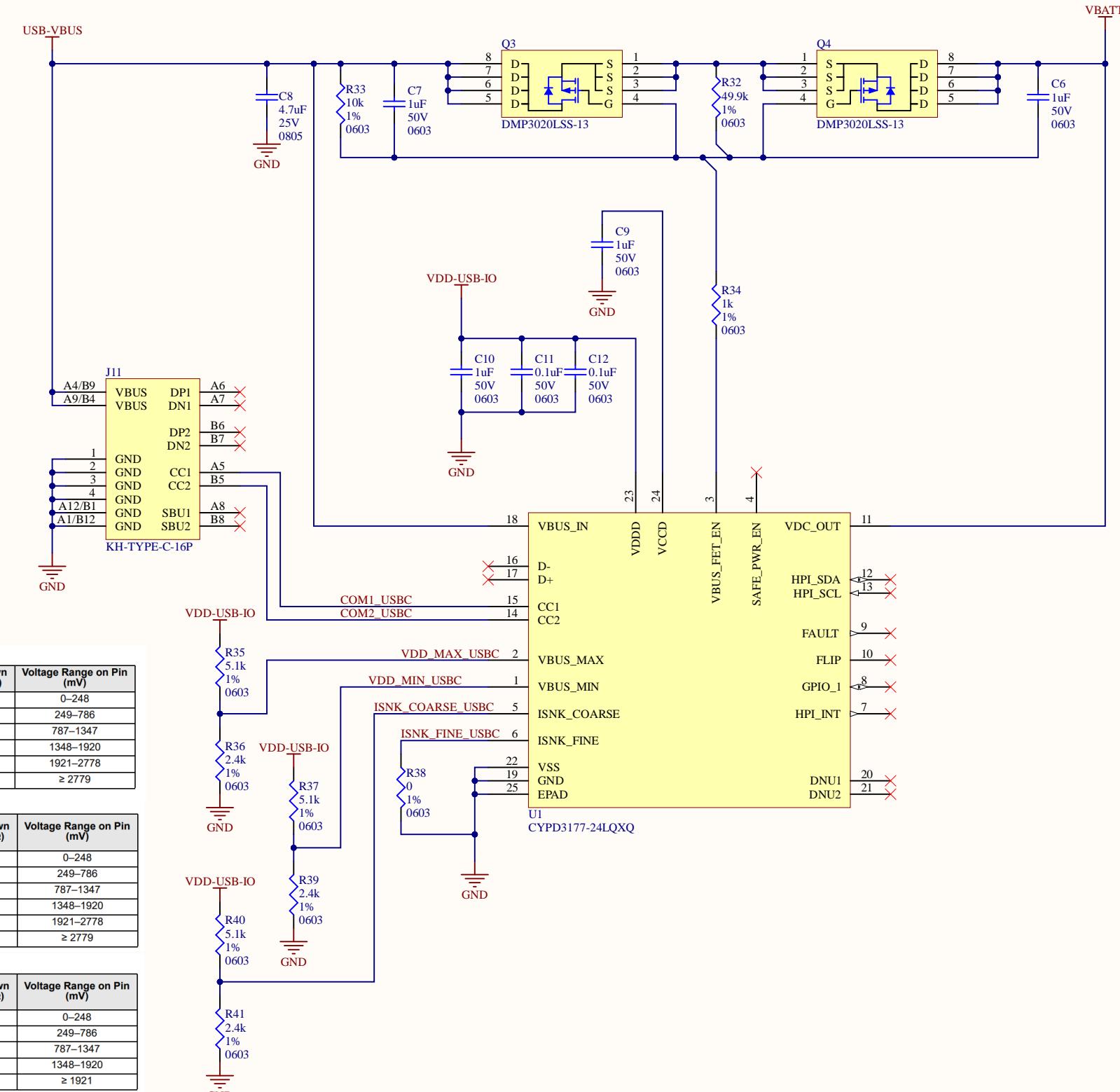
Voltage Requested (V)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor value (kΩ)	Suggested Pull-down Resistor value (kΩ)	Voltage Range on (mV)
5	0/6	Open	0	0–248
9	1/6	5.1	1	249–786
12	2/6	5.1	2.4	787–1347
15	3/6	5.1	5.1	1348–1920
19	4/6	5.1	10	1921–2778
20	> 5/6	0	Open	> 2770

Table 3. Resistor Divider Values for Coarse Setting on Operating Current (For VDD = 1.8V)

Table 3. Resistor Divider Values for Coarse Setting on Operating Current (For VDDD = 3.3 V)				
Operating Current Requested for Coarse Setting (A)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor Value (kΩ)	Suggested Pull-down Resistor Value (kΩ)	Voltage Range on (mV)
0	0/6	Open	0	0–248
1	1/6	5.1	1	249–786
2	2/6	5.1	2.4	787–1347
3	3/6	5.1	5.1	1348–1926
4	4/6	5.1	10	1921–2778
5	≥ 5/6	0	Open	≥ 2779

Table 4. Resistor Divider Values for Fine Setting on Operating Current (For VDDD =

Table 4. Resistor Divider Values for Fine Setting on Operating Current (For VDDD = 3.3 V)				
Operating Current Requested for Fine Setting (A)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor Value (kΩ)	Suggested Pull-down Resistor Value (kΩ)	Voltage Range on (mV)
+0	0/6	Open	0	0–248
+250	1/6	5.1	1	249–786
+500	2/6	5.1	2.4	787–1347
+750	3/6	5.1	5.1	1348–1920
+900	≥ 4/6	0	Open	≥ 1921



A

A

B

B

C

C

D

D

