Section 1 Professor

Richard Cliver

ENT-2156
rcceee@rit.edu

Section 2 Course

Description

This course covers the specification, analysis, modeling and design of digital systems. Standard modules, such as decoders, multiplexers, shifter registers, adders, and counters, will be analyzed. Lectures will discuss fundamental design methodologies, state machines and digital system modeling with the use of VHDL as a hardware description language. The laboratory provides hands-on experiences of the design, modeling, implementation, and testing of digital systems using commercial IC components as well as CAD tools.

Suggested Text

1. For the first 10 weeks of the course I recommend Fundamentals of Logic Design by Charles H. Roth. The definitions and methods presented in the book are used in class. Any edition is fine.
2. Fundamentals of Digital Logic with VHDL Design by Brown is an excellent text. I use some of the material from this text in class because Brown does a great job. The book includes a lot of examples in VHDL which can be very helpful in the last 5 weeks of class. Any edition is fine and an older edition book is available in the library.
3. In the last 5 weeks of class we discuss VHDL. If you google "Peter J. Ashenden VHDL tutorial" you will find several good books on VHDL. Peter Ashenden is one of my favorite VHDL authors.
4. Lastly, Digital Design and Computer Architecture, 2nd Edition, by David and Sarah Harris is an excellent reference for all topics covered in DSD 1 (and DSD 2 as well).

Section 3 Course Learning Outcomes

Comprehension

1. Understand the different types of digital systems, (i.e., combinational versus sequential circuits).
2. Learn the different digital components that build digital systems and how to use them.
3. Learn Boolean algebra and different numbering systems along with corresponding binary arithmetic operations.
4. Understand the concepts of hardware description languages and modeling of digital systems with concurrent and sequential statements.

Application

1. Use Boolean algebra, state diagram, truth/state table, and circuit diagram to represent a digital system.
2. Implement binary arithmetic operations using digital circuits.
3. Design digital circuits using various digital design techniques, (e.g., Karnaugh maps, state diagrams, etc.)

4. Implement and validate simple digital circuits using various building components, (e.g., AOI gates, decoders, multiplexers, shift-registers, etc.)
5. – Using different methods and styles apply correct VHDL code to model and simulate combinational and sequential circuits.

Analysis

Analyze the functionality and the basic performance of digital circuits built.

Evaluation

Generate well-written laboratory reports that present quantitative data and qualitative discussion.

Section 4 Grading

Category	Percentage
Lab	40%
Homework	10%
Quizzes	10%
Term Exams	20%
Final	20%

Homework

Homework is due most weeks and collected in the course drop-box on Fridays. See due dates in the Assignment drop-box. Please box answers and show a reasonable level of work. Solutions are posted prior to term exams. Exams will cover homework material.

Quizzes

Quizzes will be given every class covering lecture material. Quizzes will be closed book and closed notes. NO equation sheet will be provided. TWO quiz will be dropped. No makeup quizzes.

Tests (1 and 2)

Two tests will be given during the semester. The first test will be ***Friday, February 18th*** and the second test will be ***Friday, March 25th***. Your highest test grade will count twice as shown in Equation 1 OR Equation 2.

$$TestAvg = \frac{2(Test_1) + Test_2}{3} \; when \; Test_1 > Test_2 \tag{1}$$

$$TestAvg = \frac{Test_1 + 2(Test_2)}{3} \; when \; Test_1 < Test_2 \tag{2}$$

You may bring one 8.5"x11" sheet with hand written equations for use during Test 1 and Test 2. The tests will be closed book. In case of an emergency a reasonable attempt must be made to contact me. Use e-mail or phone call. In these cases a make-up test can be scheduled but will not receive a grade greater than 70

Final

One sheet is permitted for the Final. The final will be a closed book exam. There will not be a make-up for the final.

Section 5 Policy

Academic integrity statement

All conduct in this course is governed by the KGCOE Academic Honesty Policy, RIT Honor Code (P03.0), and RIT Student Academic Integrity Policy (D08.0).

Academic adjustments statement

RIT is committed to providing academic adjustments to students with disabilities. If you would like to request academic adjustments such as testing modifications due to a disability, please contact the Disability Services Office (DSO). Contact information for the DSO and information about how to request adjustments can be found at `http://www.rit.edu/dso`. After you receive academic adjustment approval, it is imperative that you contact the instructor as early as possible to work out whatever arrangement is necessary.

Title IX statement

Title IX violations are taken very seriously at RIT. RIT is committed to investigate complaints of sexual discrimination, sexual harassment, sexual assault, and other sexual misconduct, and to ensure that appropriate action is taken to stop the behavior, prevent its recurrence, and remedy its effects. Title IX rights and resources at RIT can be found at `http://www.rit.edu/fa/compliance/content/title-ix`