Section 1 Professor

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Section 2 Course

Description

This class covers the analysis, design and testing of digital systems. The rapid growth of digital computers, control devices, instruments and communication equipment requires a basic knowledge and general methodology that can be adapted to rapidly evolving changes and constraints. The study of combinational and sequential systems considers the use of standard modules such as decoders, multiplexers, shifters, ROMs, PLAs, adders, registers and counters. An important component of this course is testing of Digital Systems. Digital ICs undergo rigorous testing before shipping from industry. In this course students will be introduced to state-of-the-art standards in testing methodologies. The laboratory provides more insight into implementation of digital systems through the creation of a MIPs processor using modern tools like Xilinx ISE and Mentor Graphics' ModelSim. The lab-intensive hands-on aspect of this course presents different approaches to the digital system modeling and design with the use of HDLs. The lab sessions include specification and design of combinational and sequential systems using VHDL and Verilog HDL. Industry-standard simulation and synthesis tools will be used during the term of the course, which will enable students gain hands-on experience.

Suggested Text

1. Fundamentals of Digital Logic with VHDL Design (3rd Edition) by Stephen Brown and Zvonko Vranesic, ISBN 978-0-07-352953-0

2. Digital Design and Computer Architecture (2nd Edition) by David and Sarah Harris, ISBN-13: 978-0123944245.

Section 3 Software

VHDL can be a very difficult language to debug and the tools don't always offer helpful error messages. At Kodak, I would use a lot of different packages when I needed help troubleshooting. We will use all three of the packages below in lab and in homework.

Vivado

On a Windows machine:

1. You will need to download Xilinx Vivado (2019.1)
2. `https://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html`.
3. Download and install Vivado HL WebPACK

For MAC and Linux: Install a VM or DualBoot. The following will help:

1. This is about using BootCamp (i.e. dual boot): `https://support.apple.com/en-us/HT201468`
2. This is more details about using VirtualBox: `https://osxdaily.com/2015/03/25/install-run-windows-10-mac-vi`

3. Virtual Box installation: `https://www.virtualbox.org/wiki/Downloads`
4. Access Windows image here: `http://homeuse.rit.edu/`

ModelSim

Mentor's ModelSim is an industry standard simulation package covered in DSD 1. This software is loaded on the lab computers and the DSD 2 lab appendix has a ModelSim tutorial.

EDAPlayground

This web based simulator allows to experiment with lots of industry standard simulators.

Section 4 Grading

Category	Percentage
Lab	30%
Lab Attendance	5%
Homework	10%
Quizzes	5%
Term Exams	25%
Final	25%

Homework

Homework will be assigned each week and collected on-line MyCourses drop-box the following Wednesday. Please box answers and show a reasonable level of work. Late homework is accepted but penalized 3 points per week.

Quizzes

Quizzes will be given most Fridays and cover the material from the previous week's homework. Quizzes will be closed book and closed notes. NO equation sheet will be provided. TWO quiz will be dropped. No makeup quizzes. In the week of a test or break, we will not have a quiz.

Tests (1 and 2)

Two tests will be given during the semester. The first test will be ***Friday, February 24th*** and the second test will be ***Friday, March 31st***. Your highest test grade will count twice as shown in Equation 1 OR Equation 2.

$$TestAvg = \frac{2(Test_1) + Test_2}{3} \; when \; Test_1 > Test_2 \tag{1}$$

$$TestAvg = \frac{Test_1 + 2(Test_2)}{3} \; when \; Test_1 < Test_2 \tag{2}$$

You may bring one 8.5"x11" sheet with hand written equations for use during Test 1 and Test 2. The tests will be closed book. In case of an emergency a reasonable attempt must be made to contact me. Use e-mail or phone call. In these cases a make-up test can be scheduled but will not receive a grade greater than 70

Final

One sheet is permitted for the Final. The final will be a closed book exam. There will not be a make-up for the final.

Section 5 Policy

Academic integrity statement

All conduct in this course is governed by the KGCOE Academic Honesty Policy, RIT Honor Code (P03.0), and RIT Student Academic Integrity Policy (D08.0).

Academic adjustments statement

RIT is committed to providing academic adjustments to students with disabilities. If you would like to request academic adjustments such as testing modifications due to a disability, please contact the Disability Services Office (DSO). Contact information for the DSO and information about how to request adjustments can be found at `http://www.rit.edu/dso`. After you receive academic adjustment approval, it is imperative that you contact the instructor as early as possible to work out whatever arrangement is necessary.

Title IX statement

Title IX violations are taken very seriously at RIT. RIT is committed to investigate complaints of sexual discrimination, sexual harassment, sexual assault, and other sexual misconduct, and to ensure that appropriate action is taken to stop the behavior, prevent its recurrence, and remedy its effects. Title IX rights and resources at RIT can be found at `http://www.rit.edu/fa/compliance/content/title-ix`