Professor: Dr. James E. Moon
Office Hours: Monday: 12–12:50 PM, 2–2:50 PM
Tuesday: 10–10:50 AM(**Zoom**), 5–6:20 PM
Wednesday: 2–2:50 PM
Thursday: 5–6:20 PM
Friday: 12–12:50 PM

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EEEE–380 DIGITAL ELECTRONICS
Fall 2023 — Lecture Hours = 3/wk; Lab Hours = 3/wk; Total Credits = 3

Prerequisites:
EEEE–281 Circuits I ⇨⇨⇨ ***NOTE***: *You may not take this section of Digital Electronics unless you have* ***TAKEN AND PASSED*** *Circuits I*

Course Description:
This course covers the essential concepts and applications of digital electronic circuits, including NMOS and CMOS technologies. After a basic overview of MOSFET devices, NMOS and CMOS inverters are studied from both static and dynamic points of view. Design of combinational and sequential logic networks using CMOS technology is discussed. Dynamic CMOS logic networks are studied, including precharge-evaluate, domino and transmission gate techniques. Several special topics are studied as extensions of the foregoing, including static and dynamic MOS memory.

Reference Text (not required):
CMOS Digital Integrated Circuits: Analysis and Design by Kang, Leblebici, and Kim, **4th ed**., McGraw-Hill, ISBN 978–0–07–338062–9. The 2nd and 3rd editions are not good substitutes because the problems and some of the content are different.

Course Learning Objectives:
A student who successfully fulfills the course requirements will have demonstrated the following:

(1) An understanding of the principles of operation of MOS inverters, as well as an ability to determine their voltage transfer characteristics, noise margins, static power dissipation and propagation delay.
(2) An ability to design static logic gates and networks, including the determination of the sizing of individual transistors to meet performance specifications.
(3) An ability to design dynamic logic gates and networks using a variety of design principles, including precharge-evaluate, domino, and transmission gate logic.
(4) An understanding of the principles of operation of logic components such as pass transistors, transmission gates, latches, and flip-flops.
(5) An understanding of the principles of operation of static and dynamic MOS memory cells and low-power MOS logic.
(6) An understanding of parasitic resistance, capacitance, and inductance associated with devices and interconnect and their roles in determining overall circuit performance, particularly propagation delay.

Lecture Plan:
See separate syllabus. If you miss a lecture, you will need to get notes from a colleague.

COURSE GRADE EVALUATION CRITERIA:

Homework:
Sets of problems will be assigned as the course progresses and solutions will be provided. Homework will not be collected for grading.

My personal belief — supported by extensive experience and data — is that there is great learning value in doing the assigned exercises and problems, and I strongly recommend regularly doing as much of the homework as you can.

***The results of a long-running (15-year) experiment wherein students were given the options of (a) doing homework as part of their grade or (b) not doing the homework for grading are as follows*:**

average exam score for students doing homework = 80%;
average exam score for students opting out of the homework = 73%;

course grades {A, B, C, D, F; total} for students doing homework = {250, 284, 124, 32, 15; 705};
course grades for students opting out of homework = {24, 39, 38, 17, 9; 127}.

Time Commitment:
To be successful in this course — meaning, to have a reasonable expectation of attaining a course grade of A — I would expect that attending the lectures, working through examples, doing the homework, and preparing for exams would require, on average, **8–10 hours per week**. The time actually spent will vary, of course, depending on individual abilities and goals.

Exams:
There will be three mid-term exams (Friday 9/15, Friday 10/13, and Friday 11/10) given during the term. The exams will be based on the homework, lectures, labs, and assigned reading. There will also be a comprehensive final examination on Wednesday, December 13. Any or all of the following may be consulted during the exams, including the final examination: text, notes, your homework solutions, my homework solutions, lecture handouts, lab handouts, and summary sheets prepared by you.

NOTE: EXAMS ARE NOT OPTIONAL. You will receive a grade of 0 (zero) if you do not appear for an exam.

NOTE: USE OF LAPTOPS during exams will be restricted to: the electronic version of the text, if used; to lecture notes, if taken; to any work that you do for homework and lab; and to all course-related material residing on *myCourses*. You may not conduct web-based searches of any kind or use your laptop to communicate with anyone.

Labs:
The lab sequence will be as indicated here and on the course syllabus. Summary reports ("tech memos") will be used as the reporting vehicle for a subset of the labs, and they will be due according to the schedule detailed in the syllabus. A separate handout will be distributed that will give details regarding tech memos.

NOTE 1: LABORATORY WORK IS NOT OPTIONAL, and there will be substantial penalties for late submissions and especially for plagiarism. Tech memos will be due as indicated on the course syllabus (subject to amendment and/or clarification by the Teaching Assistant (TA)). Specific penalties for late pre-lab and tech memo submissions are explained below in Note 3. Plagiarized tech memos will receive scores of 0 (zero) — for both the source and the copy. Students submitting plagiarized work will be subject to additional sanctions ranging from failure of the lab (and hence the course) to expulsion.

NOTE 2: Like lecture, labs will start at the scheduled time. Your TA will be available during the lab period. The TA is not obligated to cover information again that has already been presented to those who joined on time. Pre-lab work must be completed and submitted prior to the start of lab.

NOTE 3: You must pass the lab in order to pass the course. You must have an overall lab score of at least 60% to pass the lab. Under normal circumstances, the labs account for 50% of your course grade. If you fail the labs, however, you will fail the entire course regardless of the quality of your other course work. Late work will be penalized at the rate of 10% per day late — including weekends — down to a maximum penalty of 75% of full credit if submitted more than seven days late. Unsubmitted work will receive a score of 0%. No late work will be accepted after 5 PM on Tuesday, December 12 (reading day).

NOTE 4: For Labs 2, 3, 4, and 6, the split of credit will be 30%/40%/30% for pre-lab work, in-lab work completion (check-off), and tech memo, respectively. For Labs 5 and 7, the split of credit will be 50%/50% for pre-lab work and in-lab work completion.

NOTE 5: You may not opt out of any of the labs. For *every* lab for which no work is submitted, your lab score will be lowered by 20%, in addition to the loss of the credit associated with a particular lab. This includes Lab 0, which is normally 4% of your lab score and, therefore, 1.6% of your course score. This means that you can skip — at most — one lab and potentially still pass the course. If you don't want to do the lab work, don't take the course.

NOTE 6: Pre-lab work, check-off documentation, and tech memos will be submitted to drop boxes in *myCourses*. For any given assignment — *e.g.*, Lab 2 Pre-Lab — submit your work to the regular drop box if it is open. Only submit work to a late drop box if the regular drop box is closed.

NOTE 7: Students who have failed the lab portion of the course — and, therefore, the course (see NOTE 3 above) — will be ineligible to sit for the final exam.

Laboratory Teaching Assistants (Office: 09–3248)

Monday 2:00–4:50 PM (Lab Section 01): Evan Bukofsky	emb6650@g.rit.edu
Monday 5:00–7:50 PM (Lab Section 05): Carley Visser	cev3923@g.rit.edu
Wednesday 5:00–7:50 PM (Lab Section 04): Elaine Greenfield	evg1947@g.rit.edu
Thursday 5:00–7:50 PM (Lab Section 02): Sara Firnstein	smf4748@g.rit.edu
Friday 5:00–7:50 PM (Lab Section 03): Trevor Woodard	tmw7038@g.rit.edu

Laboratory Outline:

(0) Introduction, Ethics	[**4**% of overall lab credit]
(1) SPICE Introduction	[**8**% of overall lab credit]
(2) Design and Simulation of NMOS Inverters	[**18**% of overall lab credit]
(3) CMOS Inverter Design and Dynamic Behavior	[**18**% of overall lab credit]
(4) CMOS Combinational Logic	[**18**% of overall lab credit]
(5) CMOS Sequential Logic	[**8**% of overall lab credit]
(6) CMOS Dynamic Logic	[**18**% of overall lab credit]
(7) SRAM Design and Simulation	[**8**% of overall lab credit]

Preliminary Grade Calculation:

Component	Weight
Exam 1 (Friday, September 15)	10%
Exam 2 (Friday, October 13)	10%
Exam 3 (Friday, November 10)	10%
Laboratories	50%
Final Exam (Wednesday, December 13)	20%

Correspondence of Weighted Course Score to Course Letter Grade

Weighted Course Score	Grade
92–100%	A
90–92⁻%	A–
88–90⁻%	B+
82–88⁻%	B
80–82⁻%	B–
78–80⁻%	C+
72–78⁻%	C
70–72⁻%	C–
60–70⁻%	D
< 60%	F

RIT Refined Grading System (RGS) (Effective Fall 2014)

RGS Grade	Quality Points
A	4.000
A–	3.667
B+	3.333
B	3.000
B–	2.667
C+	2.333
C	2.000
C–	1.667
D	1.000
F	0.000

Additional information regarding grading:

(1) Extra-credit is never offered on an individual basis since this is inherently unfair. There is sufficient work in the course for you to demonstrate what you have learned.

(2) A grade of Incomplete (I) is not intended to be used simply to avoid a poor grade. If you don't do the course work, don't ask about an Incomplete. I don't give them, except in cases of long-term hospitalization or administrative circumstances that are completely beyond the control of the student. ***If you can't commit to doing the course work, don't take the course.***

(3) Submitted work for any aspect of the course that is detected as having been generated in part or *in toto* by any form of Artificial Intelligence (AI) or similar tools will receive a score of 0 (zero).

Special Needs:
Students that have special needs that go beyond those of the usual student — aside from students who are already classified as deaf or hearing-impaired and are listed as such on the class roster — must present documentation to the instructor to certify the nature of his/her needs at the beginning of the term. This will allow the instructor to plan ahead with the objective of best serving your needs.

COURSE POLICY ON ACADEMIC HONESTY

KGCOE HONOR PRINCIPLES: *RIT Engineering faculty, staff and students are truthful and honorable, and do not tolerate lying, cheating, stealing, or plagiarism.*

All members of our community are expected to abide by these principles and to embrace the spirit they represent. We each have a responsibility to address any unethical behavior we observe; either through direct discussion with the offending party, or by discussion with an appropriate faculty or staff member. Allowing unethical behavior to continue unchallenged is not acceptable.

Rochester Institute of Technology does not condone any form of academic dishonesty. Academic dishonesty falls into three basic areas: cheating, duplicate submission and plagiarism (refer to http://www.rit.edu/kgcoe/advising/handbook.pdf pages 19-20 for more information).

Throughout the course, the following specific conditions exist in regards to academic honesty:

Course Element	**Specific Conditions**
Homework: Ungraded	Student collaboration is encouraged.
Exams	Individual exercise; collaboration of any kind is prohibited. Detection of collaboration will result in an exam score of 0 and in irrevocable course failure.
Laboratory Assignments	One submission required from each individual; plagiarism is strictly prohibited — detection will result in automatic failure of the corresponding lab, with a score of 0.

Any act of academic dishonesty will incur the following consequences. After notifying and presenting the student with evidence of such misconduct, the instructor has the full prerogative to assign a lower grade, including an "F" for the offense itself or for the entire course. If after careful review of the evidence, the instructor decides that the student's actions are indeed misconduct and warrant a penalty, the instructor will add a letter to the student's file in his or her home department (copy to the student, Department Head and the Dean) documenting the offense. Depending on the seriousness of the offense, the student may also be brought before the Academic Conduct Committee of the College in which the offense occurred, and may face academic suspension or dismissal from the Institute. The student has the right to appeal any disciplinary action as described in section D17.0 "Academic Conduct and Appeals Procedures" and D18.0 "RIT Student Conduct Process" of the Institute Policies and Procedures Manual.