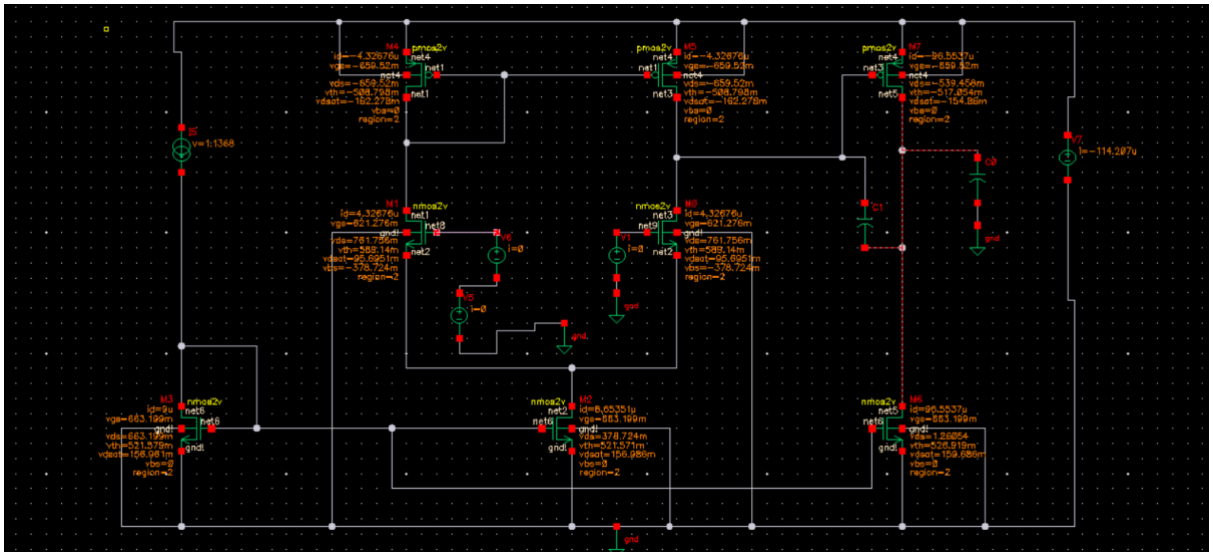
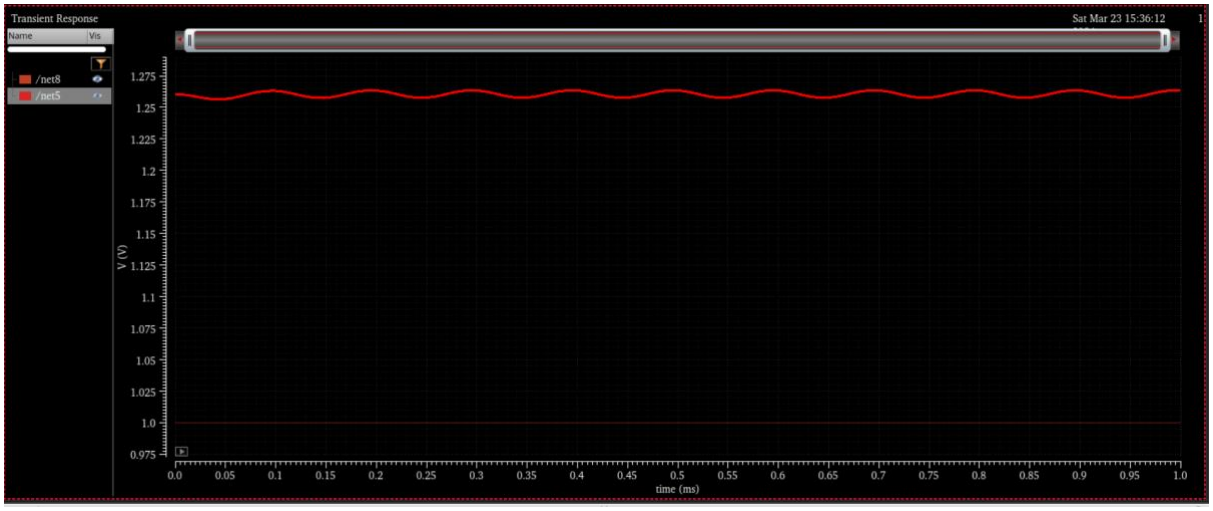
ANALOG ASSIGNMENT-4 (EE23MTECH14013)

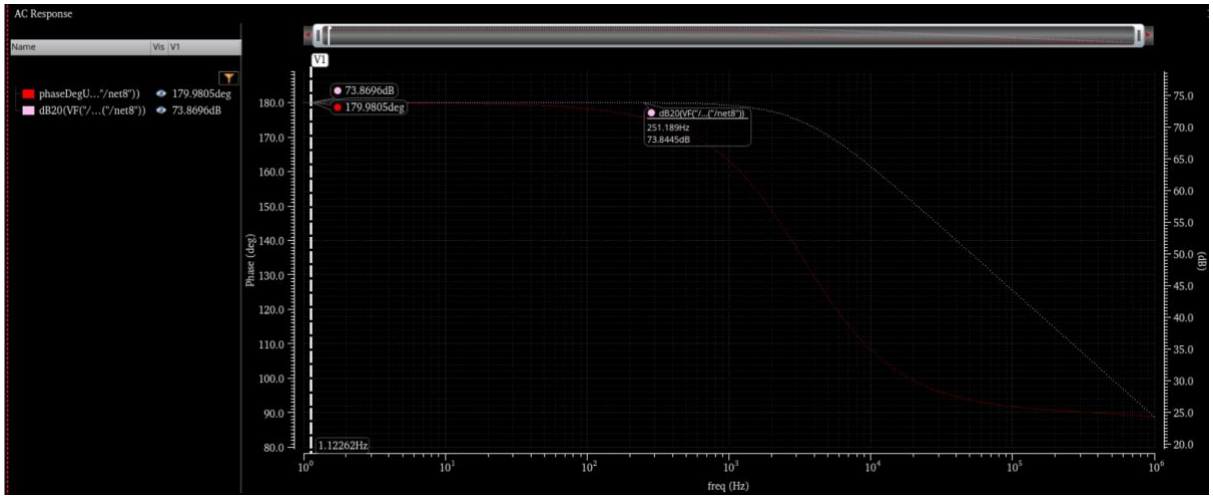
OTA-NMOS SCHEMATIC:



Transient response:

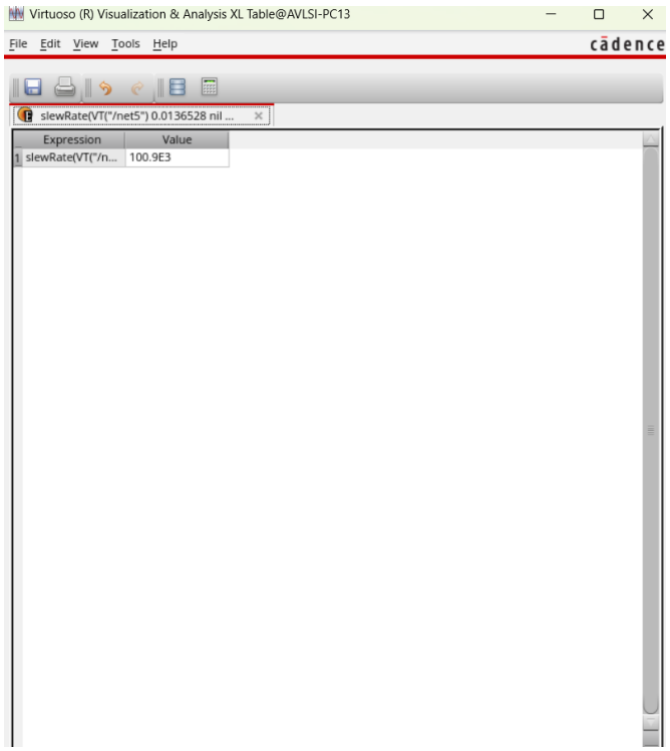


PHASE AND GAIN PLOT:



The gain obtained is 73.8696db.

SLEWRATE:



The slew rate obtained from the above calculation is 100v/us.

NMOS OTA

$C_c = 0.6\,pF$ $\quad C_L = 2pF$

small gain = 80dB.

$U.G.B.W = 10\times10^3 \times 17{,}782.794$

$= 177.827\,MHz.$

$g_{m_1} = U.G.B.W \times 2\pi \times C_c$

$g_{m_1} = 106.6962\times10^{-6} = \sqrt{2\beta|I_{D1}|}$

$|I_{D1}| = 4.5\mu A$

$$\left(W/L\right)_1 = \frac{(106.6962)^2 \times 10^{-12}}{2\times 230\times10^{-6}\times 4.5\times10^{-6}}$$

$\left(W/L\right)_1 = 5.4995 \simeq 5.5 \simeq 6$

$= \left(W/L\right)_2$

For $(W/L)_1$ ——

For $(W/L)_5$ $\quad 0.8 = \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{th} + \sqrt{\frac{2I_{D5}}{\beta_5}}$

$$0.3 = \sqrt{\frac{2I_{D1}}{\beta_1}} + \sqrt{\frac{2I_{D5}}{\beta_5}}$$

$$(W/L)_5 = 1.682 \simeq 2 = (W/L)_8$$

$$(W/L)_{3,4} = \frac{2I_{D3}}{\mu_p C_{ox}[V_{DD} - |CMR| - V_{t3max} + V_{t1max}]}$$

$$= \frac{2 \times (4.5) \times 10^{-6}}{75 \times 10^{-6} \times (1.8 - 1.6)^2} = 3$$

$V_{ISG4} = V_{ISG6}$

$$\frac{g_{m4}}{R_4} = \frac{g_{m6}}{R_6}$$

$$g_{m3} = \sqrt{2\beta I_{D3}}$$

$$g_{m3} = \sqrt{2 \times 75\times10^{-6} \times 3 \times 4.5\times10^{-6}}$$

$$g_{m3} = \sqrt{150 \times 13.5 \times10^{-12}}$$

$$g_{m3} = 45\,\mu \text{ siemens.}$$

$g_{m6} = 10 g_{m1}$

$\therefore g_{m6} = 1066.962 \times 10^{-6}$

$$\frac{45\times10^{-6}}{3} = \frac{1066.962\times10^{-6}}{(W/L)_6}$$

$$(W/L)_6 = 71.1308$$

$$g_{m6} = \sqrt{213.6}$$

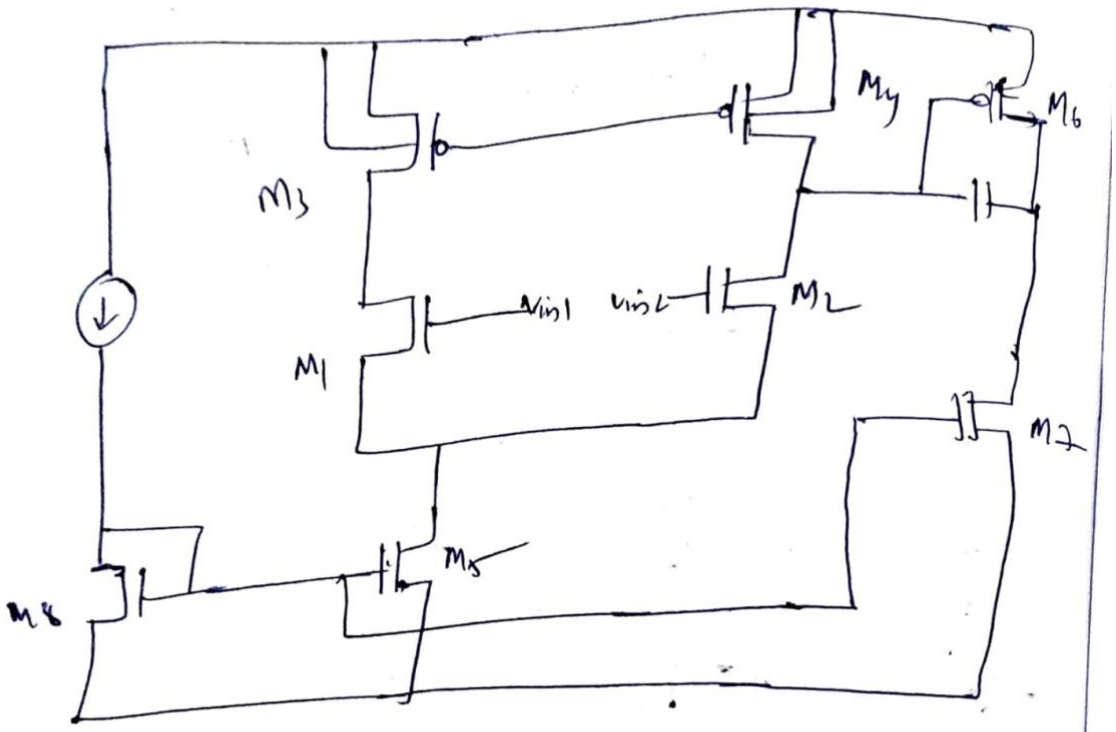
$$1066.962 \times 10^{-6} = \sqrt{213.6}$$

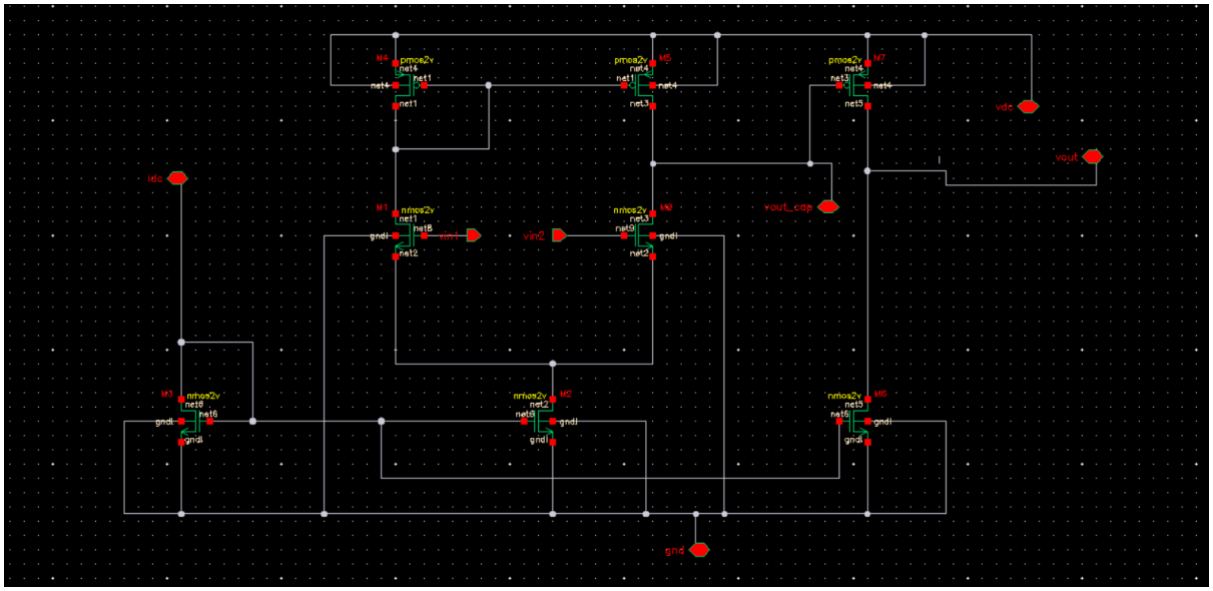
$$106 = 106.69 \times 10^{-6} = 107$$

$$\frac{15}{17} = \frac{(W/L)_1}{(W/L)_7}$$

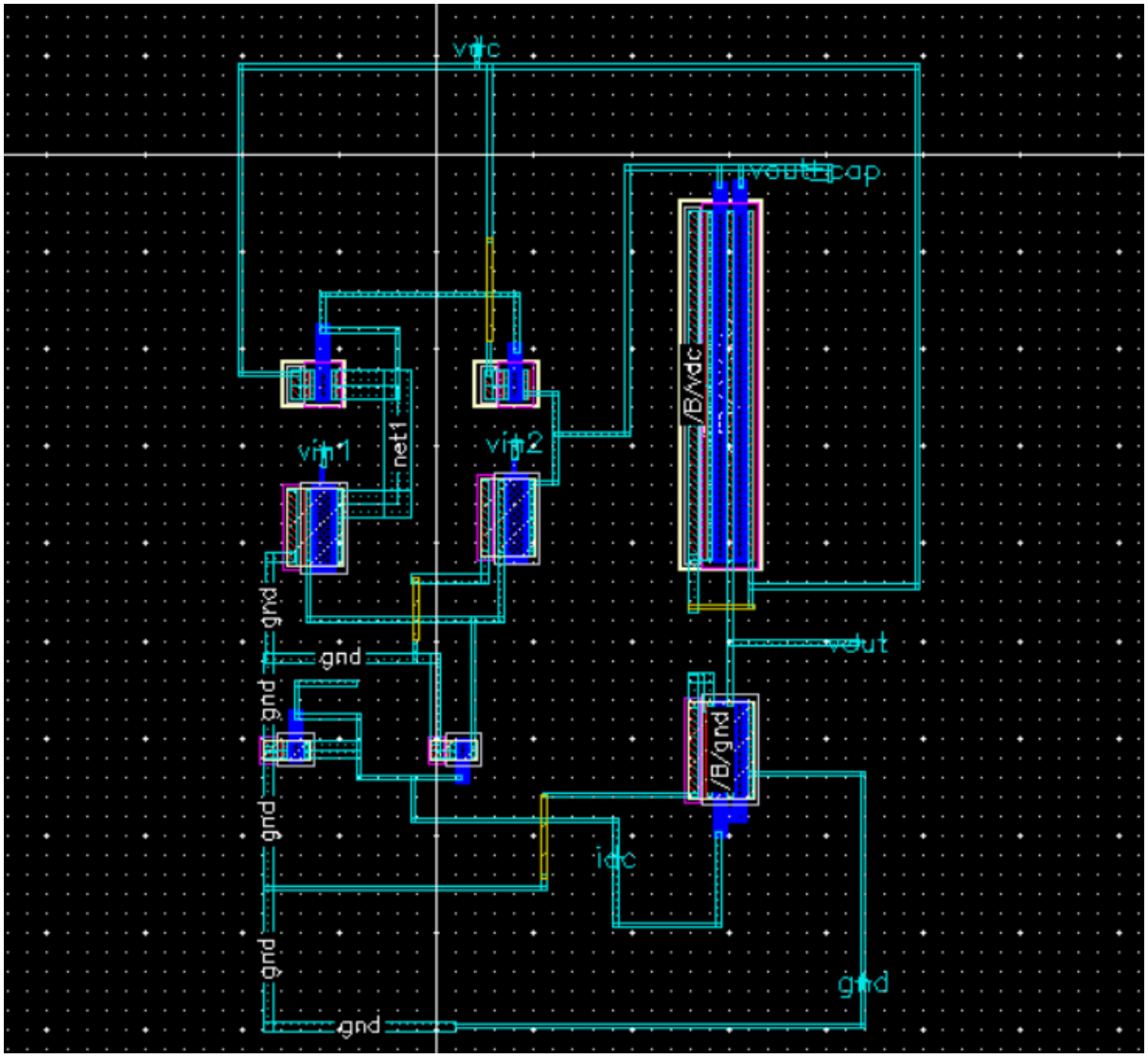
$$(W/L)_5 = 1.68 \angle \quad (W/L)_8 = 1.048 \simeq 1 \angle$$

$$(W/L)_4 = 19.939$$


M4
M6
M3
Vin1
Vin2
M2
M1
M7
M5
M8


vdc
vout
idc
vout_cap
vin1
vin2
gnd

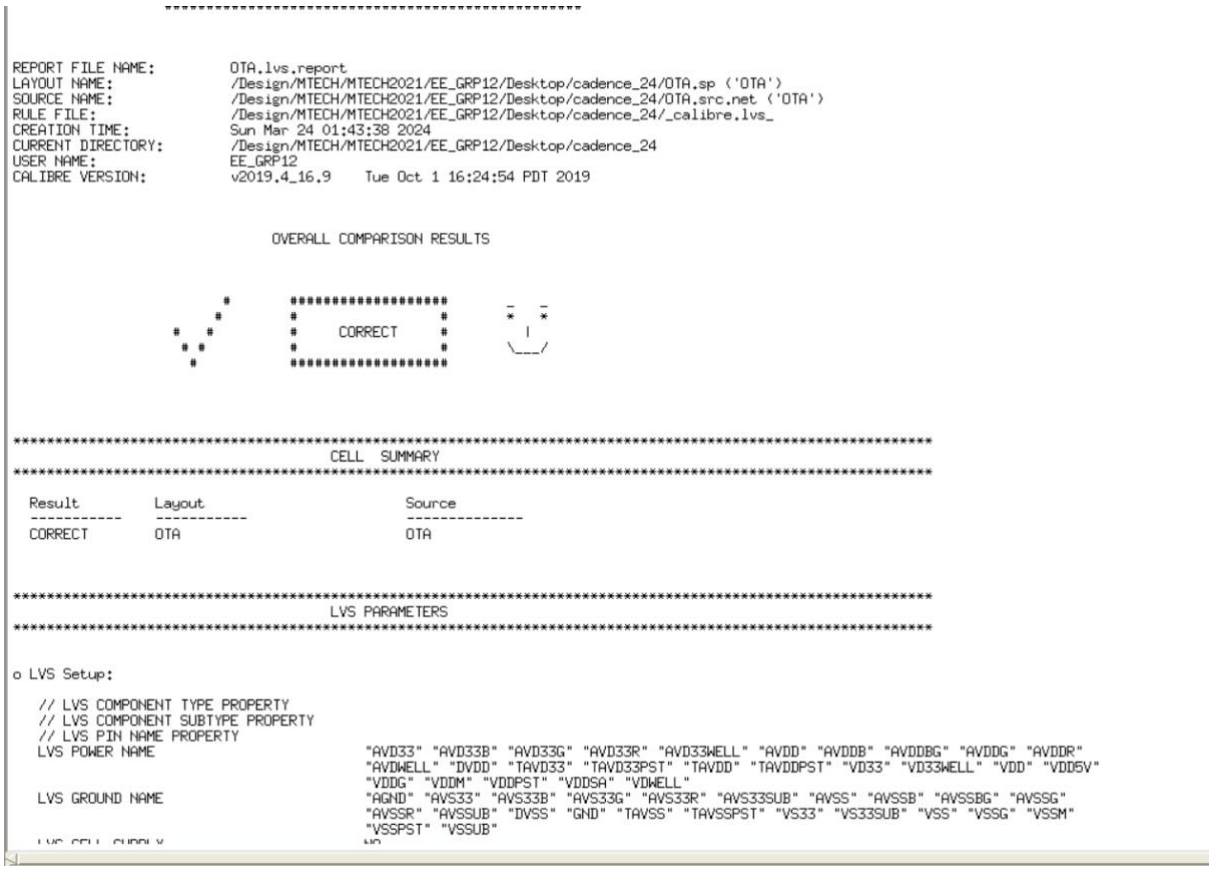
LAYOUT:


vdc
vout_cap
/B/vdc
vin1
net1
vin2
gnd
gnd
gnd
gnd
vout
/B/gnd
idc
gnd
gnd

DRC ERRORS:

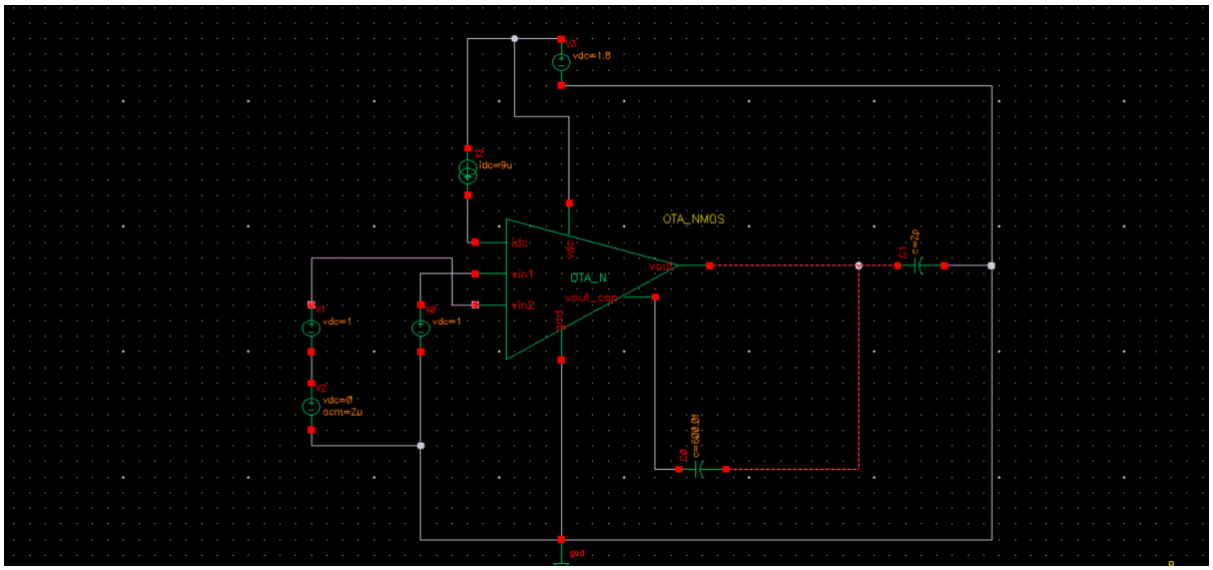
In the above DRC report only density errors are presented which can be ignored.

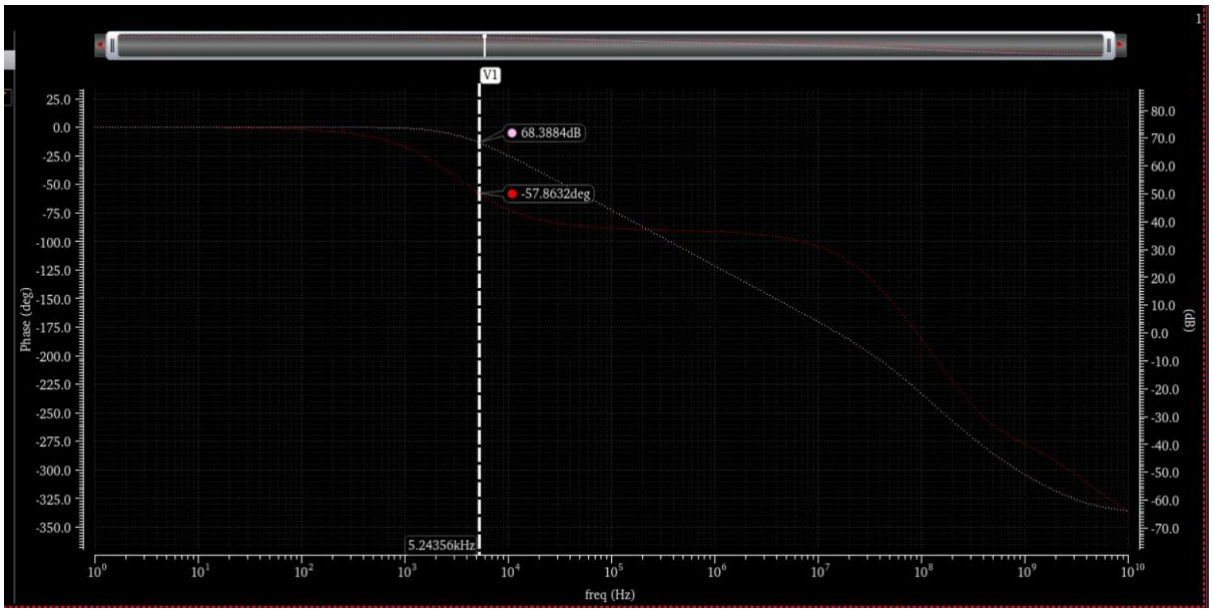
LVS REPORT:



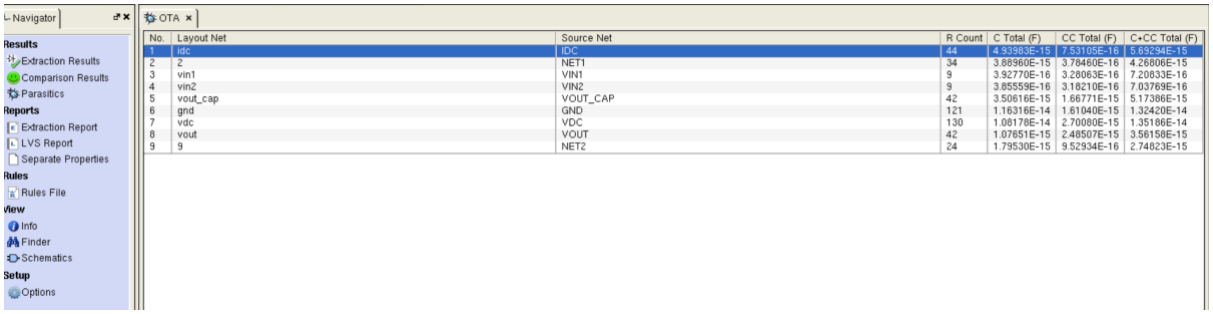
The layout and schematic are matched.

TEST_BENCH:



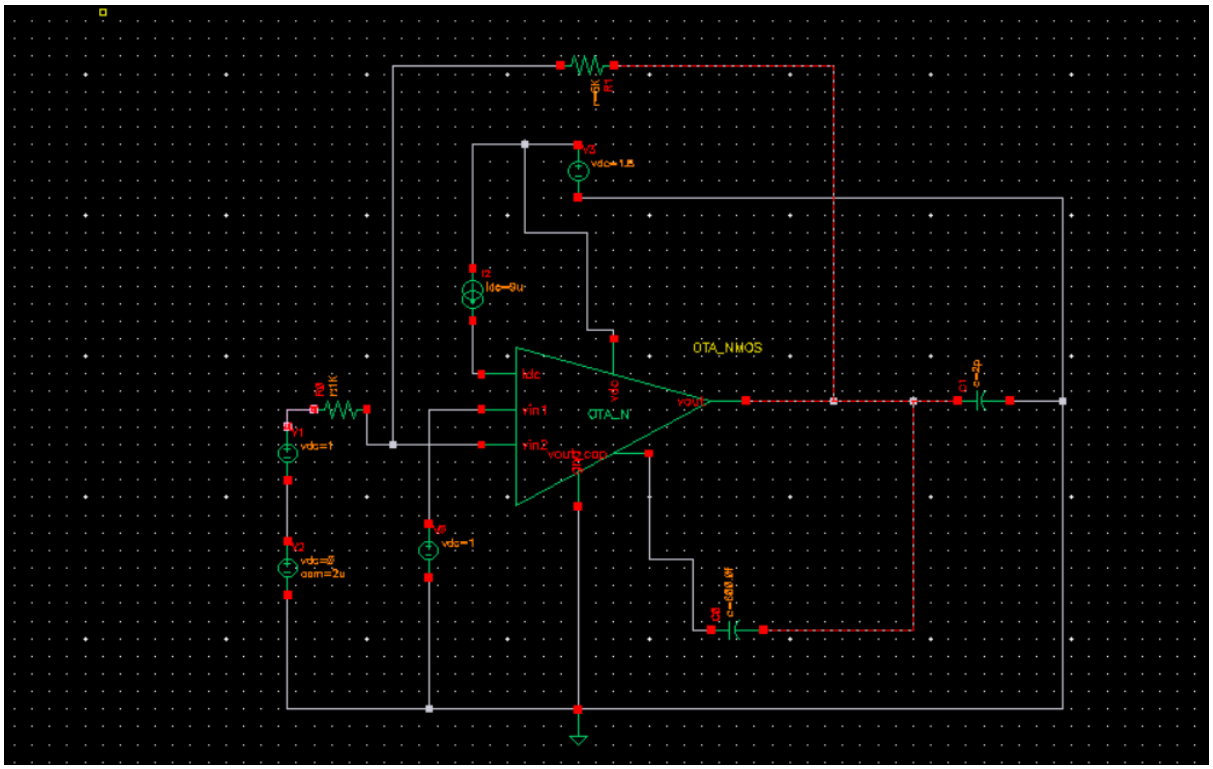


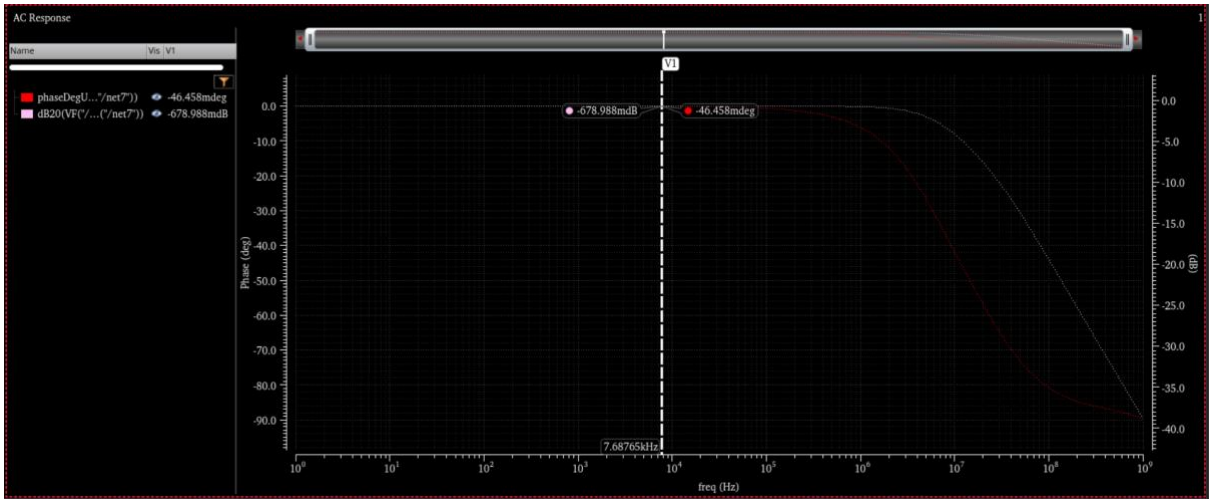
Pex report:



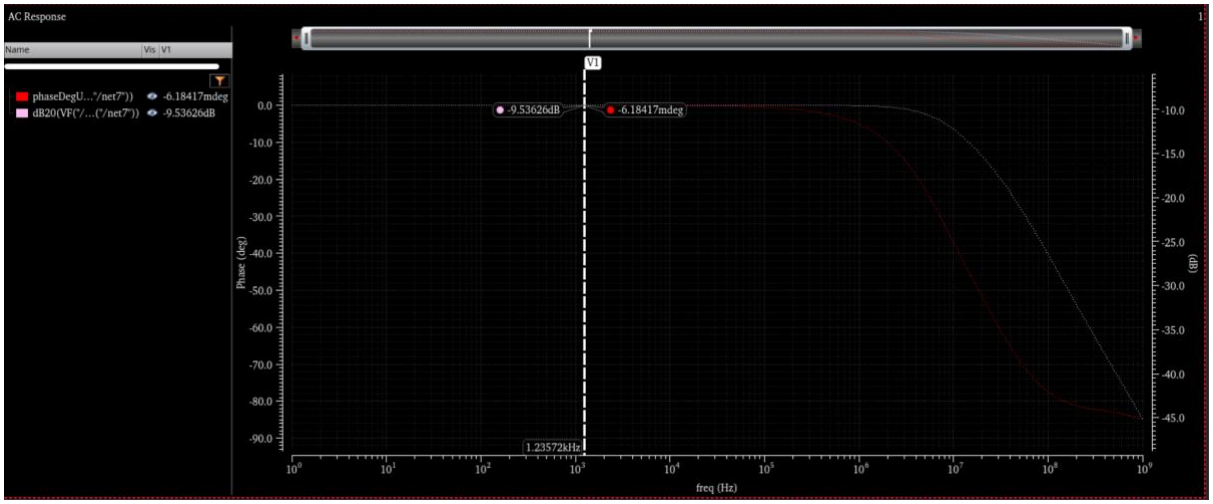
No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	idc	IDC	44	4.93983E-15	7.53105E-16	5.69294E-15
2	2	NET1	34	3.88960E-15	3.78460E-16	4.26806E-15
3	vin1	VIN1	9	3.92770E-16	3.28063E-16	7.20833E-16
4	vin2	VIN2	9	3.85559E-16	3.18210E-16	7.03769E-16
5	vout_cap	VOUT_CAP	42	3.50616E-15	1.66771E-15	5.17386E-15
6	gnd	GND	121	1.16316E-14	1.61040E-15	1.32420E-14
7	vdc	VDC	130	1.08178E-14	2.70080E-15	1.35186E-14
8	vout	VOUT	42	1.07651E-15	2.48507E-15	3.56158E-15
9	9	NET2	24	1.79530E-15	9.52934E-16	2.74023E-15

With feedback gain 5

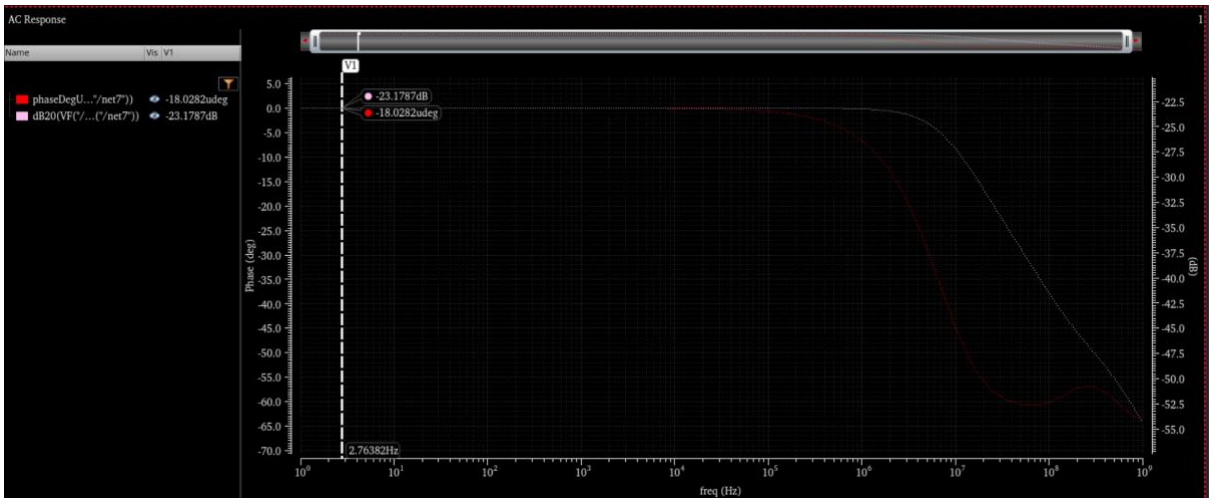




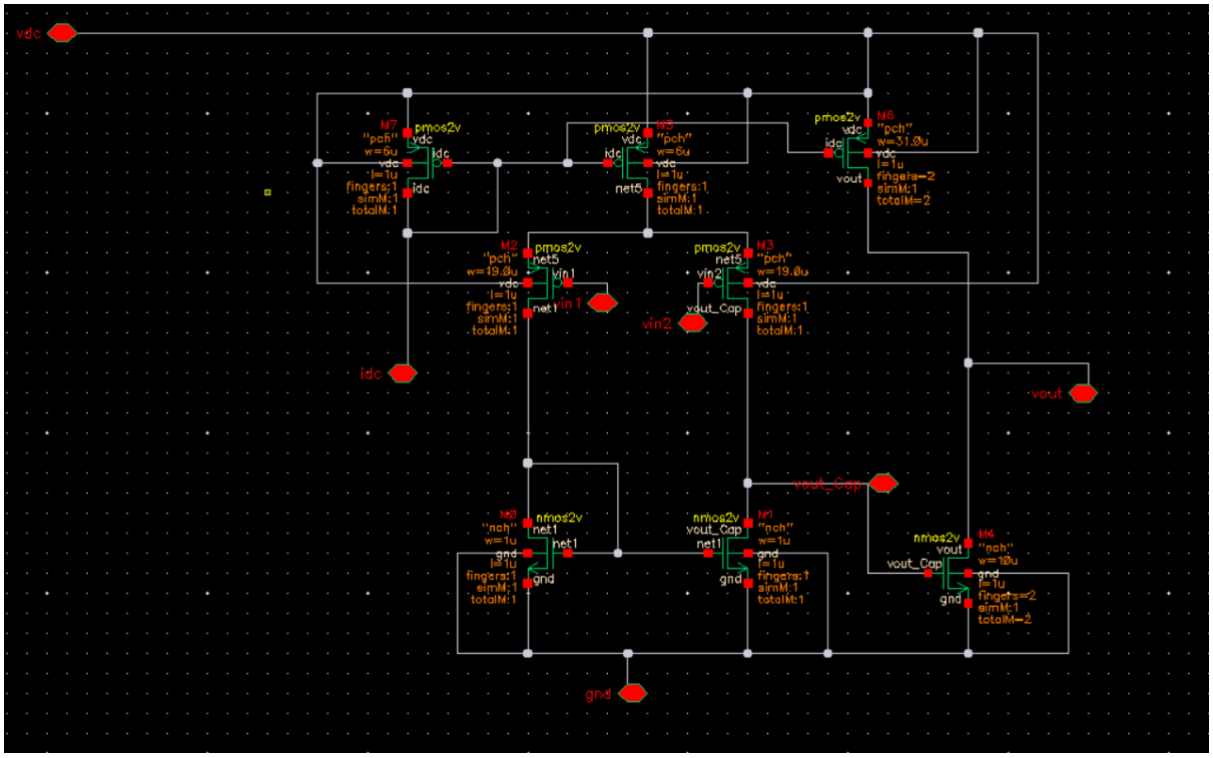
With feedback gain 10



With feedback gain 20:

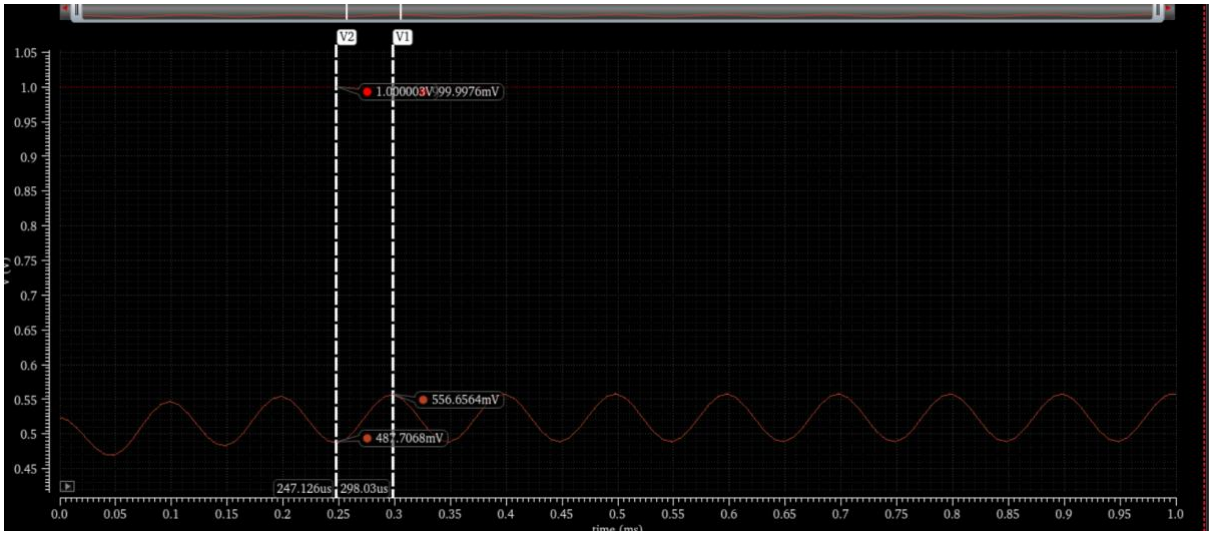


PMOS_OTA:

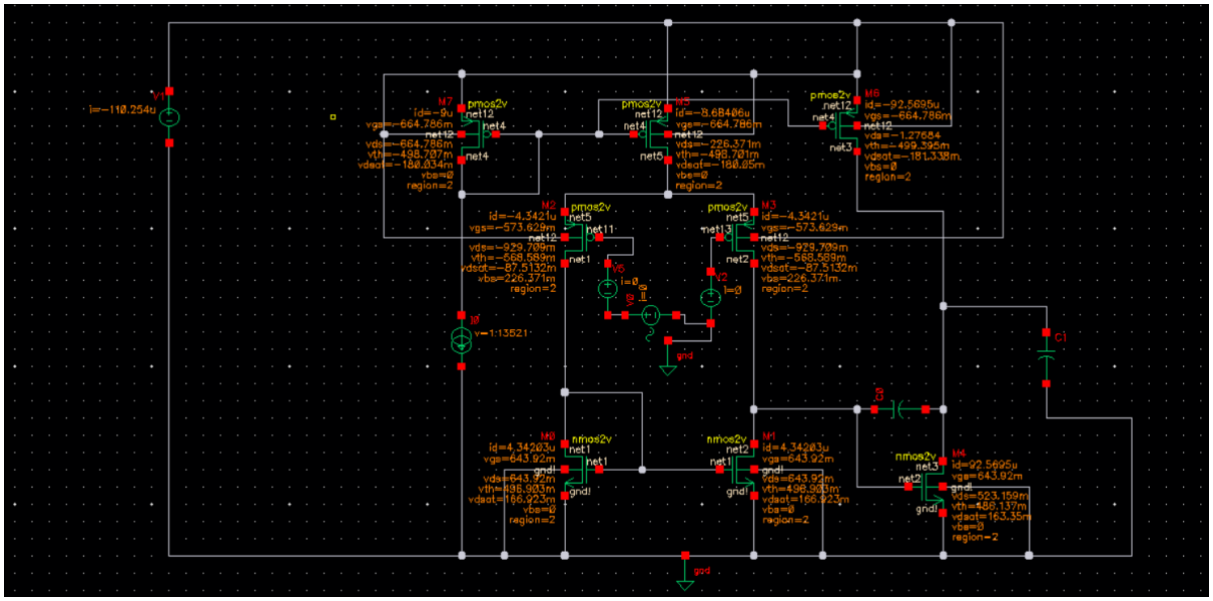


All the transistors are in region 2(saturation region).

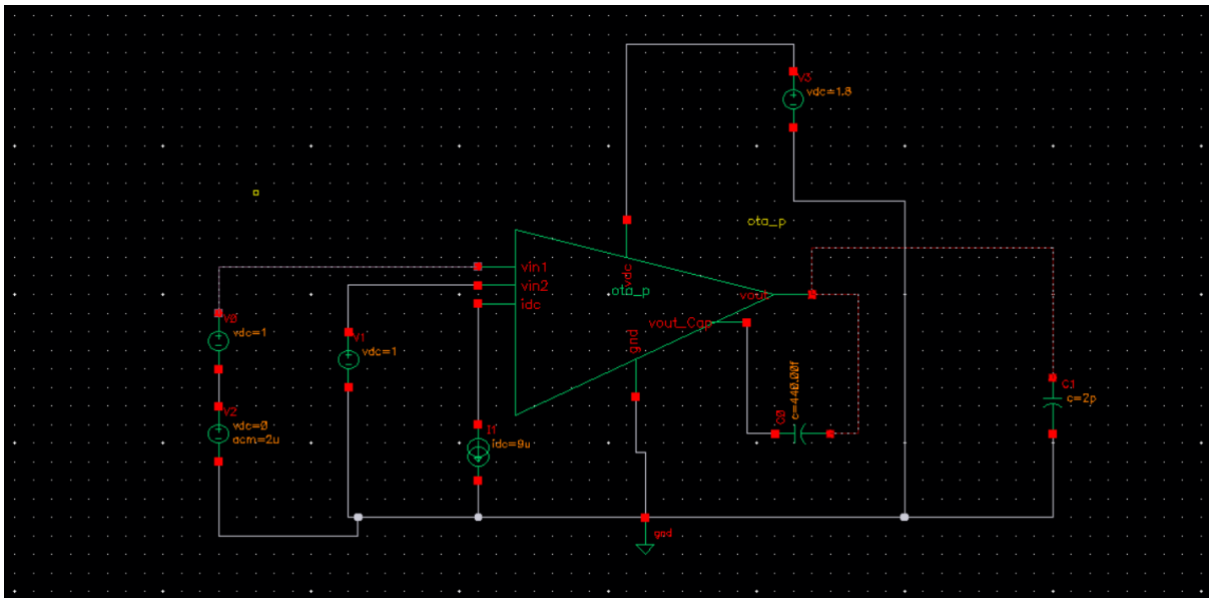
TRANSIENT RESPONSE:

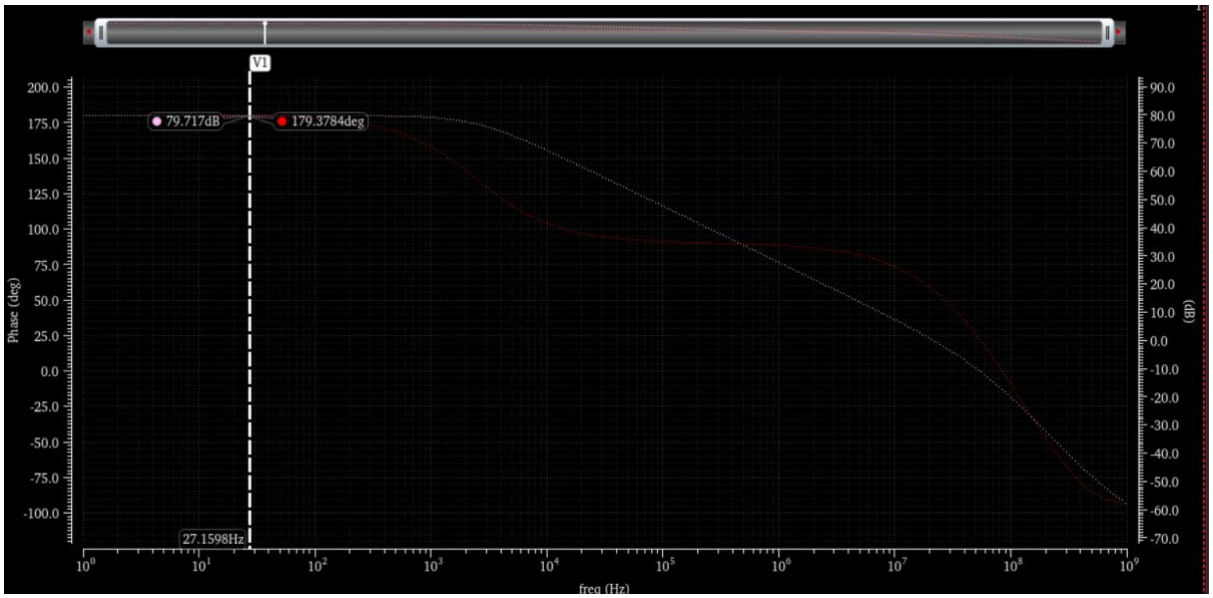

V2
V1
1.000003V
99.9976mV
556.6564mV
487.7068mV
247.126us
298.03us
time (ms)

SCHEMATIC:

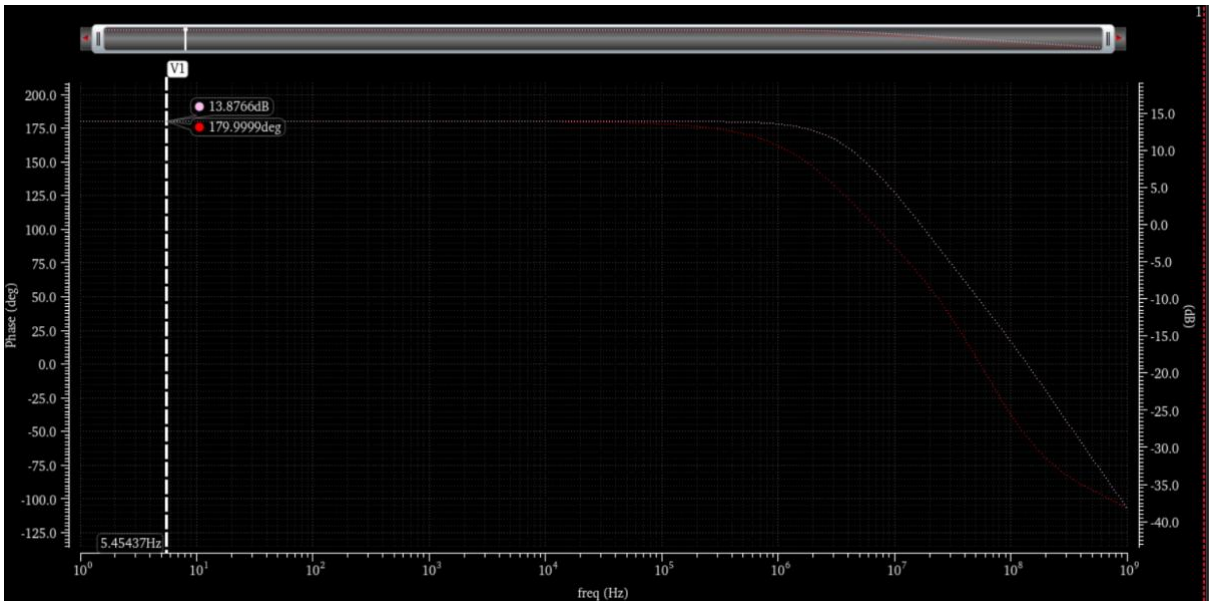


TEST_BENCH:

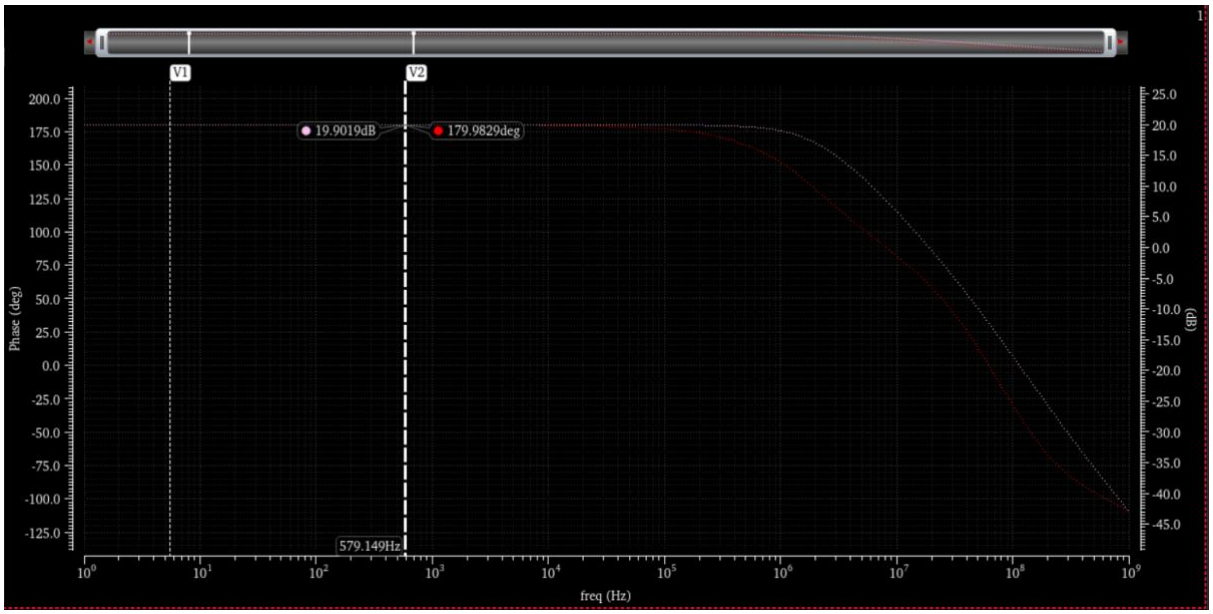

V3
vdc=1.8
ota_p
vin1
vin2
idc
vdc
ota_p
vout
vout_Cap
gnd
V0
vdc=1
V1
vdc=1
V2
vdc=0
dcmv=2u
I1
idc=9u
Cap
C=440.00f
C1
c=2p
gnd


V1
79.717dB
179.3784deg
27.1598Hz
Phase (deg)
(dB)
freq (Hz)

With gain=5



With gain=10



With gain=15