7T SRAM cell (Dual V_T) for low area on SOC using Single-ended operation

Abstract:

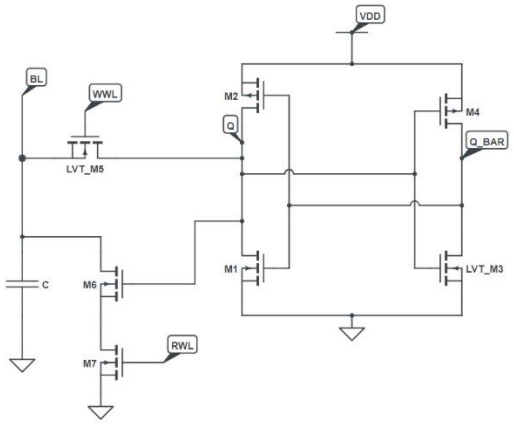
Conventional 6T SRAM architecture poses strict constraints in regard to its sizing to preserve Read Noise Margins and cell ratio is maintained above '1.2'. Also, dynamic power dissipation is higher as one of the bit lines surely discharges during every WRITE operation. The primary goal is to relax cell ratio and sizing norms of standard cell and reduce the power dissipation and leakage current. The adopted 7T SRAM architecture ensures healthy noise margins even for cell ratio of '1' by manipulating Threshold voltage (VT) of access transistor and NMOS (in cross-coupled inverter) (has lower VT) which eases write operation preserving Static Read Noise Margins. The WRITE/READ operation is performed using only one Bit Line; this acts as a single-ended operation which requires asymmetric SRAM structure for stable operation. This avoids the issue of discharging the BIT Line during every READ cycle which greatly reduces the power dissipation.

Origin of the problem:

The conventional 6T SRAM has more dynamic power loss due to usage of two-bit lines (also which makes the peripheral circuitry complex) and also cell ratio needs to be maintained at least 1.2 for stable READ/WRITE operation. As the cell ratio is more, it consumes more cell area in SOC and provides a less area for the computation. Hence, we need an SRAM which has the faster operation and consumes lower power. Hence, a 7T SRAM has been designed (adopted) with cell ratio of 1 and using a single bit line for both read and write operation which makes it less power consuming and space efficient compared to conventional 6T SRAM.

Methodology adopted:

Structure:



The given structure of 7T SRAM consists of a single bit line. The read and write operation are carried out using the single bit line. During the read operation RWL is made high and WWL made low. Conversely, during the write operation, WWL is activated with high voltage and RWL is made low. Transistors LVT_M3 and LVT_M5 have low threshold voltage while LVT_M4, LVT_M2 and LVT_M1 have high threshold voltages to aid for the proper operation of read and write. To accommodate single ended operation, the given cell is deliberately structured in asymmetric manner.

- **Write**

Write operation is initiated only on one end of the SRAM cell. The Low-Threshold NMOS transistors assists the Write operation (as it's an asymmetric structure). Bit Line is pre-charged with logic needed to be stored at storage node Q. Write Word Line (WWL) is enabled and Read Word Line (RWL) is disabled during Write operation.

Write 1:

Bit Line is pre-charged to V_{DD} and WWL is enabled. Logic low (0) and Logic high (V_{DD}) are stored at storage nodes Q and Q_BAR respectively. The LVT_M5 switches on early driving the node Q. Since, the driving capability of M5 is higher than M1, the node Q is driven to store logic high. Since, NMOS passes a Weak 1, Node Q doesn't reach V_{DD}. Since, node Q drives LVT_M3, Q_BAR is driven towards ground. Q_BAR switches on M2 (PMOS) which the drives node Q to V_{DD} (Strong 1).

Write 0:

Bit Line is pre-charged to 0 and WWL is enabled. Logic high (V_{DD}) and Logic low (0) are stored at storage nodes Q and Q_BAR respectively. Node Q discharges to ground through LVT_M3 (as BL is at 0) even though M2 tries to drive node Q to V_{DD} (since M3 has higher driving capability). As node Q goes down to logic low, M4 starts to switch on and drives node Q_BAR to V_{DD}. And the cross-coupled connections ensure stable 0 and 1 at node Q and Q_BAR resp.

- **Read**

Read operation has a separate path to detect the potential on node Q. The NMOS transistors M6 and M7 makeup the read path where node Q is given as an input to M6 and the RWL (Read Word Line) is given to M7. The RWL is enabled during read operation and the Bit Line (BL) is pre-charged to V_{DD} where the capacitor C stores the potential V_{DD}. The Write Word Line (WWL) is disabled during read operation. Transistors in cross-coupled inverters remain unaffected during read operation and storage nodes remain undisturbed.

Read 1:

The Bit Line is pre-charged to V_{DD} (logic 1) and the node Q is at a potential of V_{DD} (logic 1). Since, M6 is driven by node Q, M6 gets switched on and since the RWL is enabled, M7 also switches on creating a path to ground. Now, the Bit Line discharges and the potential across the capacitor decreases. The Bit Line is connected to the sensing circuit.

Read 0:

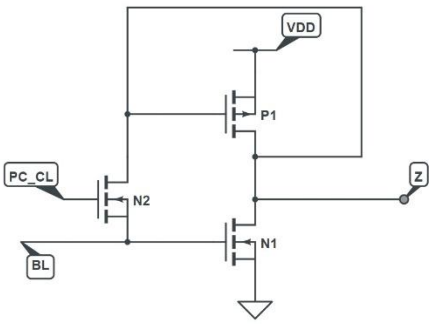
The Bit Line is pre-charged to V_{DD} and the node Q is at a potential of 0 (logic 0). As the M6 driven by node Q (at gate), M6 is switched off. Even though the M7 is switched on (due to RWL), there is no ground path for the capacitor to discharge and the potential across capacitor remains high.

Sensing Circuit:

- **Basic Inverter**

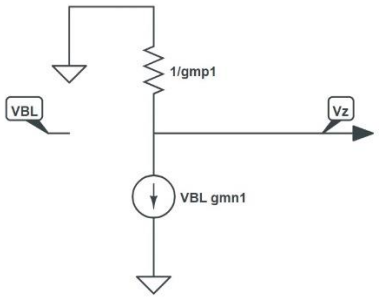
The Bit Line is given as an input to the inverter. During Read 1, bit line gets discharged to ground and it is expected to produce logic high as V_{DD} is stored at node Q. As the Bit Line drives the inverter, output is at logic high (as the bit line goes down to logic low). During Read 0, Bit Line has no discharge path and stores V_{DD}. The output from inverter is at logic low.

- **Common Source Sense Amplifier**



The common source sense amplifier consists of two NMOS transistors and one PMOS transistor. This sense amplifier operates in two stages: Pre-charge and Evaluation. During the pre-charge stage (PC_CL=1). The NMOS N2 is turned ON. From the above figure it can be seen that transistor P1 is diode connected and the BL is pre-charged to V_{DD} -Vtp1. In subsequent evaluation phase (PC_CL=0), the NMOS N2 is off. The drain and gate are shorted to each other. This transforms the transistor P1 to act as small signal resistor. This enables the circuit behaves as a common source amplifier with high inverting value output.

The below diagram shows the small signal model of the above common source amplifier.



The gain can be comprehended in terms of transconductance as Av = -(g_{mn1} / g_{mp1}).

Results and Discussion:

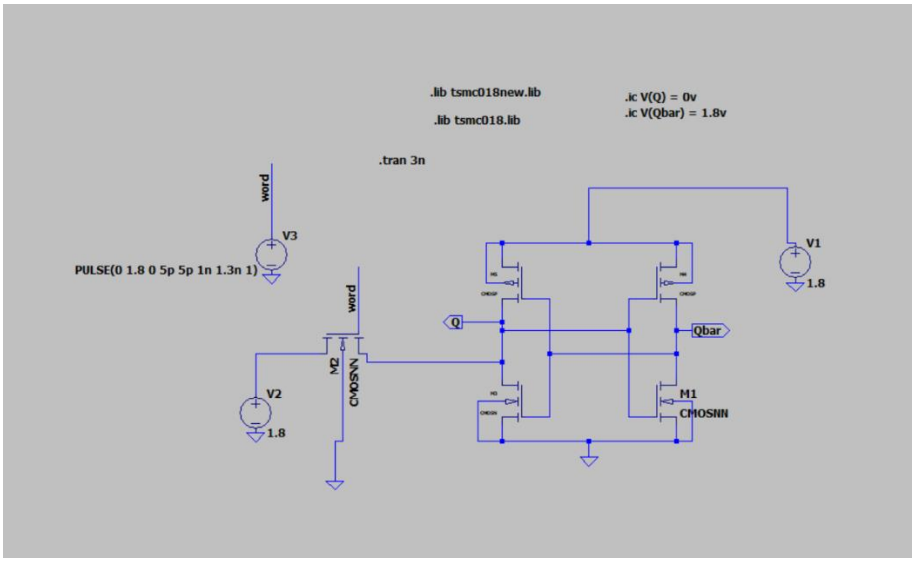


Fig: Schematic for the write operation

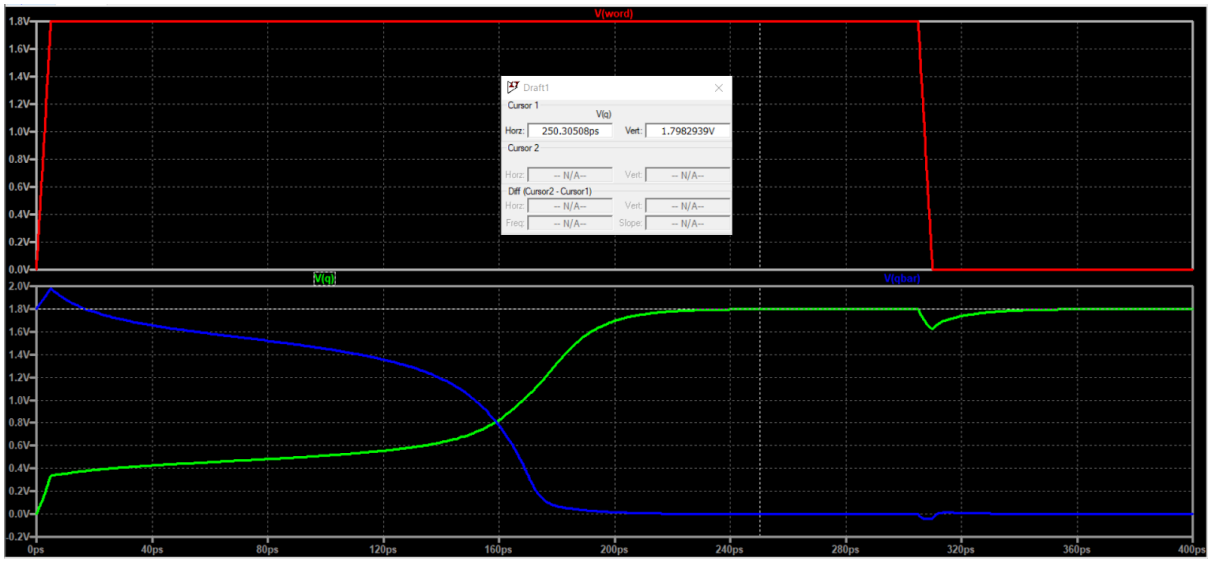


Fig: Write operation of bit 1 at node Q

For the writing 1 at node Q, the time elapsed is around 250.3psec.

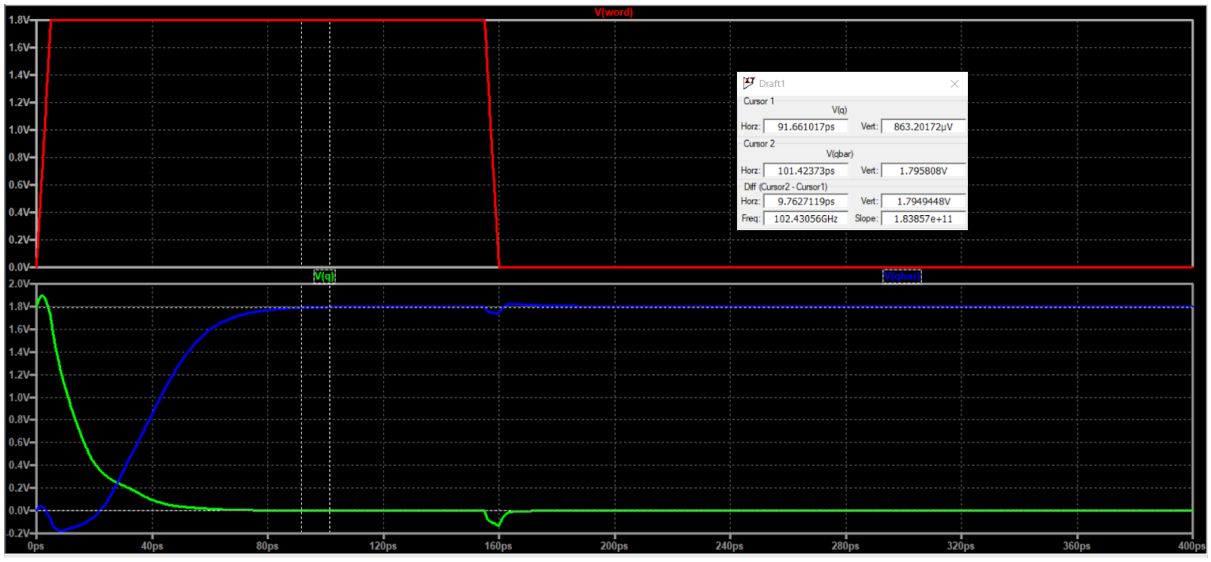


Fig: Write operation of bit 0 at node Q

For the writing 0 at node Q, the time elapsed is around 101.4psec.

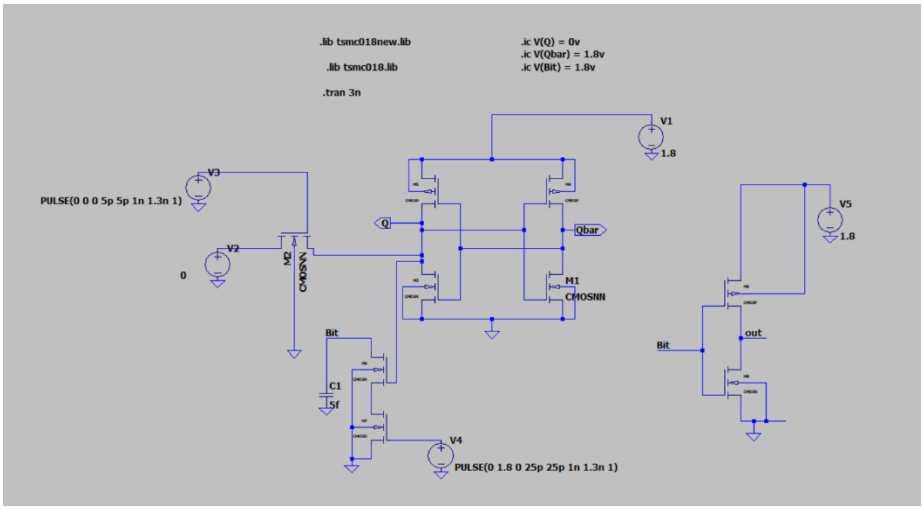


Fig: Schematic for the read operation

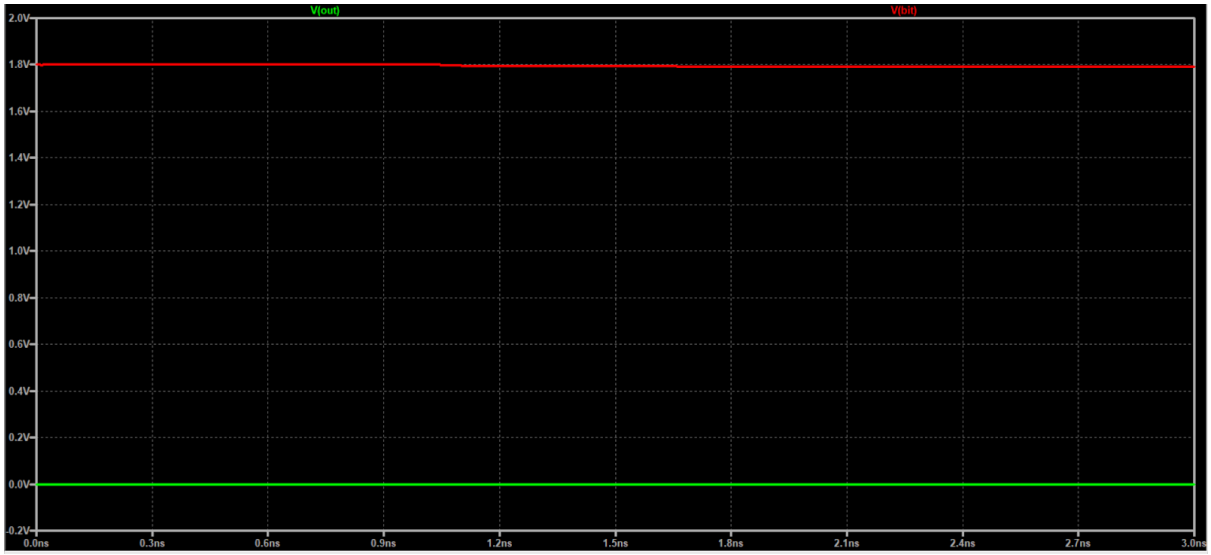


Fig: Reading 0 at node Q

As the node Q have bit 0, the discharge path during read operation is disabled and the bit line voltage is remained at V_{DD}, so that for reading 0, the elapsed time is ∼0 sec.

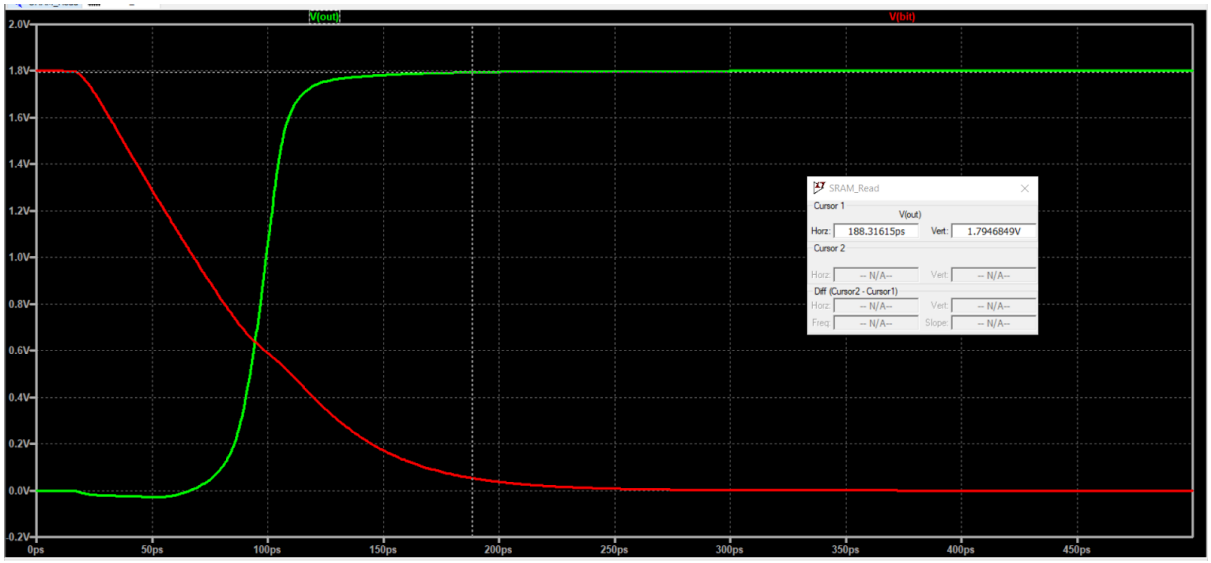


Fig: Reading 1 at node Q

As the node Q has bit 1, the discharge path will be seen by the BL capacitance (red), which is fed to the inverter as the sense amplifier which reads the decrease in BL capacitance voltage and make it read as 1 at node Q. The read time is around 188.3psec.

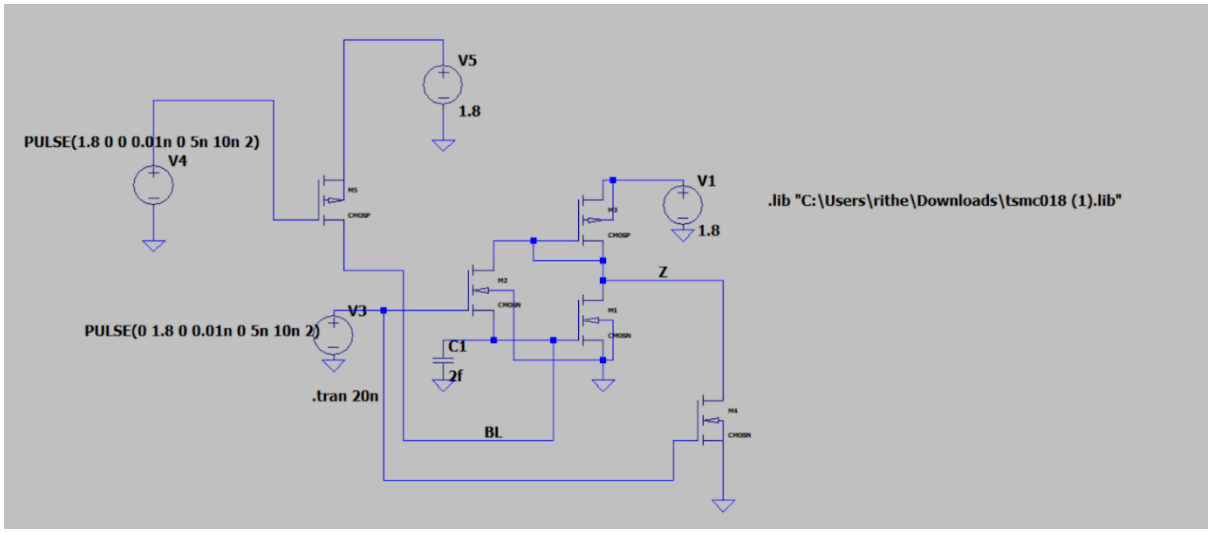
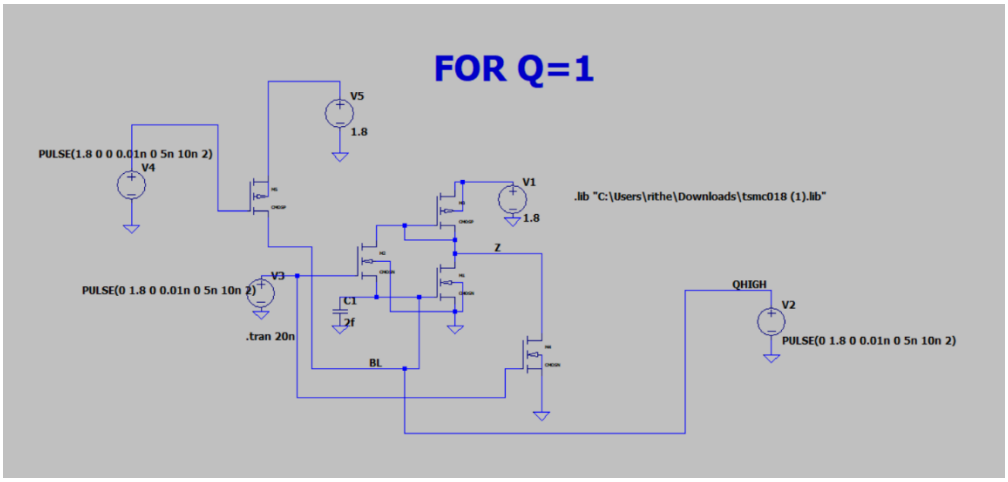
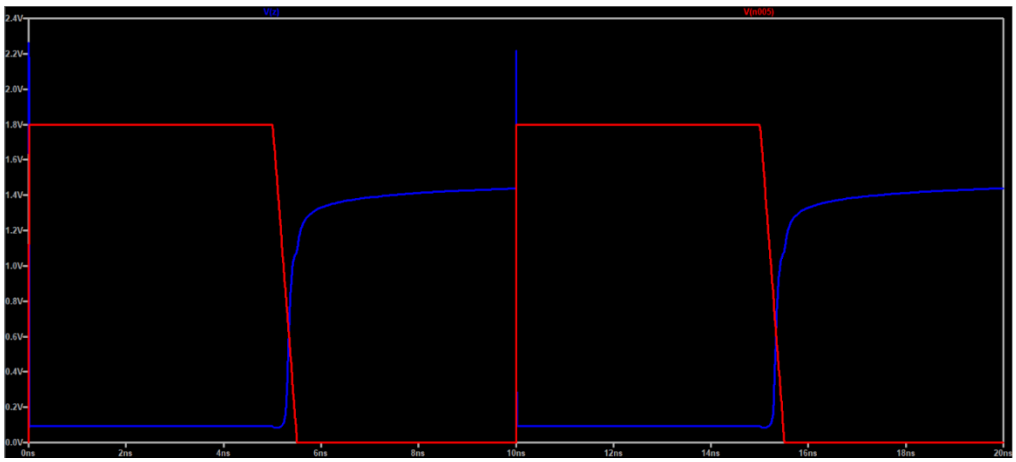


Fig: Schematic For Common Source Sense Amplifier

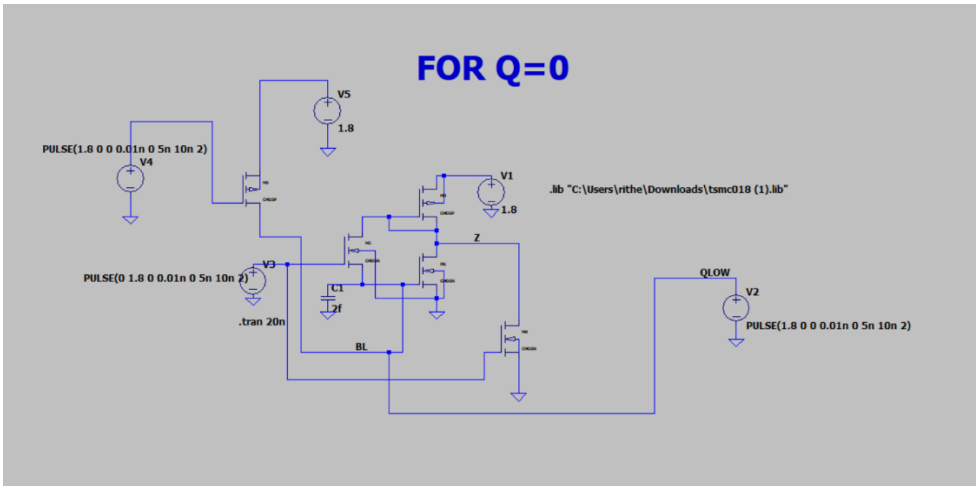
When storage node Q=1, then the bit-line discharges during read operation. Also, when Q=0, the bitline remains at V_{DD}.

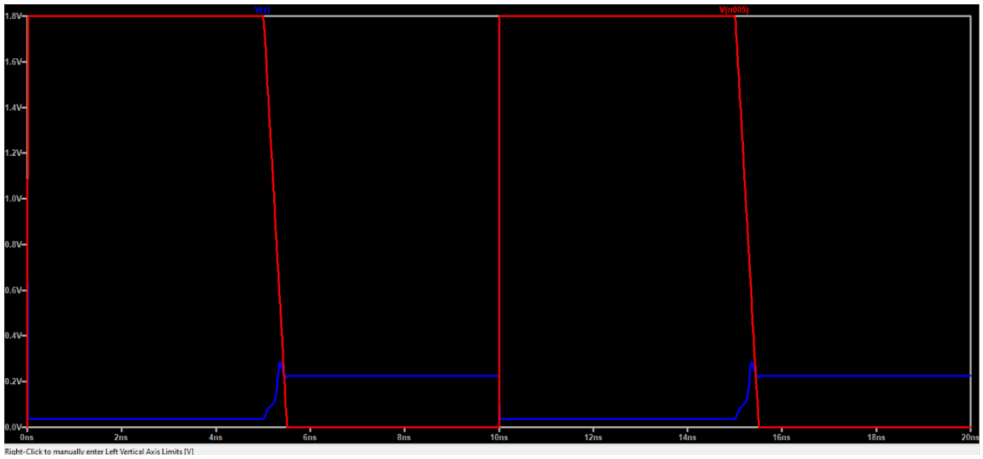
Read of Q=1





Read Of Q=0





Conclusion:

The followed methodology of dual Vt 7T SRAM has been designed using 180nm CMOS technology. As the single bit line is used for both the read and write operation, the power consumption is lesser than that of double bit line as the bit line need not to be discharged for the every read cycle. The cell ratio adopted over here is 1, so that the area consumption in the chip is expected to be reduced.

References:

[1] Ming-Hsien Tu, Jihi-Yu Lin, Ming-Chien Tsai, Shyh-Jye Jou, and Ching-Te Chuang, “Single-Ended Sub-threshold SRAM with Asymmetrical Write/Read-Assist,” in IEEE transactions on circuits and systems-I: regular papers, vol. 57, no. 12, pp. 3039-3047, December 2010.

[2] Jebamalar Leavline, Sugantha A., An efficient common source sense amplifier for single ended SRAM, Memories - Materials, Devices, Circuits and Systems, Volume 5, 2023, 100065, ISSN 2773-0646.

[3] S. A. Tawfik and V. Kursun, “Low power and robust 7t dual-vt sram circuit,” in IEEE International Symposium on Circuits and Systems, pp. 1452–1455, Seattle, Washington, D.C, USA, 2008.

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