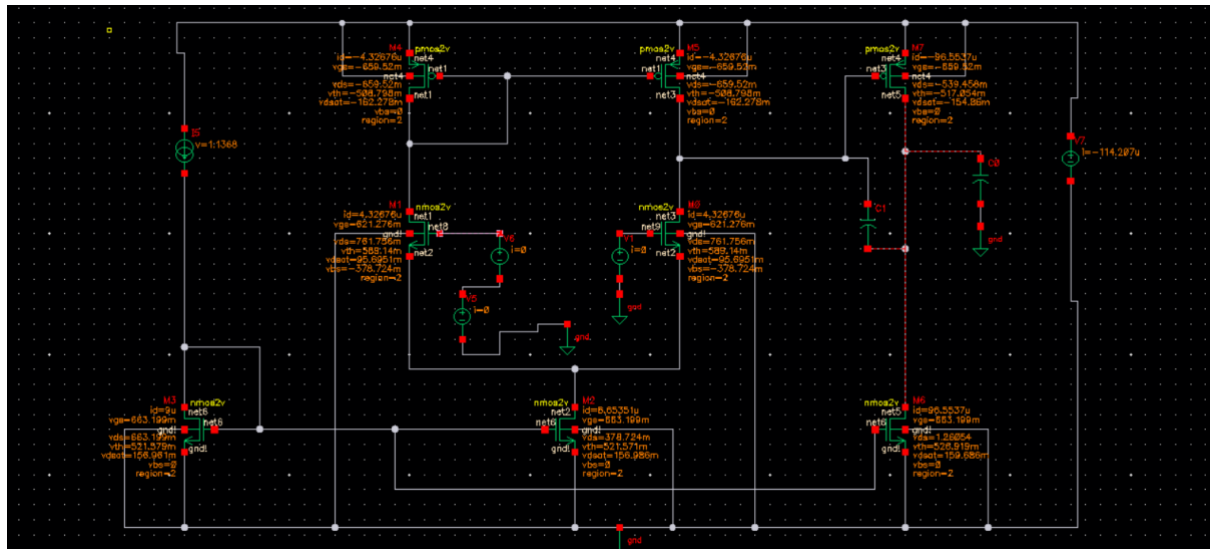
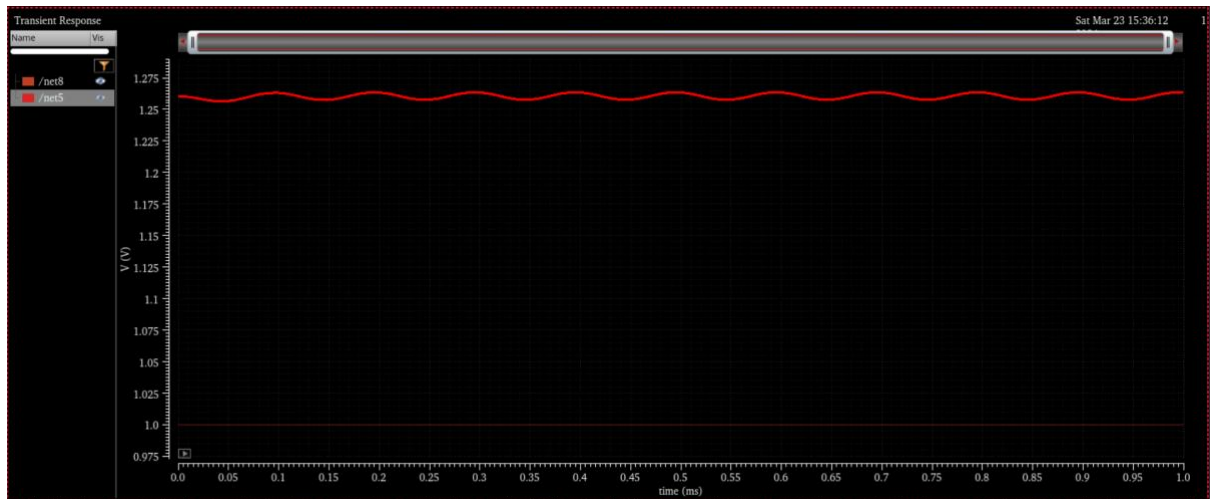


ANALOG ASSIGNMENT-4 (EE23MTECH14013)

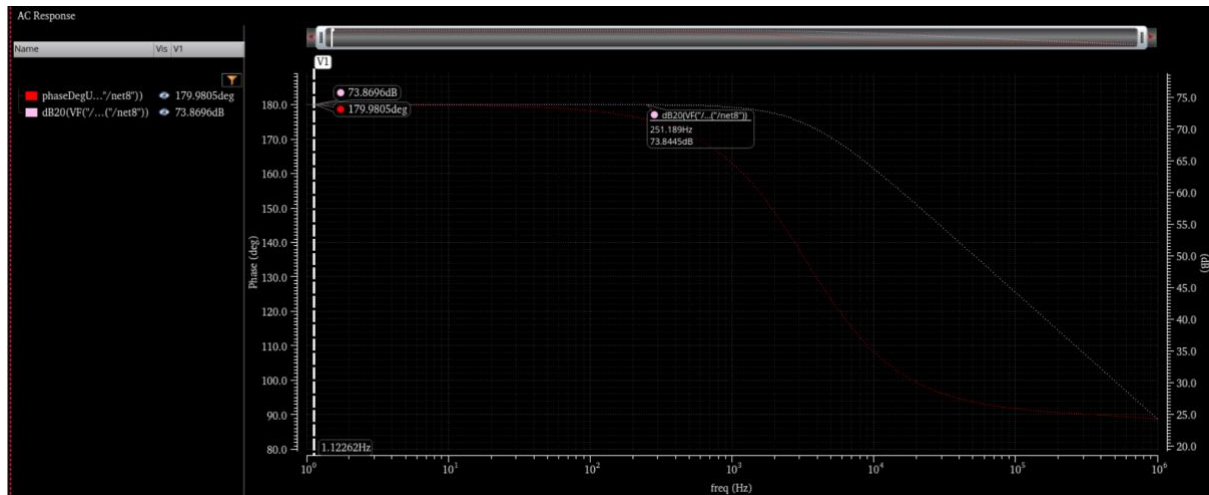
OTA-NMOS SCHEMATIC:



Transient response:

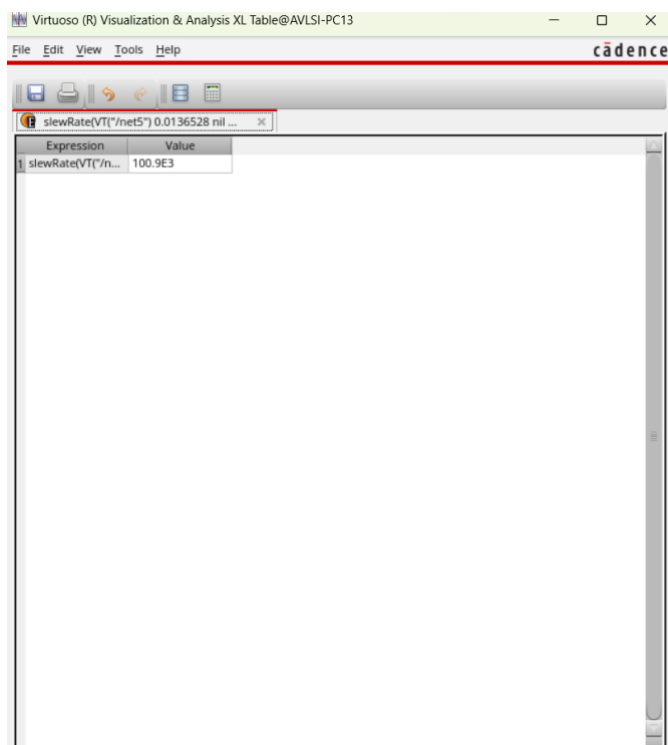


PHASE AND GAIN PLOT:



The gain obtained is 73.8696db.

SLEWRATE:



The slew rate obtained from the above calculation is 100v/us.

NMOS OTA

$$C_C = 0.6 \text{ pF} \quad C_L = 2 \text{ pF}$$

$$\text{small gain} = 80 \text{ dB}$$

$$\begin{aligned} \text{U.G.B.W} &= 10 \times 10^3 \times 17,782.794 \\ &= 177.827 \text{ MHz} \end{aligned}$$

$$g_{m1} = \text{U.G.B.W} \times 2\pi \times C_C$$

$$g_{m1} = 106.6962 \times 10^6 = \sqrt{2\beta I_{D1}}$$

$$I_{D1} = 4.5 \mu\text{A}$$

$$\left(\frac{W}{L}\right)_1 = \frac{(106.6962)^2 \times 10^6}{2 \times 230 \times 10^6 \times 4.5 \times 10^{-6}}$$

$$\begin{aligned} \left(\frac{W}{L}\right)_1 &= 5.7995 \approx 5.5 \approx 6 \\ &= \left(\frac{W}{L}\right)_2 \end{aligned}$$

For $(W/L)_1$

$$\text{For } (w/L)_5 \quad 0.8 = \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{th} + \sqrt{\frac{2I_{D5}}{\beta_5}}$$

$$0.3 = \sqrt{\frac{2I_{D1}}{\beta_1}} + \sqrt{\frac{2I_{D5}}{\beta_5}}$$

$$(w/L)_5 = 1.682 \approx 2 = (w/L)_8$$

$$(w/L)_{3,4} = \frac{2I_{D3}}{\mu_{plox} [V_{DD} - |V_{CMR}| - V_{t3max} + V_{t1max}]^2}$$

$$= \frac{2 \times (4.5) \times 10^{-6}}{75 \times 10^{-6} \times (1.8 - 1.6)^2} = 3$$

$$V_{DS4} = V_{DS6}$$

$$\frac{g_{m4}}{R_4} = \frac{g_{m6}}{R_6}$$

$$g_{m3} = \sqrt{2\beta_1 I_{D3}}$$

$$g_{m3} = \sqrt{2 \times 75 \times 10^{-6} \times 3 \times 4.5 \times 10^{-6}}$$

$$g_{m3} = \sqrt{150 \times 13.5 \times 10^{-12}}$$

$$g_{m3} = 45 \mu \text{ Siemens}$$

$$g_{m6} \approx 10 g_{m3}$$

$$\text{let } g_{m6} = 1066.962 \times 10^{-6}$$

$$\frac{45 \times 10^{-6}}{3} = \frac{1066.962 \times 10^{-6}}{(\omega/L)_6}$$

$$(\omega/L)_6 = 71.1308$$

$$\sqrt{\dots}$$

$$g_{m6} = \sqrt{213.6}$$

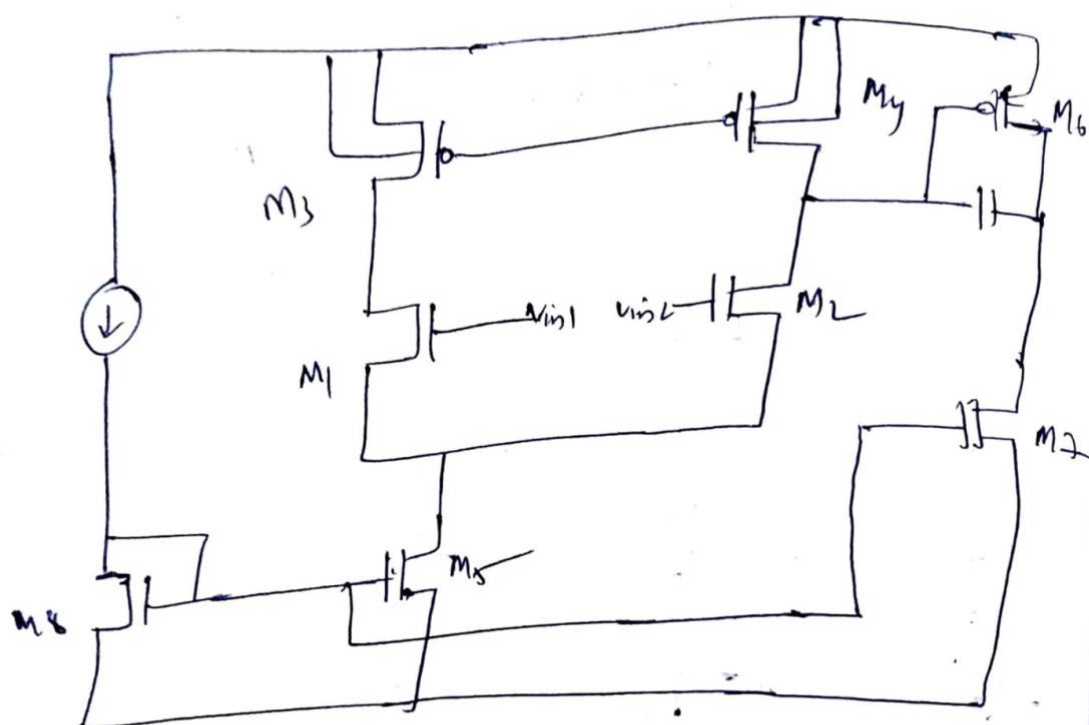
$$1066.962 \times 10^{-6} = \sqrt{213.6}$$

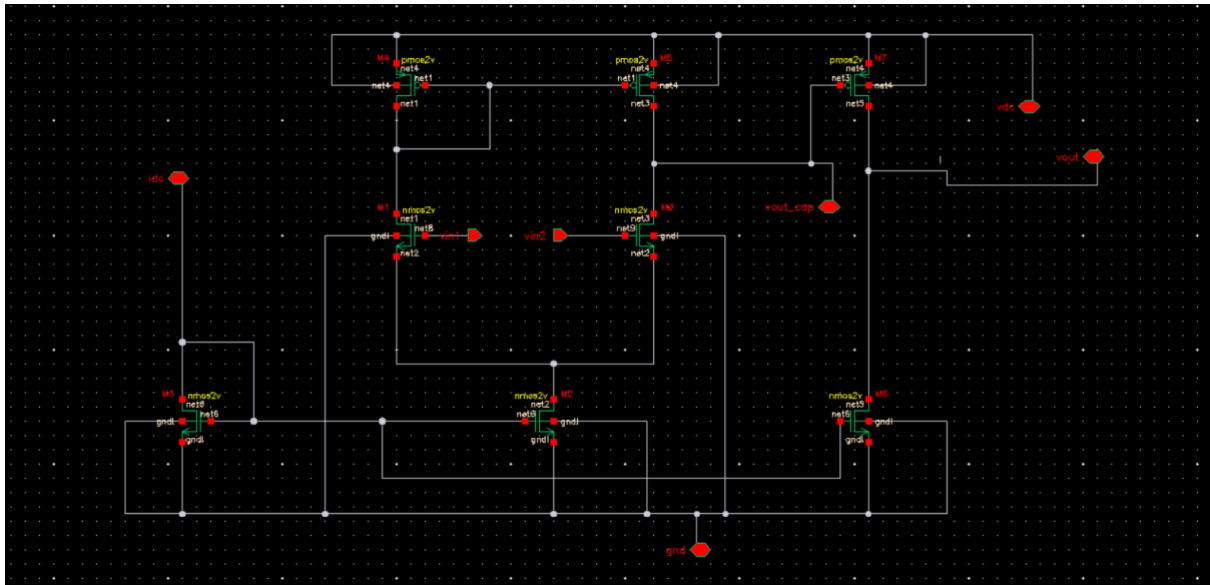
$$106 = 106.69 \times 10^{-6} = 107$$

$$\frac{15}{17} = \frac{(w/L)_5}{(w/L)_7}$$

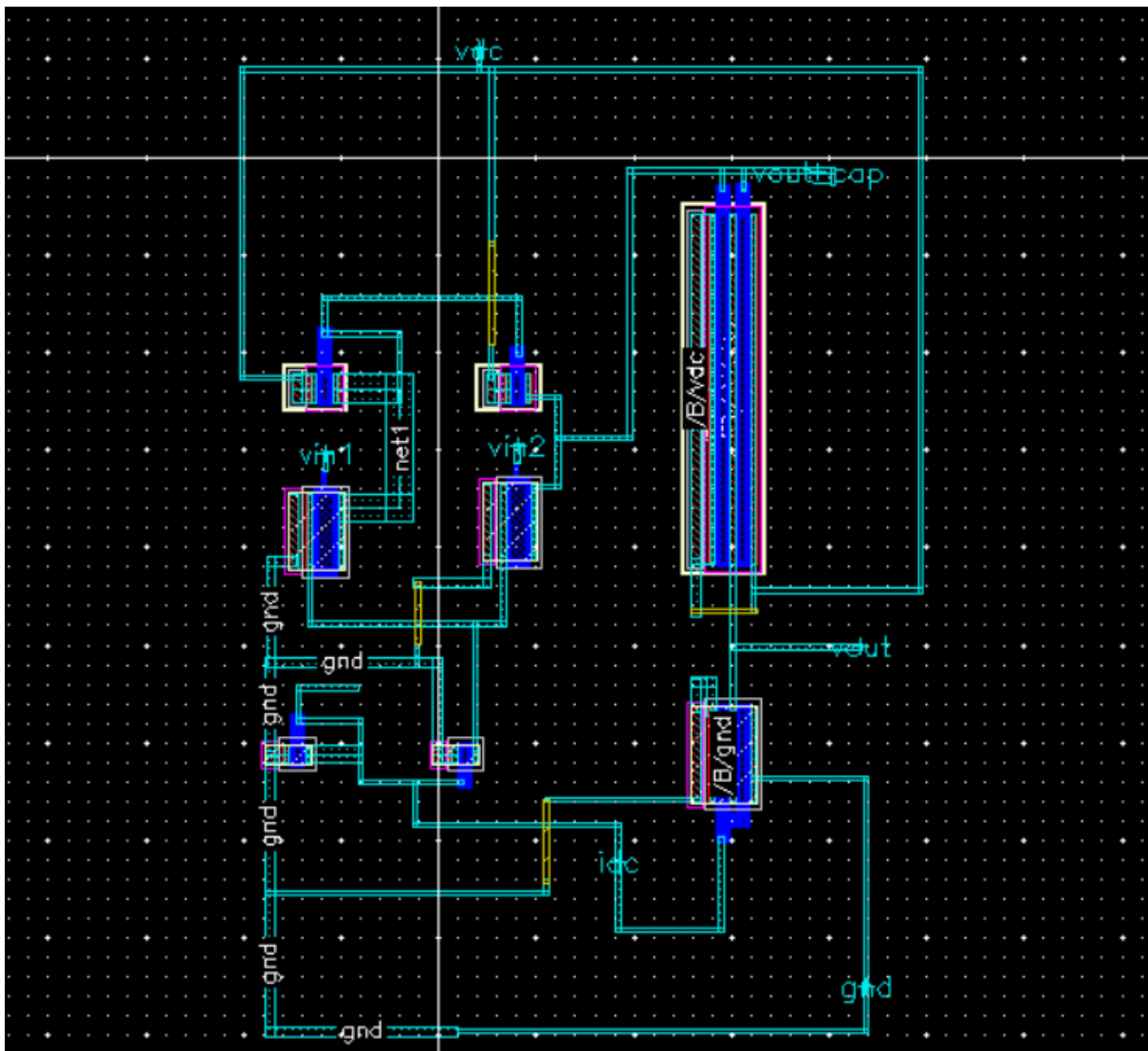
$$(w/L)_5 = 1.682 = (w/L)_8 = 1.628 \approx 1.6$$

$$(w/L)_A = 19.939$$





LAYOUT:



DRC ERRORS:

Filter: Show Unresolved OTA, 7 Results (in 7 of 353 Checks)

Check / Cell	R	1
✖ Check P.O.R.3	1	
✖ Check M1.R.1	1	
✖ Check M2.R.1	1	
✖ Check M3.R.1	1	
✖ Check M4.R.1	1	
✖ Check M5.R.1	1	
✖ Check UTM40K.R.1	1	

P.O.R.3 [0 Min poly area coverage < 14%
 ALL_POLY = POLY1 OR DPO
 DENSITY ALL_POLY < 0.14 PRINT POLY_DENSITY.log
 }

In the above DRC report only density errors are presented which can be ignored.

LVS REPORT:

```

REPORT FILE NAME:      OTA.lvs.report
LAYOUT NAME:          /Design/MTECH/MTECH2021/EE_GRP12/Desktop/cadence_24/OTA.sp ('OTA')
SOURCE NAME:          /Design/MTECH/MTECH2021/EE_GRP12/Desktop/cadence_24/OTA.src.net ('OTA')
RULE FILE:            /Design/MTECH/MTECH2021/EE_GRP12/Desktop/cadence_24/_calibre.lvs_
CREATION TIME:        Sun Mar 24 01:43:38 2024
CURRENT DIRECTORY:    /Design/MTECH/MTECH2021/EE_GRP12/Desktop/cadence_24
USER NAME:            EE_GRP12
CALIBRE VERSION:      v2019.4_16.9   Tue Oct 1 16:24:54 PDT 2019

OVERALL COMPARISON RESULTS

# # # # #
# # CORRECT # # #
# # # # #

*****
CELL SUMMARY
*****

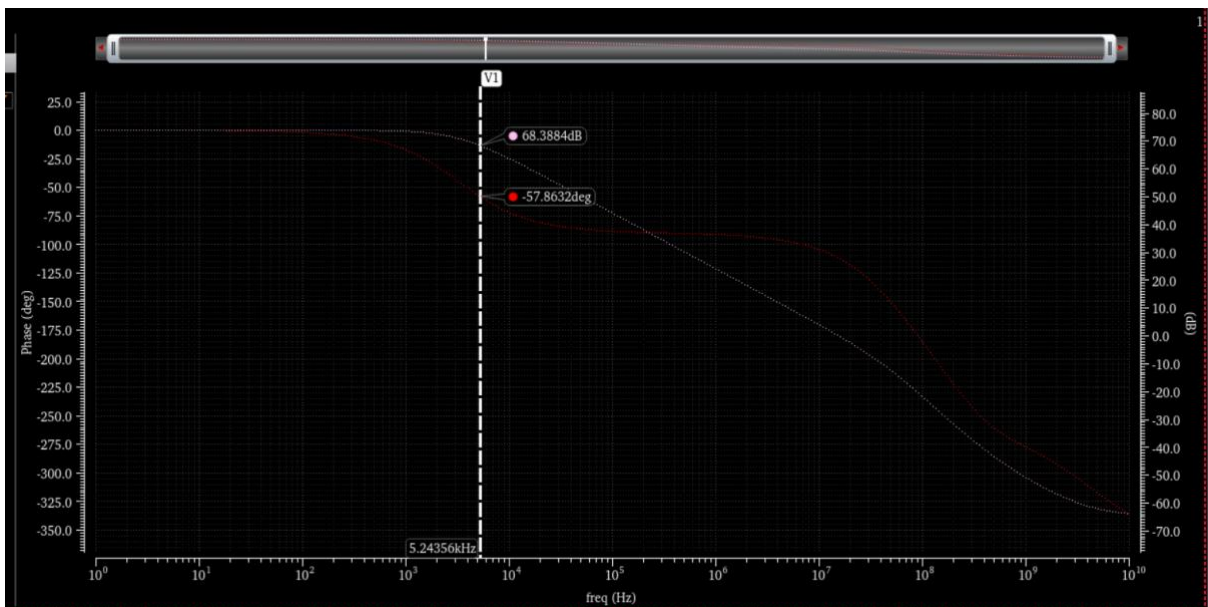
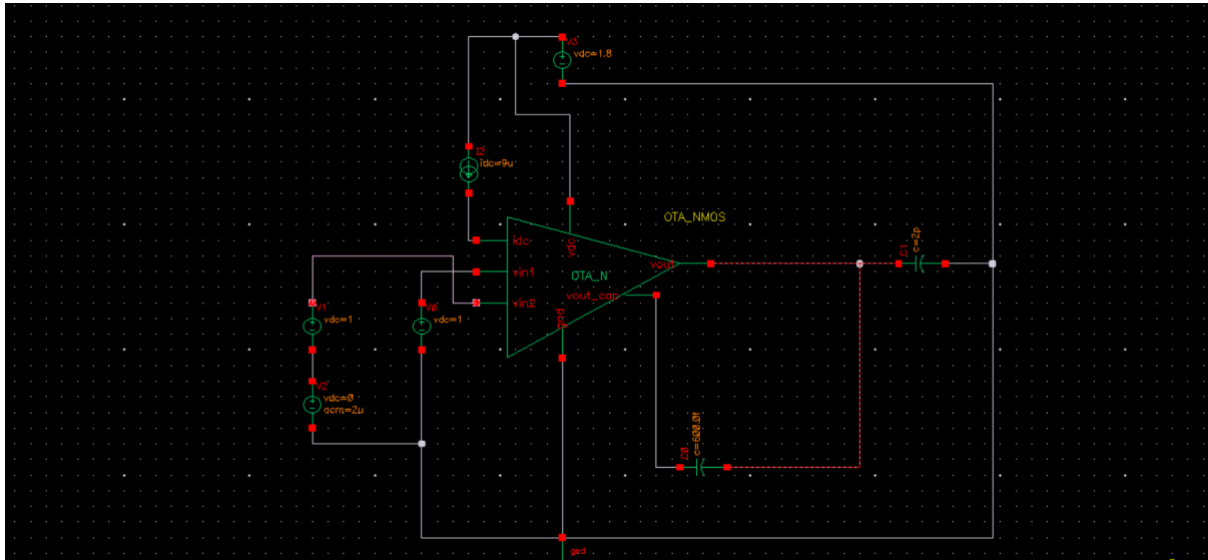
Result----- Layout----- Source-----
CORRECT      OTA             OTA

*****
LVS PARAMETERS
*****

o LVS Setup:
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
// LVS PIN NAME PROPERTY
LVS POWER NAME      "AVD33" "AVD33B" "AVD33G" "AVD33R" "AVD33WELL" "AVDD" "AVDD8" "AVDD8G" "AVDDG" "AVDDR"
                    "AVDWELL" "DVDD" "TAVD33" "TAVD33PST" "TAVDD" "TAVDDPST" "VD33" "VD33WELL" "VDD" "VDD5V"
                    "VDDG" "VDDM" "VDDPST" "VDDSA" "VDWELL"
LVS GROUND NAME     "AGND" "AVS33" "AVS33B" "AVS33G" "AVS33R" "AVS33SUB" "AVSS" "AVSSB" "AVSSBG" "AVSSG"
                    "AVSSR" "AVSSUB" "DVSS" "GND" "TAVSS" "TAVSSPST" "VS33" "VS33SUB" "VSS" "VSSG" "VSSM"
                    "VSSPST" "VSSUB"
LVS CELL SUPPLY     LVS
  
```

The layout and schematic are matched.

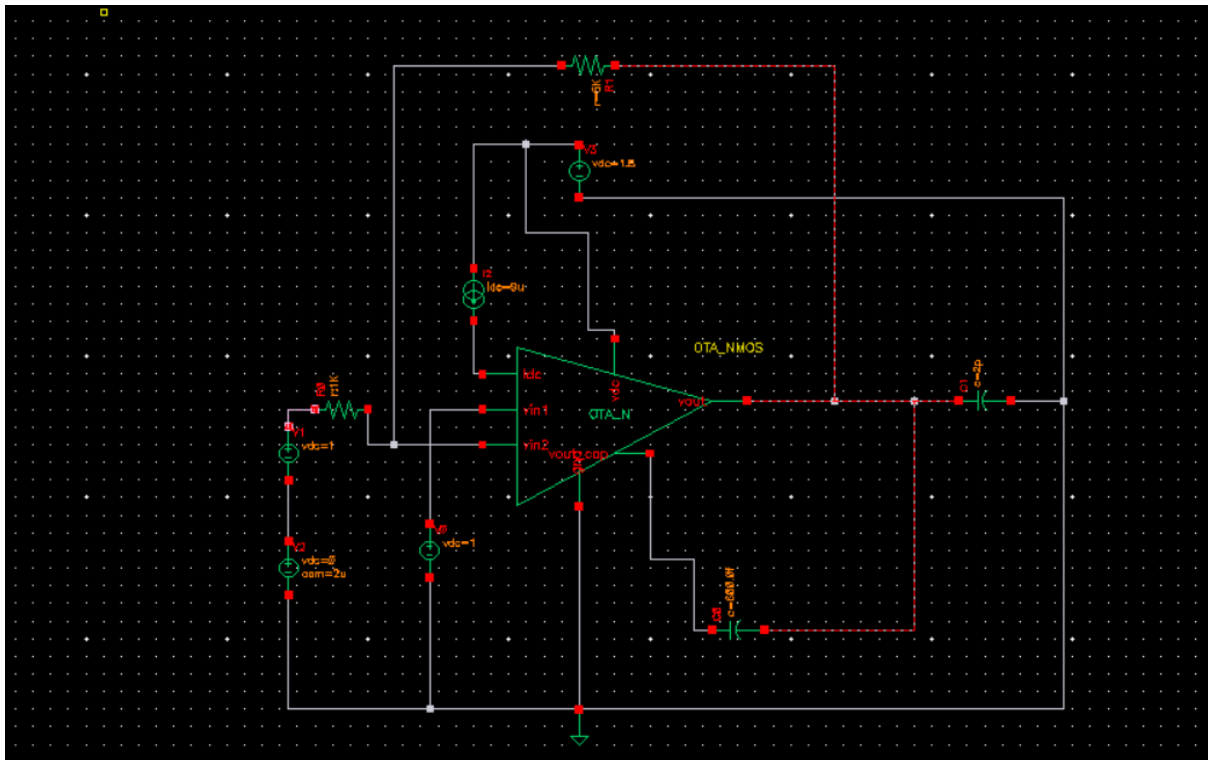
TEST_BENCH:

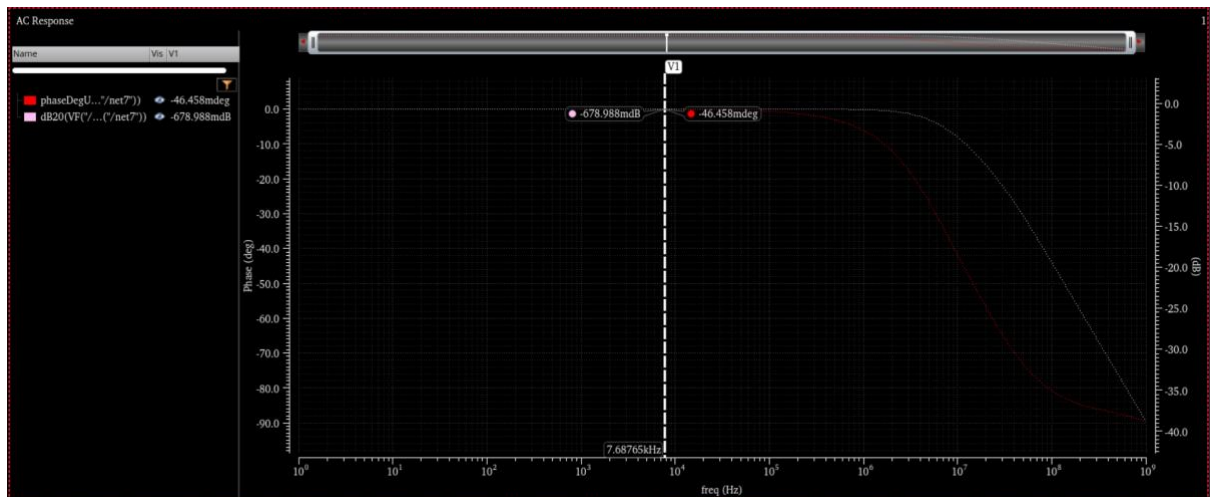


Pex report:

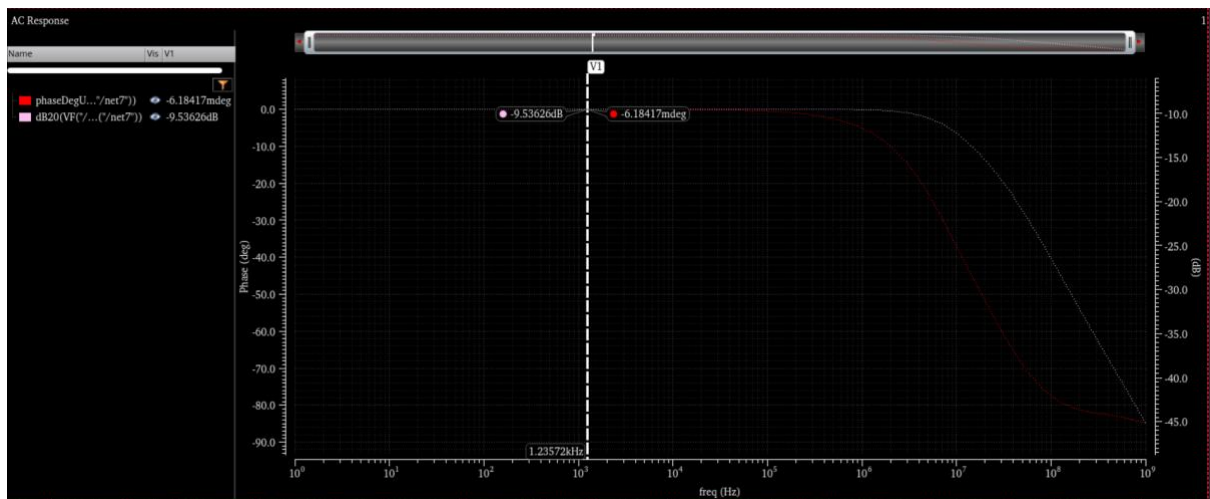
OTA				
No.	Layout Net	Source Net	R Count	C Total (F)
1	ldc	ldc	42	4.5353E-15
2	2	NET1	34	3.8996E-15
3	vin1	VIN1	9	3.9277E-16
4	vin2	VIN2	9	3.8555E-16
5	vout_cap	VOUT_CAP	42	3.5081E-15
6	gnd	GND	121	1.1631E-14
7	vdc	VDC	130	1.0817E-14
8	vout	VOUT	42	1.0765E-15
9	9	NET2	24	1.7553E-15
CC Total (F)				
7.6310E-16				
C+CC Total (F)				
5.8023E-15				
C+CC Total (F)				
4.2600E-15				
C+CC Total (F)				
7.2083E-16				
C+CC Total (F)				
5.1738E-15				
C+CC Total (F)				
1.3242E-14				
C+CC Total (F)				
1.3518E-14				
C+CC Total (F)				
3.5815E-15				
C+CC Total (F)				
2.7482E-15				

With feedback gain 5

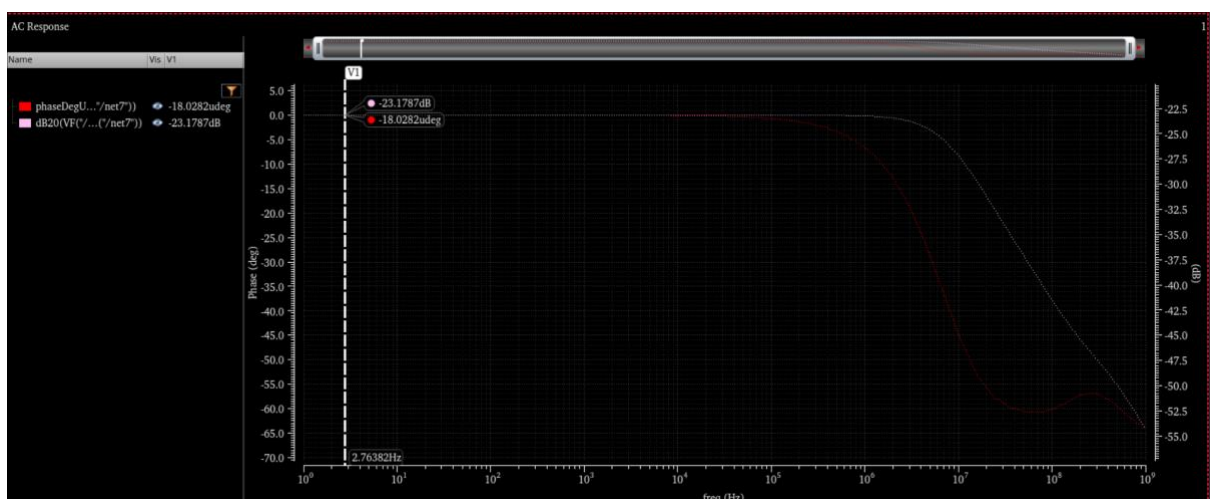




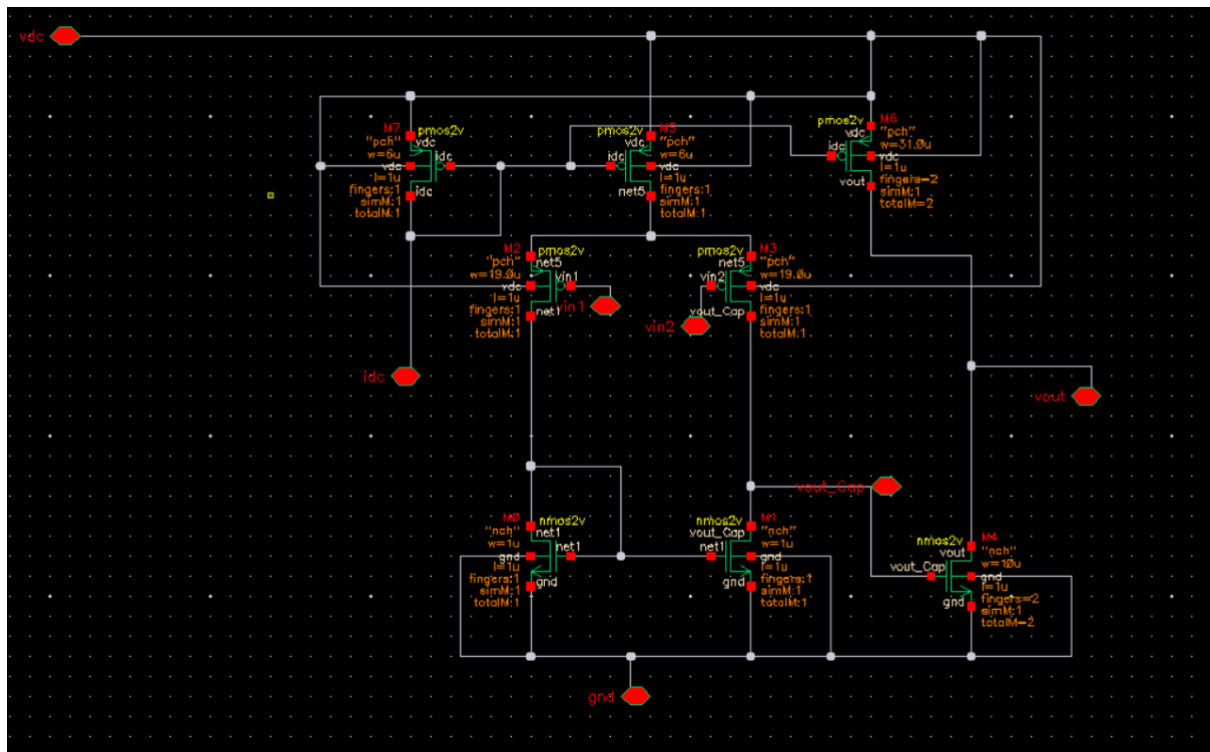
With feedback gain 10



With feedback gain 20:

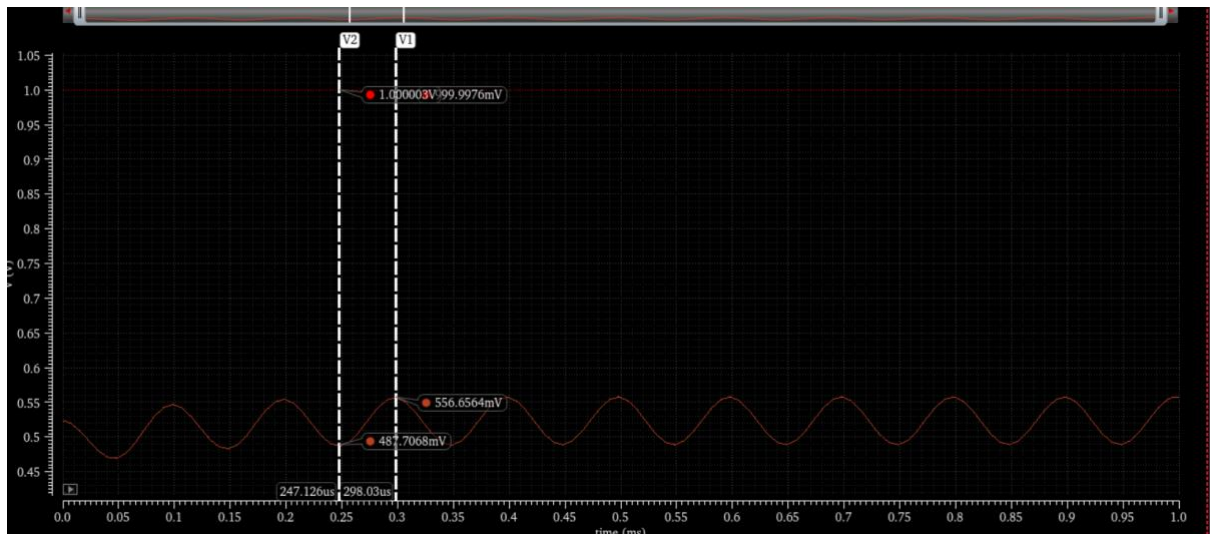


PMOS_OTA:

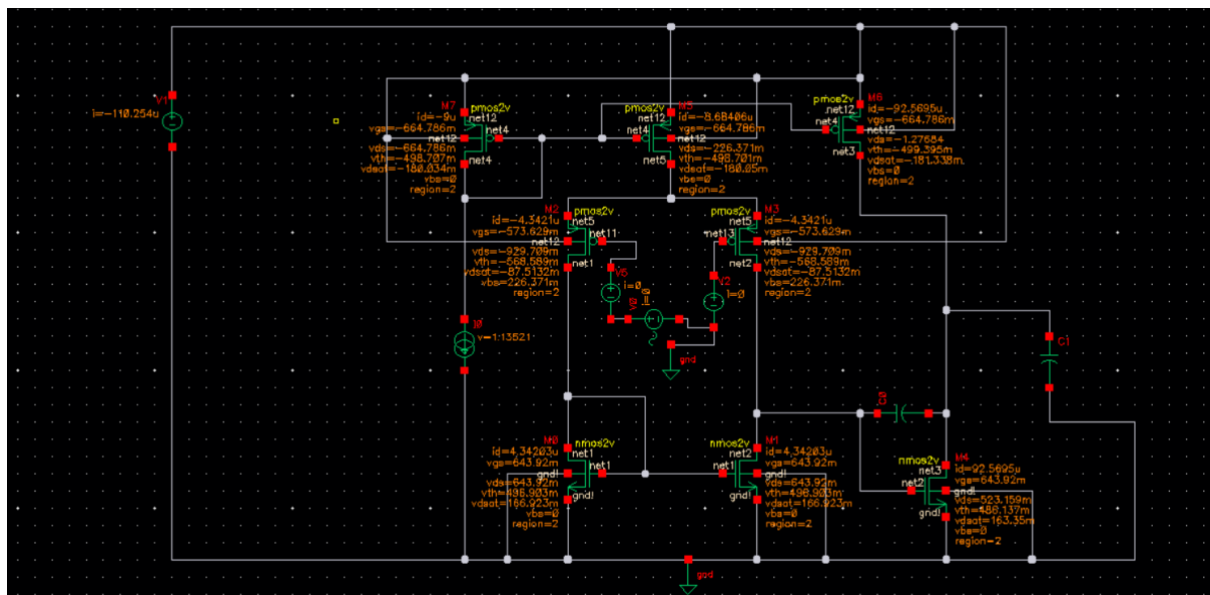


All the transistors are in region 2(saturation region).

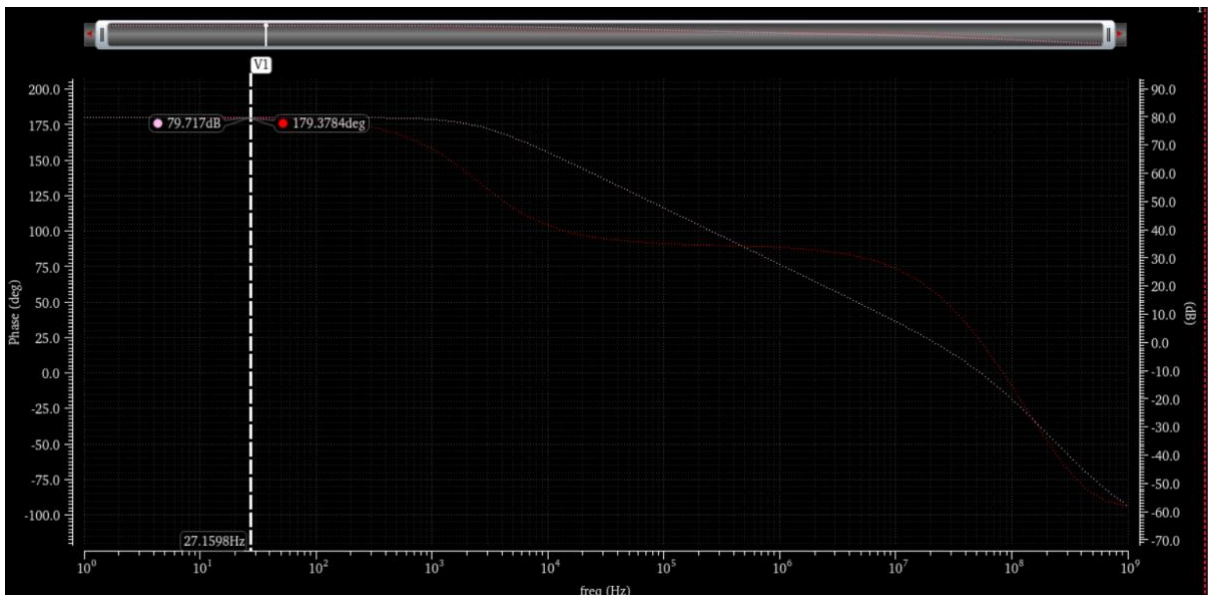
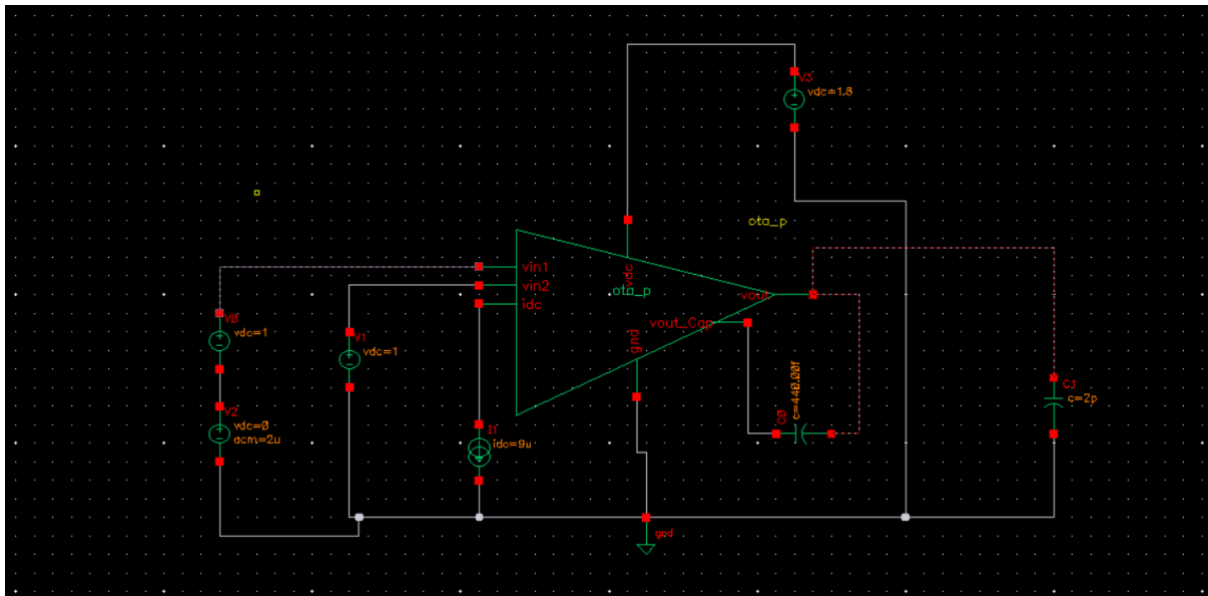
TRANSIENT RESPONSE:



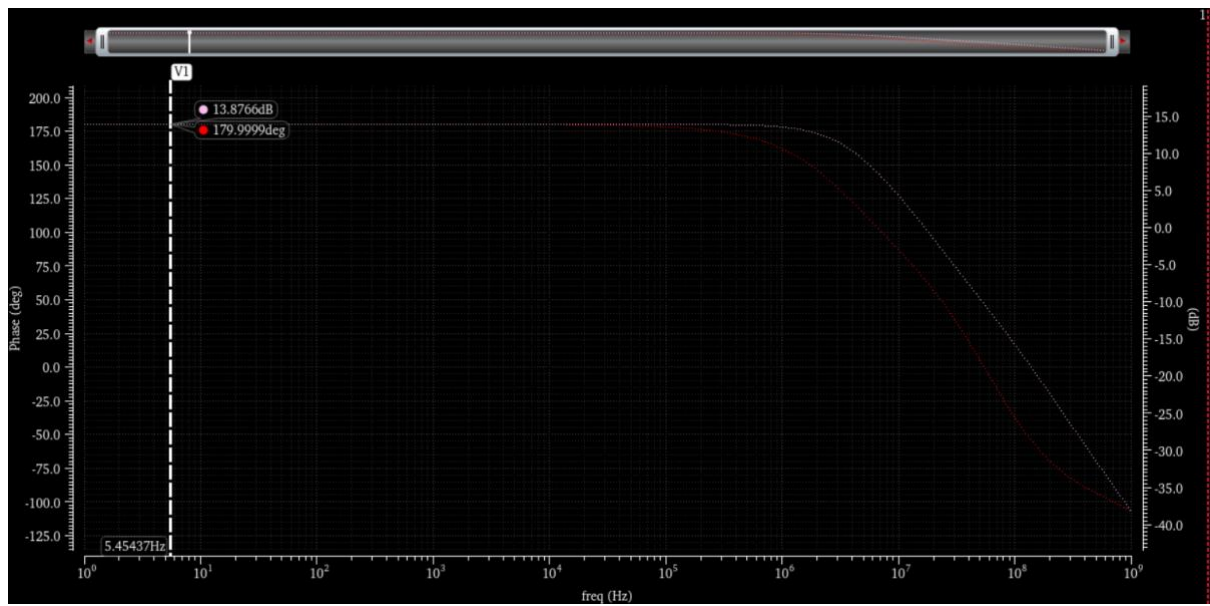
SCHEMATIC:



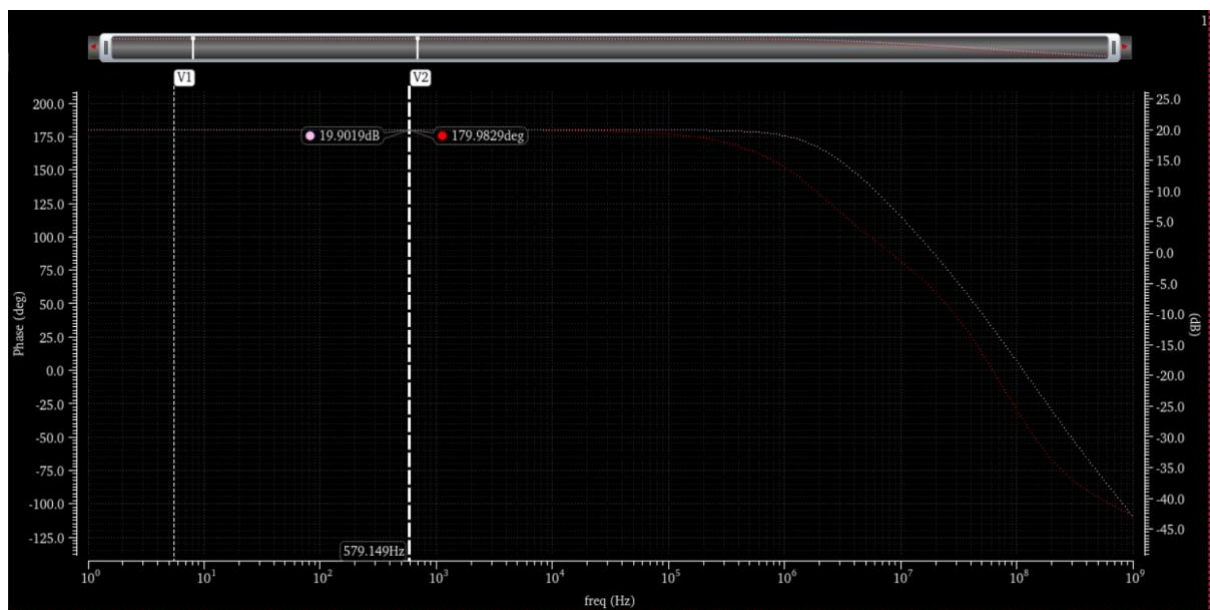
TEST_BENCH:



With gain=5



With gain=10



With gain=15

