Started on	Wednesday, 21 October 2020, 4:00 PM
State	Finished
Completed on	Wednesday, 21 October 2020, 4:59 PM
Time taken	59 mins 15 secs
Grade	**8.50** out of 20.00 (**43**%)

Question **1**

Incorrect

Mark 0.00 out of 1.00

Consider the following BCD numbers A=(0111 0100 1001 1001), B=(0001 1001 1000 0110) involved in BCD addition. Finally how many times BCD adder sets carry flag and adds zero value to convert the sum into BCD are _____,_____.

- 1. 3, 2
- 2. 3, 1
- 3. 4, 1 ✖
- 4. 4, 0

Your answer is incorrect.

The correct answer is:
3, 1

Question **2**

Correct

Mark 1.00 out of 1.00

A combinational circuit is designed to find at least four progressive ones in the 8-bit input. The output logic expression for such a design is

- [ ] 1. These are not valid output logic expressions for the given design.
- [ ] 2. pqr+qrs+rst+stu+tuv+uvw
- [x] 3. pqrs+qrst+rstu+stuv+tuvw
- [ ] 4. p'q'r's'+tuvw+ p'q'tu+r's'vw+pqrs

Your answer is correct.

The correct answer is: pqrs+qrst+rstu+stuv+tuvw

Question **3**

Not answered

Marked out of 1.00

Consider the Boolean expression F(A,B,C)=∑m(1,2,3,4,5,6). Use Petrick's method to simplify the expression and the simplified SOP of PI terms is P =_____.(Note: Collect PI terms from left to right in K-MAP and assign names like P1, P2,... etc.)

- [ ] 1. P1P3P6+P1P2P3P6+P1P2P4P5+P2P3P5P6+P2P4P6
- [ ] 2. None of these.
- [ ] 3. P1P3P4P6+P1P2P4P5+P2P3P5P6+P2P4P6+P1P3P5
- [ ] 4. P1P2P5+P1P3P6+P1P2P3P6+P1P2P4P5+P2P3P5P6

Your answer is incorrect.

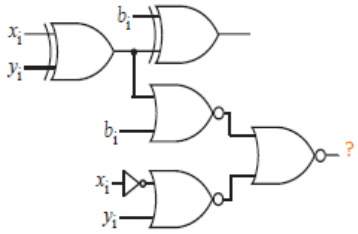
The correct answer is:
P1P3P4P6+P1P2P4P5+P2P3P5P6+P2P4P6+P1P3P5

Question **4**

Incorrect

Mark 0.00 out of 1.00

What is the logic expression at ? in the logic circuit given below and is used in _____



- 1. $[(x_i \oplus y_i) + b_i](x_i + y_i')$, adder circuit
- 2. $[(x_i \oplus y_i) + b_i](x_i' + y_i)$, adder circuit ✖
- 3. $[(x_i \oplus y_i) + b_i](x_i' + y_i)$, subtractor circuit
- 4. $[(x_i \oplus y_i) + b_i](x_i + y_i')$, subtractor circuit

Your answer is incorrect.

The correct answer is:
$[(x_i \oplus y_i) + b_i](x_i' + y_i)$, subtractor circuit

Question **5**

Incorrect

Mark 0.00 out of 1.00

The components of the digital logic module in Verilog are nonconcurrent functionality.

Select one:

- True ✖
- False

The correct answer is 'False'.

Question **6**

Not answered

Marked out of 2.00

Design a combinational logic circuit to accept four inputs A, B, C, D, and produces three outputs X, Y, Z. The outputs of each combination are to find the number of nulls (0s) in each input sequence. What are the output logic expressions?

- A'B'C'D', A'B'D + A'C'D + A'CD' + B'CD' + BC'D' + AB'C', A'B'C'D + A'B'CD + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D + ABCD'
- A'B'C'D', A'B'D + A'C'D + A'CD' + B'CD' + BC'D' + AB'C', A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D + ABCD'
- A'B'C'D', A'B'D + A'C'D + A'CD' + B'CD' + BC'D' + AB'C', A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D + ABCD
- A'B'C'D', A'B'D + A'C'D + A'CD' + B'CD + BC'D' + AB'C', A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D + ABCD'

Your answer is incorrect.

The correct answer is:
A'B'C'D', A'B'D + A'C'D + A'CD' + B'CD' + BC'D' + AB'C', A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D + ABCD'

Question **7**

Correct

Mark 1.00 out of 1.00

Consider the table to convert numbers from BCD to Excess 4 code. After simplification of Boolean expression of Y, and Z are _____,_____.

BCD				Excess 4			
A	B	C	D	X	Y	Z	W
0	0	0	0	0	1	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1

- [x] 1. Y=B', Z=C
- [ ] 2. Y=B, Z=C'
- [ ] 3. Y=B', Z=C'
- [ ] 4. Y=B, Z=C

Your answer is correct.

The correct answer is:
Y=B', Z=C

Question **8**

Correct

Mark 1.00 out of 1.00

Simplify the following Boolean expression F(A,B,C,D)=

∑m(4,5,8,9,11,12) using prime implicant chart. The simplified expression is F=_____.

- [x] 1. A'BC'+AB'D+AC'D'
- [ ] 2. A'BC'+AB'D+AC'D
- [ ] 3. A'BC'+ABD+AC'D'
- [ ] 4. ABC'+AB'D+AC'D'

Your answer is correct.

The correct answer is:
A'BC'+AB'D+AC'D'

Question **9**

Not answered

Marked out of 1.00

WXY' + W'Y'X + (W'Y')' X' + (Y ⊕ WZ) is euivalent to

- [ ] 1. W'X + X'Y + XZ' + WY
- [ ] 2. W'Y + WX' + WZ' + XY'
- [ ] 3. W'X + XY' + WZ + WY'
- [ ] 4. YZ' + W'X + XY' + WY'

Your answer is incorrect.

The correct answers are:
W'Y + WX' + WZ' + XY',

YZ' + W'X + XY' + WY'

Question **10**

Correct

Mark 1.00 out of 1.00

Find the valid option(s) regarding Time Division Multiplexers (TDM).

i) Multiple data transmission using a single medium.

ii) At a time multiple data transmissions happened.

iii) Multiple parties can have data transmissions at distinct intervals.

- [x] 1. i, iii
- [ ] 2. ii, iii
- [ ] 3. All of these
- [ ] 4. i, ii

Your answer is correct.

The correct answer is:
i, iii

Question **11**

Correct

Mark 1.00 out of 1.00

Consider the Boolean expression F(A,B,C,D)= ∑m(5,6,7,9,10,11,13,14). Simplify the above Boolean expression by using Cyclic Prime Implicant Chart (CPIC) and the simplified expression is F=_____(Note: The PI term is deleted at first step in CPIC is having smallest sum of minterms that formed the PI).

- 1. AB'D+BCD'+AB'C+AC'D
- 2. A'BD+ B'CD'+AB'C+AC'D
- 3. A'BD+BCD'+AB'C+AC'D ✔
- 4. A'BD+BCD'+AB'C+A'C'D

Your answer is correct.

The correct answer is:
A'BD+BCD'+AB'C+AC'D

Question **12**

Not answered

Marked out of 1.00

Identify the invalid statement(s) of the following concerning the cyclic Boolean functions.

i) It contains equal size PI terms, and the number of PI terms is equal to the number of implicants.

ii) It will generate a unique Boolean expression after simplification of a cyclic boolean expression.

iii) EPI terms are present in cyclic Boolean functions.

- 1. None of these
- 2. i, ii, iii
- 3. ii, iii
- 4. i, iii

Your answer is incorrect.

The correct answer is:
ii, iii

Question **13**

Partially correct

Mark 0.50 out of 1.00

Test bench of a Verilog module is

- 1. a file that has no real inputs or outputs
- 2. to generates stimulus to drive the MUT ✔
- 3. valid code to get the real logic circuit
- 4. real circuit to be synthesized

Your answer is partially correct.

You have correctly selected 1.
The correct answers are:
a file that has no real inputs or outputs,

to generates stimulus to drive the MUT

Question **14**

Correct

Mark 1.00 out of 1.00

Select the correct choice(s) of the following statements concerning Verilog and VHDL

1. Verilog and VHDL are HDLs.
2. Modules of both HDLs are nonsynthesizable.
3. Both are General purpose HDLs.
4. Both are used as the industry standard HDLs

- [x] 1. 1, 3, 4 are valid statements
- [ ] 2. *1, 2, 3 are valid statements*
- [ ] 3. *2, 3, 4 are valid statements*
- [ ] 4. *1, 2, 4 are valid statements*

Your answer is correct.

The correct answer is:
1, 3, 4 are valid statements

Question **15**

Not answered

Marked out of 1.00

Identify the invalid statement(s) from the following statements.

i) Petrick’s method doesn’t handle cyclic boolean expressions.

ii) Cyclic Prime Implicant Chart method is easier than Petrick's method.

iii) Petrick’s method is tedious to implement on a computer.

1. i, ii
2. None of these
3. i, iii
4. i, ii, iii

Your answer is incorrect.

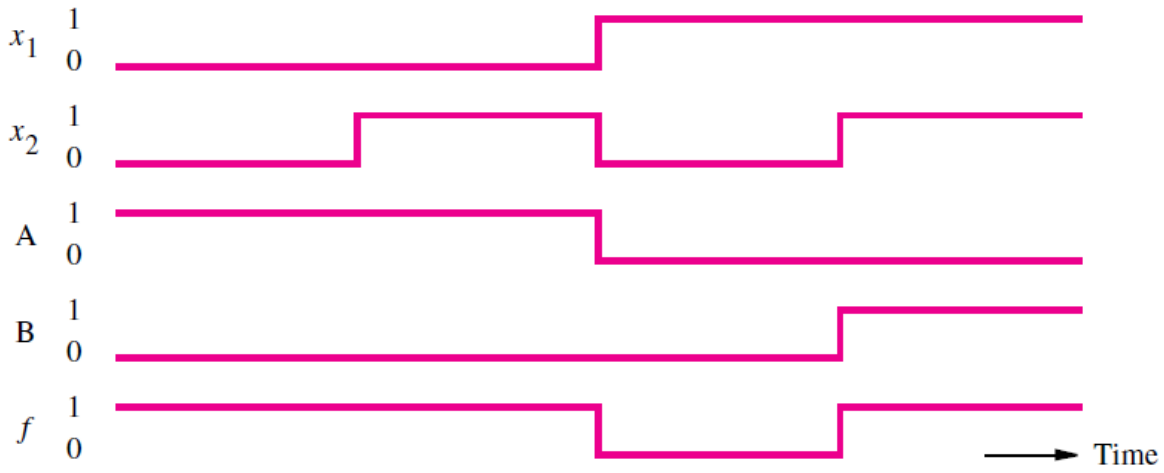
The correct answer is:
i, iii

Question **16**

Correct

Mark 1.00 out of 1.00

Concerning the following timing diagram, x_1, x_2 are inputs, and A, B are intermediate results and inputs for some logic gate. Analyze the logic expression for f.



- [x] 1. $x_1' + x_1 . x_2$
- [x] 2. $x_1' + x_2$
- [ ] 3. $x_1' + x_2'$
- [ ] 4. $x_1 + x_2'$

Your answer is correct.

The correct answers are:

$x_1' + x_1 . x_2$, $x_1' + x_2$

Question **17**

Correct

Mark 1.00 out of 1.00

A digital logic function ***X*** with variable ***a*** can build different Boolean functions. Choose the appropriate outputs of built digital functions.

- 1. a'+a' ✔
- 2. a+a ✔
- 3. a'+a ✔
- 4. a+a' ✔

Your answer is correct.

The correct answers are:
a'+a',

a'+a,

a+a',

a+a

Question **18**

Incorrect

Mark 0.00 out of 1.00

Identify the TRUE statements from the following statement/statements.

i) Encoder handles multiple inputs at a time and yields the correct result.

ii) Priority encoders handle multiple inputs with priority.

iii) Encoders do not create any ambiguity for all inputs.

- 1. i
- 2. i, ii
- 3. ii
- 4. i, ii, iii ✖

Your answer is incorrect.

The correct answer is:
ii

Question **19**

Not answered

Marked out of 1.00

Consider the following Boolean expression F(A,B,C,D)=∑m(1,2,5,8,9,10)+∑d(3,11,13). Simplify the Boolean expression by using the Quine-McCluskey algorithm and Find the total number of terms and number of redundant term/terms among all terms are found in second round are_____,_____.

- 1. 7, 3
- 2. 8, 3
- 3. 7, 4
- 4. 8, 4

Your answer is incorrect.

The correct answer is:
8, 4

◄ LD_Class18

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