**ASSIGNMENT 1: BEHAVIOURAL MODELLING**

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1.

module INVERTER\_B\_MOD(out,in);

output out;

input in;

reg out;

always@(in)

begin

out=~in;

end

endmodule

2.

module and\_gate\_b\_mod(y,a,b);

output reg y;

input a,b;

always@(a,b)

begin

y=a&b;

end

endmodule

3.

module or\_bmod(y,a,b);

output reg y;

input a,b;

always@(a,b)

begin

y=a|b;

end

endmodule

4.

module nand\_bahave(y,a,b);

input a,b;

output y;

reg y;

always@(a,b)

begin

y=~(a&b);

end

endmodule

5.

module nor\_behave(y,a,b);

input a,b;

output reg y;

always@(a,b)

begin

y=~(a|b);

end

endmodule

6.

module xor\_behave(y,a,b);

output reg y;

input a,b;

always@(a,b)

begin

y=(a^b);

end

endmodule

7.

module xnor\_behave(y,a,b);

input a,b;

output reg y;

always@(a,b)

begin

y=~(a^b);

end

endmodule

8.

module nor\_input\_behave(y,a,b,c,d,e,f,g,h);

input a,b,c,d,e,f,g,h;

output reg y;

always@(a,b,c,d,e,f,g,h)

begin

y=~(a|b|c|d|e|f|g|h);

end

endmodule

9.

module nand\_input\_behave(y,a,b,c,d,e,f,g,h);

output reg y;

input a,b,c,d,e,f,g,h;

always@(a,b,c,d,e,f,g,h)

begin

y=~(a&b&c&d&e&f&g&h);

end

endmodule

10.

module inverterarray\_behave(y,a);

output reg[15:0] y;

input[15:0] a;

always@(a)

begin

y=~a;

end

endmodule

11.

module andarray\_behave(y,a,b);

output reg[15:0] y;

input[15:0] a,b;

always@(a,b)

begin

y=(a&b);

end

endmodule

12.

module orarray\_behave(y,a,b);

output reg[16:1] y;

input[16:1] a,b;

always@(a,b)

begin

y=a|b;

end

endmodule

13.

module nandarray\_behave(y,a,b);

output reg[15:0] y;

input[15:0] a,b;

always@(a,b)

begin

y=~(a&b);

end

endmodule

14.

module norarray\_behave(y,a,b);

output reg[15:0] y;

input[15:0] a,b;

always@(a,b)

begin

y=~(a|b);

end

endmodule