**ASSIGNMENT 1: DATAFLOW MODELLING**

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1.

module inverter\_dataflow(out\_1,in\_1);

output out\_1;

input in\_1;

assign out\_1=~in\_1;

endmodule

2.

module and\_gate\_dataflow(input a,b, output y);

assign y=a&b;

endmodule

3.

module or\_gate\_dataflow(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

assign y\_out=a\_in|b\_in;

endmodule

4.

module nand\_dataflow(y\_out,a\_in,b\_in);

output y\_out;

input a\_in,b\_in;

assign y\_out=~(a\_in&b\_in);

endmodule

5.

module nor\_dataflow(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

assign y\_out=~(a\_in|b\_in);

endmodule

6.

module xor\_dataflow(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

assign y\_out=(a\_in^b\_in);

endmodule

7.

module xnor\_dataflow(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

assign y\_out=~(a\_in^b\_in);

endmodule

8.

module nor\_input\_dataflow(y,a,b,c,d,e,f,g,h);

input a,b,c,d,e,f,g,h;

output y;

assign y=~(a|b|c|d|e|f|g|h);

endmodule

9.

module nand\_input\_dataflow(y,a,b,c,d,e,f,g,h);

input a,b,c,d,e,f,g,h;

output y;

assign y=~(a&b&c&d&e&f&g&h);

endmodule

10.

module inverterarray\_dataflow(y\_out,a\_in);

output[15:0] y\_out;

input[15:0] a\_in;

assign

y\_out=~a\_in;

endmodule

11.

module andarray\_dataflow(y\_out,a\_in,b\_in);

output[16:1] y\_out;

input[16:1] a\_in,b\_in;

assign

y\_out=a\_in&b\_in;

endmodule

12.

module orarray\_dataflow(y\_out,a\_in,b\_in);

output[15:0] y\_out;

input[15:0] a\_in,b\_in;

assign y\_out=a\_in|b\_in;

endmodule

13.

module nandarray\_dataflow(y\_out,a\_in,b\_in);

output[17:2] y\_out;

input[17:2] a\_in,b\_in;

assign

y\_out=~(a\_in&b\_in);

endmodule

14.

module norarray\_dataflow(y,a,b);

output[17:2] y;

input[17:2] a,b;

assign y=~(a|b);

endmodule