**ASSIGNMENT 1: GATE-LEVEL MODELLING**

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1.

module inverter\_gate\_level(out\_1,in\_1);

output out\_1;

input in\_1;

not(out\_1,in\_1);

endmodule

2.

module add\_gate\_gatelevel(y\_out,a\_in,b\_in);

input a\_in;

input b\_in;

output y\_out;

and(y\_out,a\_out,b\_out);

endmodule

3.

module or\_gate\_gatelevel(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

or(y\_out,a\_in,b\_in);

endmodule

4.

module nand\_gatelevel(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

nand(y\_out,a\_in,b\_in);

endmodule

5.

module nor\_gatelevel(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

nor(y\_out,a\_in,b\_in);

endmodule

6.

module xor\_gatelevel(y\_out,a\_in,b\_in);

output y\_out;

input a\_in,b\_in;

xor(y\_out,a\_in,b\_in);

endmodule

7.

module xnor\_gatelevel(y\_out,a\_in,b\_in);

input a\_in,b\_in;

output y\_out;

xnor(y\_out,a\_in,b\_in);

endmodule

8.

module nor\_input\_gatelevel(y\_out,a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in);

input a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in;

output y\_out;

nor(y\_out,a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in);

endmodule

9.

module nand\_input\_gatelevel(y\_out,a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in);

input a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in;

output y\_out;

nand(y\_out,a\_in,b\_in,c\_in,d\_in,e\_in,f\_in,g\_in,h\_in);

endmodule

10.

module inverterarray\_gatelevel(y\_out,a\_in);

output[16:1] y\_out;

input[16:1] a\_in;

not array\_of\_inverter[16:1](y\_out,a\_in);

endmodule

11.

module andarray\_gatelvl(y\_out,a\_in,b\_in);

output[15:0] y\_out;

input[15:0] a\_in;

input[15:0] b\_in;

and array\_of\_andgates[15:0](y\_out,a\_in,b\_in);

endmodule

12.

module orarray\_gatelevel(y\_out,a\_in,b\_in);

output[18:3] y\_out;

input[18:3] a\_in;

input[18:3] b\_in;

or array\_of\_orgates[18:3](y\_out,a\_in,b\_in);

endmodule

13.

module nandarray\_gatelvl(y\_out,a\_in,b\_in);

output[15:0] y\_out;

input[15:0] a\_in;

input[15:0] b\_in;

nand array\_of\_nandgates[15:0](y\_out,a\_in,b\_in);

endmodule

14.

module norarray\_gatelevel(y\_out,a\_in,b\_in);

output[15:0] y\_out;

input[15:0] a\_in;

input[15:0] b\_in;

nor array\_of\_norgates[15:0](y\_out,a\_in,b\_in);

endmodule