**GATELEVEL MODELLING**

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**ROLL NUMBER: B200055CS**

1.

module ASSIGNMENT\_12X1MUX(out\_y,in\_A,in\_B,selec\_S);

input in\_A, in\_B, selec\_S;

output out\_y;

wire intermid\_S\_in, intermid\_t1, intermid\_t2;

nand nand\_1\_in(intermid\_S\_in,selec\_S,selec\_S);

nand nand\_2\_in1(intermid\_t1,in\_A,intermid\_S\_in);

nand nand\_3\_in2(intermid\_t2,in\_B,selec\_S);

nand nand\_4\_final(out\_y,intermid\_t1,intermid\_t2);

endmodule

2.

module DEMUX\_GATE(y\_out,y\_out\_1,in\_y\_,in\_selec);

output y\_out,y\_out\_1;

input in\_y\_;

input in\_selec;

wire inter\_t1, inter\_t2, inv\_selec;

nand(inv\_selec,in\_selec,in\_selec);

nand(inter\_t1,in\_y\_,inv\_selec);

nand(inter\_t2,in\_y\_,in\_selec);

nand(y\_out,inter\_t1,inter\_t1);

nand(y\_out\_1,inter\_t2,inter\_t2);

endmodule

3.

module SIXTEENBIT\_MUX\_GATE(y\_out,in\_y,in\_y\_,in\_selec);

output [15:0]y\_out;

input [15:0] in\_y, in\_y\_;

input in\_selec;

wire inv\_s;

wire[15:0]inter\_t;

wire[15:0]inter\_t2;

nand nand\_1\_\_(inv\_s,in\_selec,in\_selec);

nand nand\_2\_\_[15:0](inter\_t,in\_y,inv\_s);

nand nand\_3\_\_[15:0](inter\_t2,in\_y\_,in\_selec);

nand nand\_op[15:0](y\_out,inter\_t,inter\_t2);

endmodule

4.

module mux4x1\_sixteenbitmux(out,i0,i1,i2,i3,s1,s0);

input[15:0] i0,i1,i2,i3;

input s1;

input s0;

output[15:0] out;

wire[15:0] mux1,mux2;

SIXTEENBIT\_MUX\_GATE mux\_1(mux1,i0,i1,s1);

SIXTEENBIT\_MUX\_GATE mux\_2(mux2,i2,i3,s1);

SIXTEENBIT\_MUX\_GATE mux\_3(out,mux1,mux2,s0);

endmodule

5.

module mux\_16X1\_eightbit(out\_p\_,in1,in2,in3,in4,in5,in6,in7,in8,s0,s1,s2);

output[15:0] out\_p\_;

input s0,s1,s2;

input[15:0] in1,in2,in3,in4,in5,in6,in7,in8;

wire[15:0] t1,t2;

mux4x1\_sixteenbitmux test\_1(.out(t1),.i0(in1),.i1(in2),.i2(in3),.i3(in4),.s1(s0),.s0(s1));

mux4x1\_sixteenbitmux test\_2(.out(t2),.i0(in5),.i1(in6),.i2(in7),.i3(in8),.s1(s0),.s0(s1));

ASSIGNMENT\_12X1MUX test\_3(.out\_y(out\_p\_),.in\_A(t1),.in\_B(t2),.selec\_S(s2));

endmodule

6.

module demux\_4x1(out\_1,out\_2,out\_3,out4,in\_1,in\_s1,in\_s2);

output out\_1,out\_2,out\_3,out4;

input in\_1,in\_s1,in\_s2;

wire y0,y1;

DEMUX\_GATE(.y\_out(y0),.y\_out\_1(y1),.in\_y\_(in\_1),.in\_selec(in\_s1));

DEMUX\_GATE(.y\_out(out\_1),.y\_out\_1(out\_2),.in\_y\_(y0),.in\_selec(in\_s2));

DEMUX\_GATE(.y\_out(out\_3),.y\_out\_1(out4),.in\_y\_(y1),.in\_selec(in\_s2));

endmodule

7.

module demux\_1x8\_gate(out1,out2,out3,out4,out5,out6,out7,out8,in1,ins1,ins2,ins3);

output out1,out2,out3,out4,out5,out6,out7,out8;

input in1,ins1,ins2,ins3;

wire t0,t1,t2,t3,t4,t5;

DEMUX\_GATE test\_1(.y\_out(t0),.y\_out\_1(t1),.in\_y\_(in1),.in\_selec(ins1));

DEMUX\_GATE test\_2(.y\_out(t2),.y\_out\_1(t3),.in\_y\_(t0),.in\_selec(ins2));

DEMUX\_GATE test\_3(.y\_out(t4),.y\_out\_1(t5),.in\_y\_(t1),.in\_selec(ins2));

DEMUX\_GATE test\_4(.y\_out(out1),.y\_out\_1(out2),.in\_y\_(t2),.in\_selec(ins3));

DEMUX\_GATE test\_5(.y\_out(out3),.y\_out\_1(out4),.in\_y\_(t3),.in\_selec(ins3));

DEMUX\_GATE test\_6(.y\_out(out5),.y\_out\_1(out6),.in\_y\_(t4),.in\_selec(ins3));

DEMUX\_GATE test\_7(.y\_out(out7),.y\_out\_1(out8),.in\_y\_(t5),.in\_selec(ins3));

endmodule