

PANDABOX HARDWARE USER GUIDE

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PANDABOX HARDWARE USER GUIDE

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1. PREFACE : ABOUT THIS GUIDE

This Manual accompanies the PandA Box rack and contains information about its hardware.

1.1. GUIDE CONTENTS

This manual contains the following chapters:

- Chapter 2.1: Provides an overview of the PandaBox.
- Chapter 2.2: Provides details of the PandaBox components and features on the Embedded Board.
- Appendix 3: Provides Additional resources used in this documentation

1.2. ADDITIONAL DOCUMENTATION

The Panda box electronic and mechanical design can be found on:

<https://www.ohwr.org/projects/pandabox-hw/>

The cards can be found in two variants :

- DLS: Variant of DIAMOND Synchrotron
- SOL: Variant of SOLEIL Synchrotron

1.2.1. PANDA CARRIER BOARD SCHEMATIC

DIAMOND Variant :

https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_Carrier/PANDA_CARRIER_ASS%23DLS%2301.pdf

SOLEIL Variant :

https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_Carrier/PANDA_CARRIER_ASS%23SOL%2302.pdf

1.2.2. PANDA CARRIER BOARD PLACEMENT

The board placement can be found in files ASS#DLS#01_TOP.pdf and ASS#DLS#01_BOTTOM.pdf of the following archive:

https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_Carrier/PANDA_CARRIER_GERBER.zip

1.2.3. *PANDA FRONT BOARD SCHEMATIC*

DIAMOND Variant :

[https://www.ohwr.org/project/pandabox-](https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23DLS%2301.pdf)

[hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23DLS%2301.pdf](https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23DLS%2301.pdf)

SOLEIL Variant :

[https://www.ohwr.org/project/pandabox-](https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23SOL%2301.pdf)

[hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23SOL%2301.pdf](https://www.ohwr.org/project/pandabox-hw/blob/master/PandA_front_Board/PANDA_FRONT_BOARD_ASS%23SOL%2301.pdf)

1.2.4. *ENCODER-DAUGHTER-CARD SCHEMATIC*

DIAMOND Variants :

[https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23DLS%2301.pdf)

[Card/panda-encoder-module-ASS%23DLS%2301.pdf](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23DLS%2301.pdf)

[https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23DLS%2303_MONITOR.pdf)

[Card/panda-encoder-module-ASS%23DLS%2303_MONITOR.pdf](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23DLS%2303_MONITOR.pdf)

SOLEIL Variant :

[https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23SOL%2301.pdf)

[Card/panda-encoder-module-ASS%23SOL%2301.pdf](https://www.ohwr.org/project/pandabox-hw/blob/master/Encoder-Daughter-Card/panda-encoder-module-ASS%23SOL%2301.pdf)

1.2.5. *PICOZED 7Z030 HARDWARE USER GUIDE*

[PicoZed 7015/7030 HW Users Guide v2.0](#)

1.2.6. *7 SERIES FPGAs GTX/GTH TRANSCEIVERS USER GUIDE*

https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf

1.3. ADDITIONAL SUPPORT RESOURCES

2. PANDABox RACK

2.1. OVERVIEW

PandA Motion Project is a collaboration between SOLEIL and DIAMOND to upgrade their “Position and Acquisition” processing platform. PandA will provide a common encoder processing platform based on Zynq 7030 and supporting multiple encoder standards (incremental, SSI, BISS...). It will deliver synchronous triggering and data capture capabilities.

PandaBOX being developed for both Soleil and Diamond two variants of the same Carrier board has been done.

2.1.1. FEATURES

The PandaBox provides the following Features:

- SOC via Avnet picoZed xcZ7030
- 4x Encoders Inputs / outputs
- Multi-Channel TLL and LVDS Inputs/outputs with Led status
- LPC - FMC connector (optional board)
- External clock
- 3 SFP
- 1 Gigabit Ethernet for Control and DAQ
- Slow control via SPARTAN-6 with PROM
- RS232 UART ARM terminal
- USB host
- JTAG
- Status LED
- On board clock tree
- On-Board Temperature sensors
- On-Board voltage monitoring
- On-Board Fan tachymeter
- On board compact flash

2.1.2. BLOCK DIAGRAM

Figure 1 shows a high-level block diagram of the PandaBOX and its peripherals.

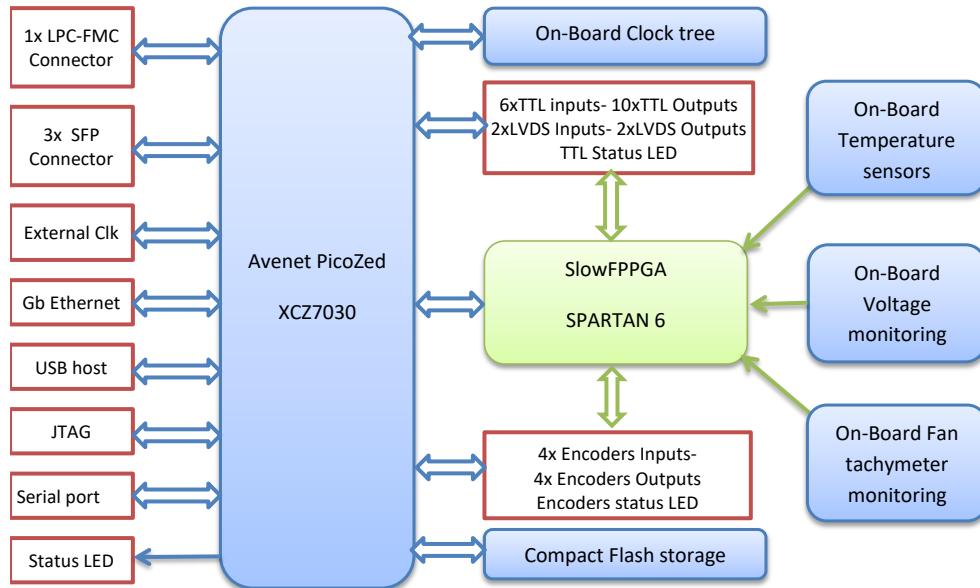


FIGURE 1: PANDABOX HIGH-LEVEL BLOCK DIAGRAM

2.1.3. DESCRIPTION

The pandaBox consist of a 1U rack composed of:

- 130W power supply
- PandA carrier Board
 - Avnet picozed zynq 7030 board support
 - Up to 4 PandA Encoder daughter board support
 - LPC FMC (optional) daughter board support
 - PandA Front panel daughter board support

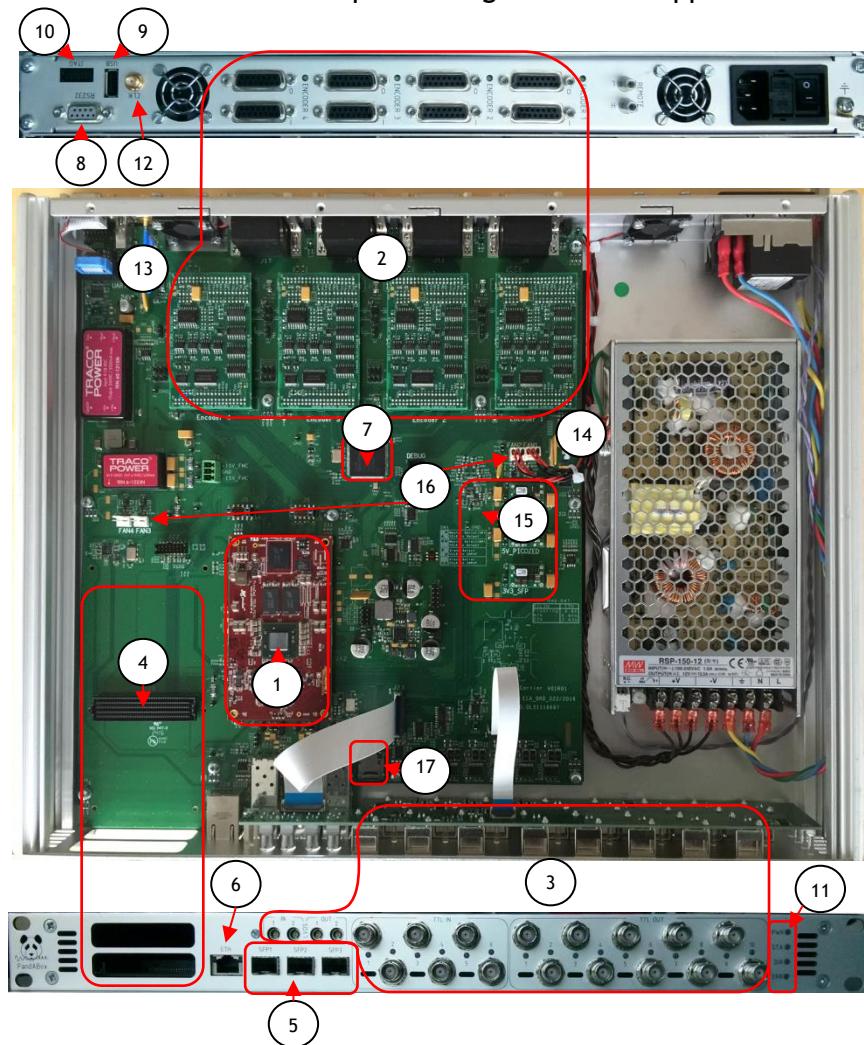


FIGURE 2: PANDABOX INSIDES PHOTO

Features' number are listed in Table 1 providing general listing of the board features and Page numbers of Carrier Board Schematic

Details are provided in §Detailed Description starting page 11.

TABLE 1 : PANDABOX FEATURES

Number	Feature	Notes	Carrier Board Schematic Page
1	SOC via Avnet picoZed xcZ7030	§2.2.1	4, 6
2	4x Encoders Inputs / outputs	§2.2.2	9,10,11,12
3	Multi-Channel TLL and LVDS Inputs/outputs with Led status	§2.2.3	14,15,16,17
4	LPC - FMC connector (optional board)	§2.2.4	13
5	3 SFP	§2.2.5	18,19,20,21
6	1 Gigabit Ethernet for Control and DAQ	§2.2.6	22
7	Slow control via SPARTAN-6 with PROM	§2.2.7	7, 8
8	RS232 UART ARM terminal	§2.2.8	25
9	USB host	§2.2.9	29
10	JTAG	§2.2.10	26
11	Status LED	§2.2.11	14
12	External clock	§2.2.12	5
13	On board clock tree	§2.2.13	5
14	On-Board Temperature sensors	§2.2.14	27
15	On-Board voltage monitoring	§2.2.15	28
16	On-Board Fan tachymeter	§2.2.16	23
17	On board compact flash	§2.2.17	24

2.2. DETAILED DESCRIPTION

2.2.1. SOC VIA AVNET PICOZED xcZ7030

PandaBOX hosts the Avnet picoZed xcZ7030 daughter board.
PicoZed daughter board can be considered in two environments.
For Processor Side see Figure 3
For Logic Side see Figure 4

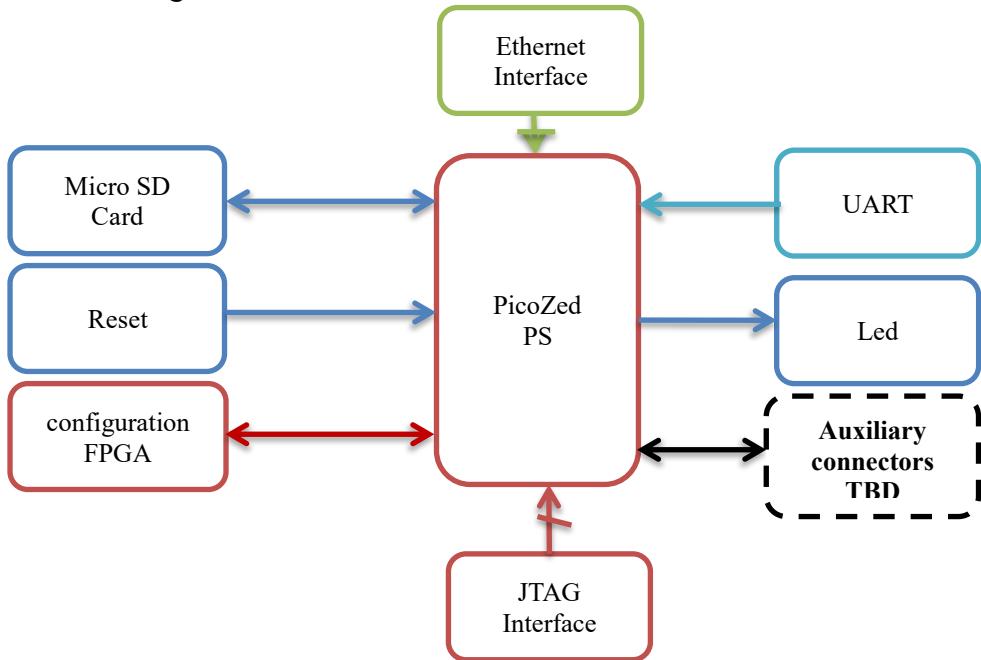


FIGURE 3: PANDABOX ZYNQ PROCESSOR SIDE BLOC DIAGRAM

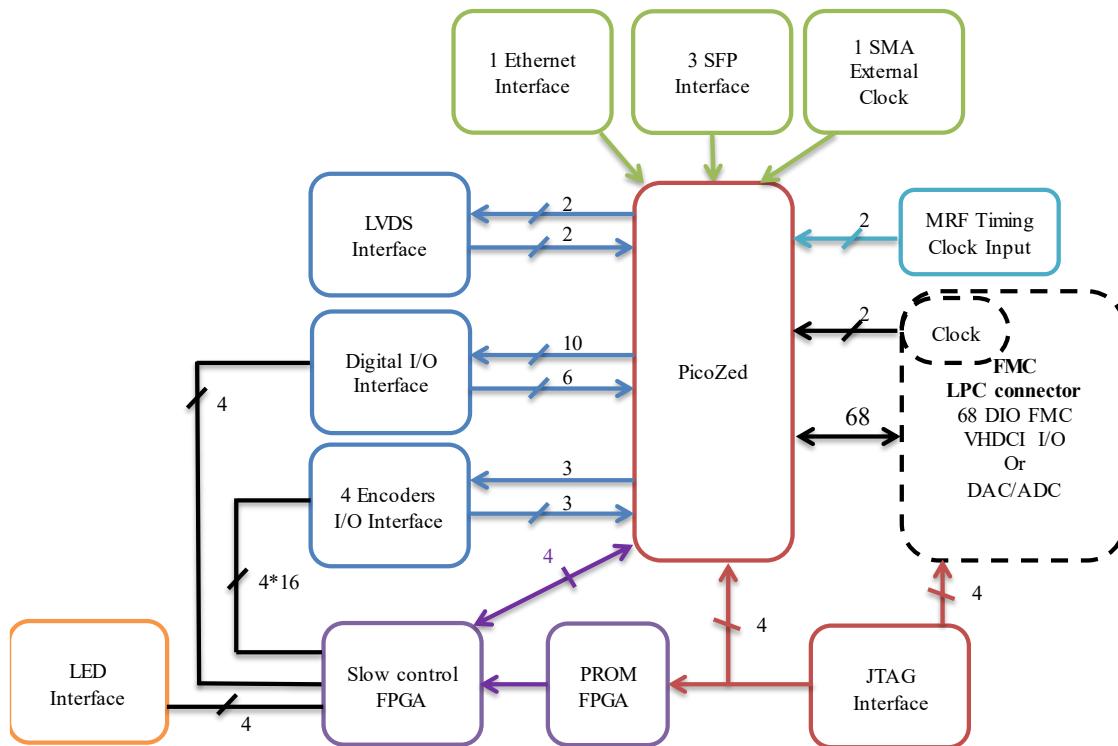


FIGURE 4: PANDABOX LOGIC SIDE BLOCK DIAGRAM

2.2.1.1. References

See the Avnet picoZed xcZ7030 HW Users guide. §1.2.5

2.2.1.2. Picozed boot Configuration

Zynq-7000 AP SoC devices use a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device mode pins are read to determine the primary boot device to be used: NOR, NAND, Quad-SPI, SD Card or JTAG.

PicoZed 7015/7030 allows 3 of those boot devices: QSPI, while SD Card and JTAG boot are easily accessible by changing PicoZed 7015/7030 board switch SW1 settings.

For Pandaboard applications the boot device is set to the SD Card!

PicoZed 7015/7030 board switch SW1 has to be changed as follows:



FIGURE 5 : PICOZED BOARD BOOT MODE SET TO SD CARD

2.2.1.3. PicoZed Pin assignment

In order to summarized the previous description of each functional Block, the pin assignment on the PicoZed is described in the following appendix PandA-Picozed pins assignement

2.2.2. 4X ENCODERS INPUTS / OUTPUTS

In order to configure SOLEIL and Diamond use case, up to four Encoder daughter boards can be mounted on the carrier board inside the PandABox.

- On Soleil version:

PandA handles 4 encoder inputs with Female subd15 connectors and 4 encoder outputs with Female subd15 connectors. The pin configuration of the encoder connectors is shown in the table below.

SubD15 Pin N°	RS422 quadrature incremental encoder	SSI, BISS or Endat absolute encoder
1	A	not used
2	B	not used
3	Z	not used
4	not used	CLK
5	not used	DATA
6	not used**	not used**
7	not used*	not used*
8	GND	GND
9	/A	not used
10	/B	not used
11	/Z	not used
12	not used	/CLK
13	not used	/DATA
14	not used*	not used*
15	5VDC	5VDC

* not used inside PandA, but input signal is wired straight through to output signal.

** 24VDC pin in SOLEIL standard but not powered by PandA, input signal is wired straight through to output signal, possible to wire them of different encoder channels in a chain via jumpers on the carrier main board (see chapter 2.2.2.3).

- On Diamond version:

PandA handles 4 encoder inputs with Female subd15 connectors and 4 encoder outputs with Male subd15 connectors. The pin configuration of the encoder connectors is shown in the table below.

SubD15 Pin N°	RS422 quadrature incremental encoder	SSI, BISS or Endat absolute encoder
1	A	<i>not used</i>
2	/A	<i>not used</i>
3	B	<i>not used</i>
4	/B	<i>not used</i>
5	Z	<i>not used</i>
6	/Z	<i>not used</i>
7	5VDC	5VDC
8	GND	GND
9	<i>not used</i>	/DATA
10	<i>not used</i>	CLK
11	<i>not used</i>	/CLK
12	<i>not used</i>	DATA
13	<i>not used*</i>	<i>not used*</i>
14	<i>not used*</i>	<i>not used*</i>
15	<i>not used*</i>	<i>not used*</i>

* not used inside PandA, but input signal is wired straight through to output signal.

Through these boards, encoder data decoding/encoding will be managed by the PicoZed module, and the setup for all encoders boards will be managed by the Slow FPGA.

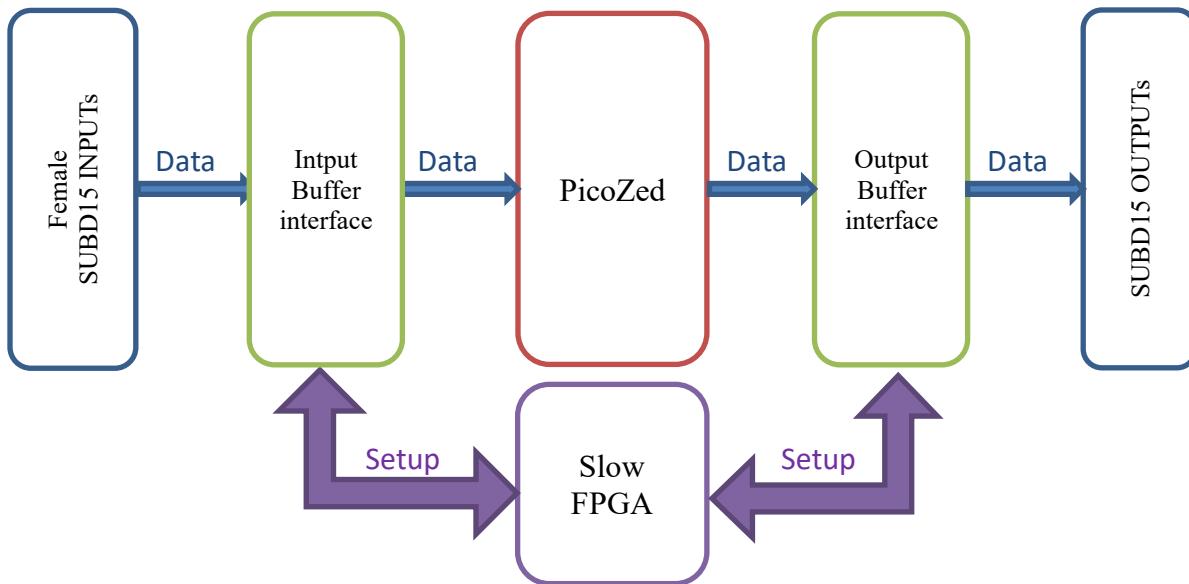


FIGURE 6 : ENCODER INTERFACE FUNCTIONAL BLOC

Each encoder line has a buffer control in order to reduce pin count on the ZYNQ (see Figure 8 describing 1 encoder buffering).

The encoder interface is meant to be compliant for SOLEIL and Diamond encoder pin out. The encoder interface is meant to manage incremental and absolute SSI, ENDAT and BISS encoders.

2.2.2.1. Encoder RS422 pinout

Encoder inputs and outputs to the outside of the box are SubD-15 ports located on PandaBox rear panel(see §3.1 PandaBox Rear and front Panels).

Each four encoders has same pinout on its connectors interface to the outside world (J8A, J8B, J11A, J11B, J14A, J14B, J15A, J15B).

And has same pinout on its connectors on encoder to carrier board interface (J9, J10, J12,J13, J15, J16, J18, J19).

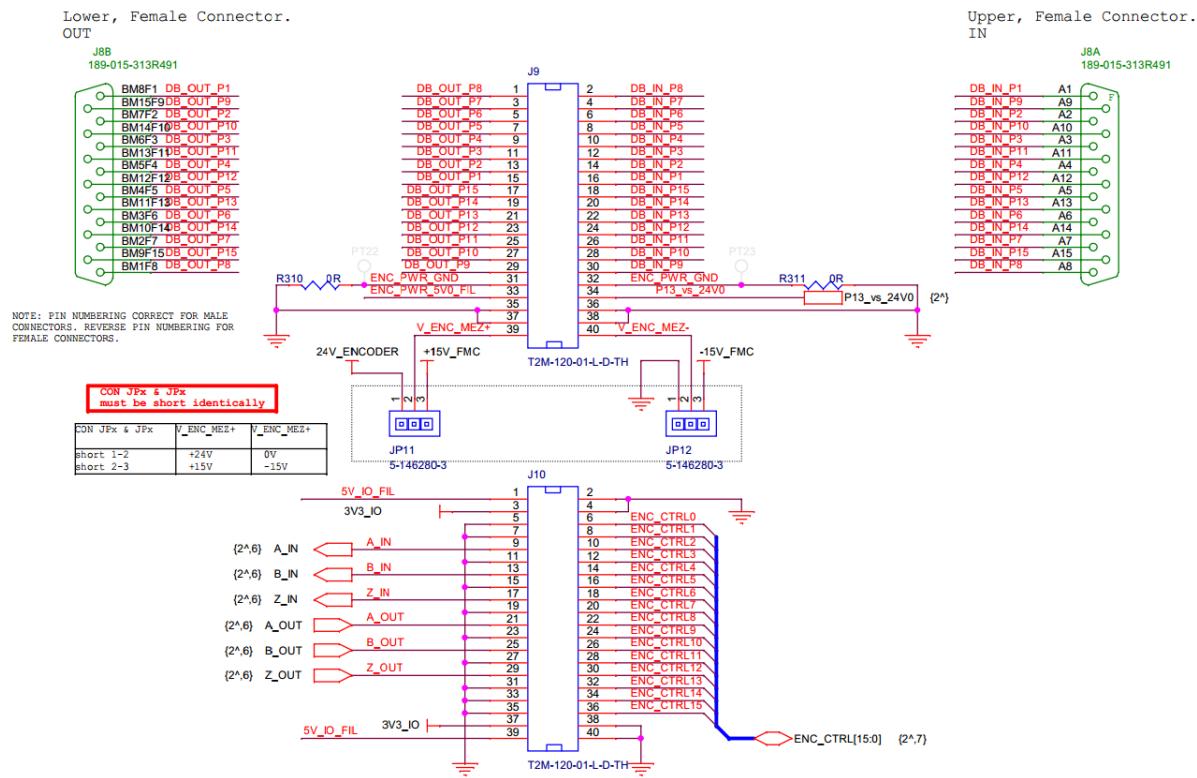


FIGURE 7 : ENCODER 1 PINOUT SCHEMATIC EXEMPLANT

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

2.2.2.2. Encoder board detailed architecture

In order to reduce the number of pin on the PicoZed, a buffer interface is controled by the slow control FPGA. It allows Protocol control, loss of signal detection

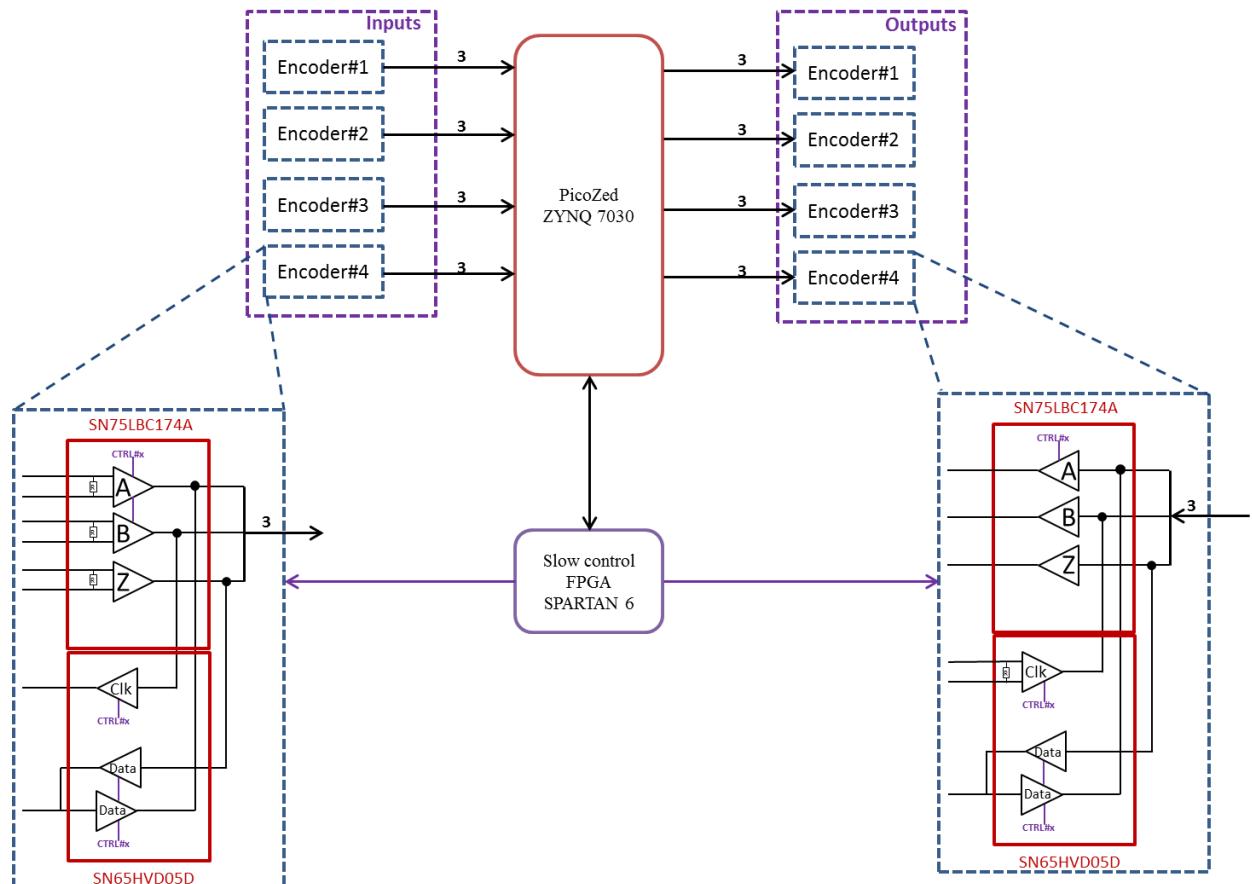


FIGURE 8 : INPUT ENCODER SIGNALS BUFFER CONTROL

In order to permit a set of configuration between SOLEIL and Diamond use case, a set of 0 ohm resistor are used to carry out pin out setting and loopback functionality to hard wired the input to the output.

2.2.2.2.1. *Supported Encoders TYPES*

Incremental position TTL type encoder requirement:

Electrical consummation below 200mA

2 Digital outputs signals in quadrature: A et B

1 Digital signal output in absolute reference: Z

Differential RS422 signals

Maximal frequency 50Mhz

Examples:

Baumer : BDT 16.05A1000-6-5 (rotation)

Heidenhain : ST1278 (translation) or ROD420 (rotation)

Renishaw : RGH25F/Tonic

Absolute position SSI type encoder requirement:

Electrical consummation below 300mA

SSI type digital signals level RS422 : Clock et Data

Support High or Low frequencies

Maximal frequency = 50 MHz

Data frame on <=32 bits in data coding : Binary

Absolute position ENDAT 2.2 type encoder requirement:

Electrical consummation below 300mA

Serial Bidirectional

Code: Pure binary code

Maximal frequency = 50MHz

Position word length: <= 32bits

System Accuracy: ± 20"

Further information available in the datasheet folder in the file: EnDat 21_22.pdf

Absolute position BISS C type encoder requirement:

Electrical consummation below 300 mA

Serial Unidirectional

Pure serial communications (no analogue signal)

Maximal frequency = 50 MHz

Position word length: <= 32 bits

Suitable for linear and rotary axes

Further information available in the datasheet folder in the file: Bissinterface_c5es.pdf

2.2.2.2.2. References

For the current realization of encoder card see §1.2.4 Encoder-Daughter-Card

2.2.2.3. Encoder Power distribution jumper configuration

In order to power encoders either from PandaA or from the Motion controller, a set of jumpers permits this configuration. This configuration allows powering of one or more encoder from the motion controller.

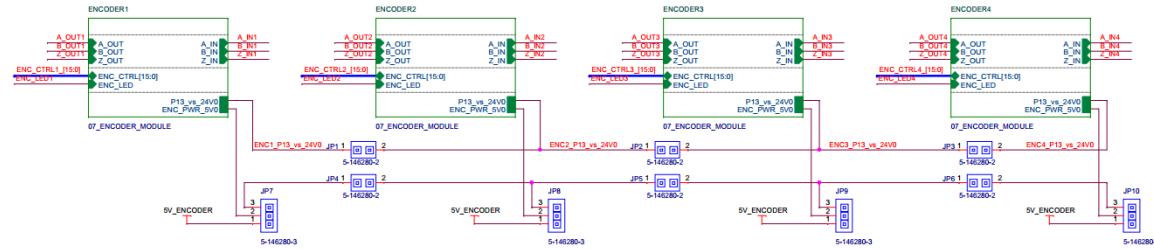


FIGURE 9:POWER SUPPLIES SCHEMATICS

Complete description of encoder power configuration can be found on §3.2.1 Carrier Board Encoder configuration Jumpers

2.2.3. MULTI-CHANNEL TLL AND LVDS INPUTS/OUTPUTS WITH LED STATUS

Multi-Channel TLL and LVDS Inputs/outputs from the font Panel are linked to the picoZed. The slow-fpga can control LED status and TTL inputs impedance via an SPI interface

2.2.3.1. TTL Digital Inputs/Outputs Interface

Panda handles 6 Inputs and 10 Outputs TTL driven by 8-Bit Dual-Supply Bus Transceiver with Configurable voltage translation and 3-State (SN74LVC8T245) Outputs (see Figure 10). This 8-bit non inverting bus transceiver uses two separate configurable power-supply rails. The SN74LVC8T245 is optimized to operate with VCCA and VCCB set at 1.65V to 5.5V. It was chosen primarily for its configurable level translation capability. It permits with one component to interface TTL and 1.8V levels either as an input or output signals.

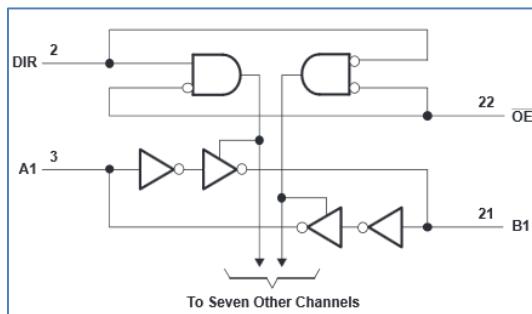


FIGURE 10: SN74LVC8T245 LOGIC DIAGRAM

Control pins DIR and OE# are supplied by VCCA.

2.2.3.1.1. TTL Digital Inputs

Only one SN74LVC8T245 is required for the 6 digital inputs (see Figure 11).

TTL inputs are connected to female BNC port on PandaBox front (see §3.1 PandaBox Rear and front Panels) to carrier FPGA inputs on Picozed Board.

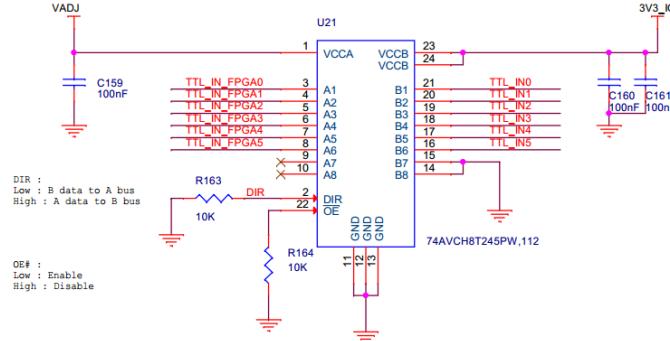


FIGURE 11 : DIGITAL INPUTS BUFFER SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 2: TTL INPUT PIN ASSIGNMENT ON PICOZED

JX2 Pin #	Net Name JX2	Zync 7030 FPGA	Carrier board name	Function
17	34_LVDS_0_P	BANK34 - M4	TTL_IN_FPGA0	TTL_IN1
18	34_LVDS_1_P	BANK34 - J2	TTL_IN_FPGA1	TTL_IN2
19	34_LVDS_0_N	BANK34 - M3	TTL_IN_FPGA2	TTL_IN3
20	34_LVDS_1_N	BANK34 - J1	TTL_IN_FPGA3	TTL_IN4
23	34_LVDS_2_P	BANK34 - K7	TTL_IN_FPGA4	TTL_IN5
24	34_LVDS_3_P	BANK34 - J3	TTL_IN_FPGA5	TTL_IN6

2.2.3.1.2. TTL Digital Outputs

For the 10 digital outputs, we connect them to 4 outputs of the transceiver to have enough current ($4 \times 32\text{mA} = 128\text{mA}$ max) for TTL output (see Figure 12).

TTL outputs are connected to female BNC port on PandaBox front (see §3.1 PandaBox Rear and front Panels).

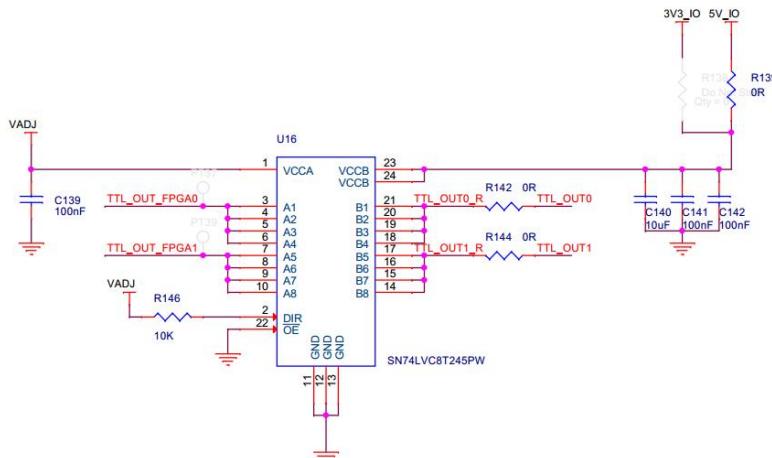


FIGURE 12 : DIGITAL OUTPUT BUFFER SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 3: TTL OUTPUT PIN ASSIGNMENT ON PICOZED

JX2 Pin #	Net Name JX2	Zync 7030 FPGA	Carrier board name	Function
29	34_LVDS_4_P	BANK34 - P7	TTL_OUT_FPGA0	TTL_OUT1
30	34_LVDS_5_P	BANK34 - L2	TTL_OUT_FPGA1	TTL_OUT2
31	34_LVDS_4_N	BANK34 - R7	TTL_OUT_FPGA2	TTL_OUT3
32	34_LVDS_5_N	BANK34 - L1	TTL_OUT_FPGA3	TTL_OUT4
35	34_LVDS_6_P	BANK34 - N4	TTL_OUT_FPGA4	TTL_OUT5
36	34_LVDS_7_P	BANK34 - P3	TTL_OUT_FPGA5	TTL_OUT6
37	34_LVDS_6_N	BANK34 - N3	TTL_OUT_FPGA6	TTL_OUT7
38	34_LVDS_7_N	BANK34 - P2	TTL_OUT_FPGA7	TTL_OUT8
25	34_LVDS_2_N	BANK34 - L7	TTL_OUT_FPGA8	TTL_OUT9
26	34_LVDS_3_N	BANK34 - K2	TTL_OUT_FPGA9	TTL_OUT10

2.2.3.2. TTL Inputs/Outputs Leds and inputs 50 Ω Termination control

2.2.3.2.1. TTL Inputs/Outputs Leds

Each Digital Inputs/Outputs have his own led for visual information on PANDABOX front (see §3.1 PandaBox Rear and front Panels).

TTL input/output led, together with §2.2.11 STA and ACQ status led and §2.2.3.2.2 TTL Inputs 50 Ω Termination, are controlled from Slow FPGA Shift registers signals
For complete description of its control see appendix §3.4 Front Board SHIFT Registers

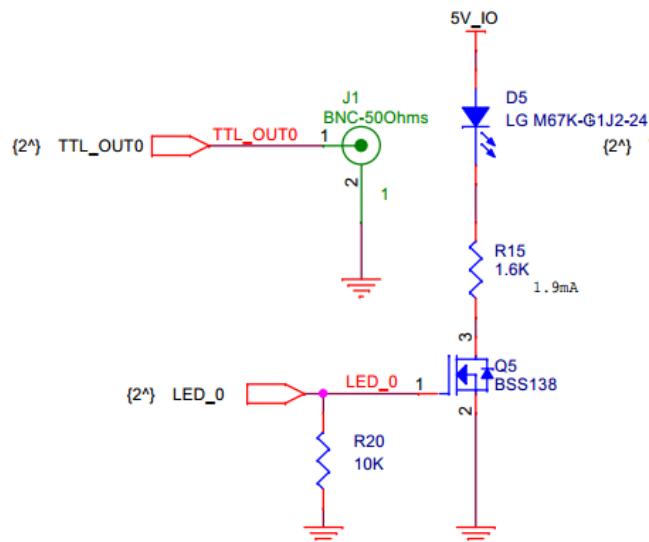


FIGURE 13 : TTL OUT LED EXEMPLE ON THE FRONT BOARD

(Note: The source of this schematic can be found in § 1.2.3 Panda Front board schematic)

2.2.3.2.2. TTL Inputs 50 Ω Termination

Each Digital Inputs have its own 50Ω termination controlled by the slow FPGA. To save pin, serial communication is used(4 signals, DATA, CLK, LATCH and OE#) to control the shift register on the Front Board.

For complete description of its control see appendix §3.4 Front Board SHIFT Registers

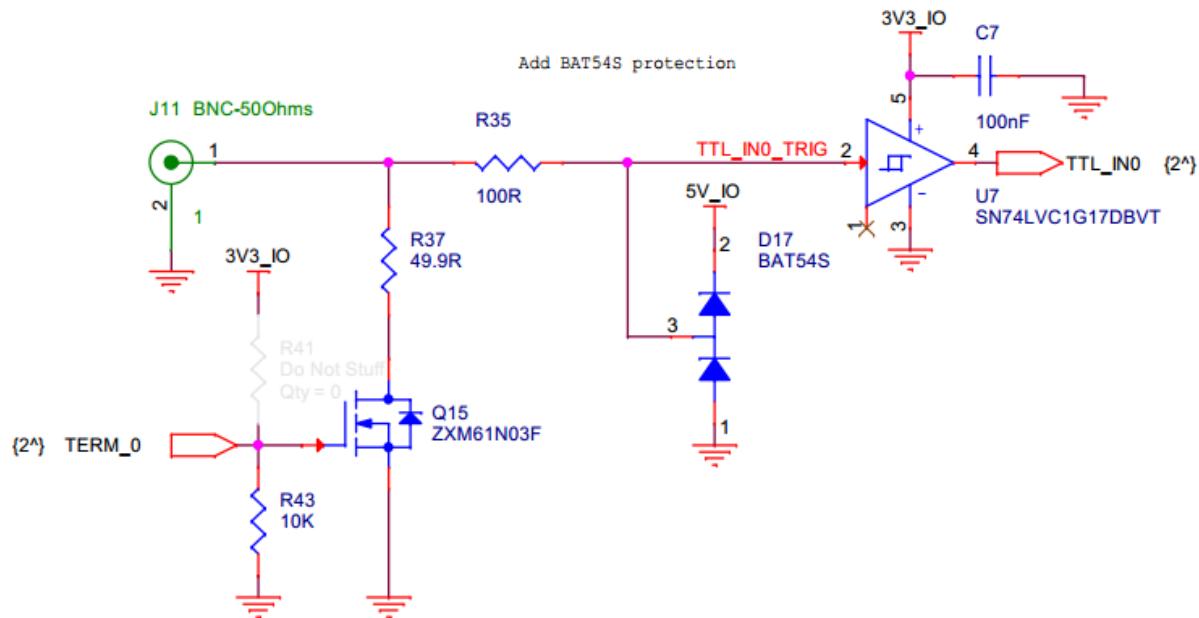


FIGURE 14 : EXAMPLE OF TTL INPUT 50Ω TERMINATION ON THE FRONT BOARD

(Note: The source of this schematic can be found in § 1.2.3 Panda Front board schematic)

2.2.3.3. LVDS Inputs/Outputs Interface

PandA handles 2 LVDS drivers and 2 LVDS receivers. 2 DS91M047 quad drivers (see Figure 17) are connected to 2 differential connectors (Lemo EZG.00.302.NLN). 2 LVDS input receivers, SN65LVDS348 quad receivers (see Figure 15) are connected to 2 differential connectors (Lemo EZG.00.302.NLN).

LVDS input port and output port are on PandaBox front(see §3.1 PandaBox Rear and front Panels)

2.2.3.3.1. LVDS Inputs

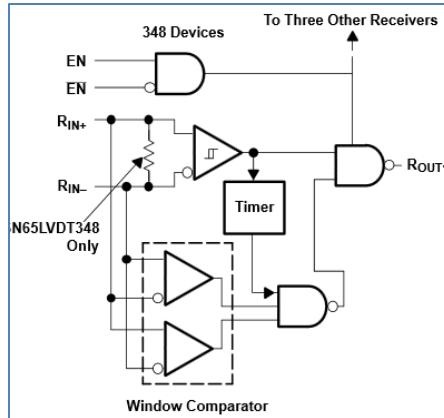


FIGURE 15 : SN65LVDS348 RECEIVER LOGIC DIAGRAM

Each LVDS differential inputs are single-ended with the SN65LVDS348 quad receivers. To not damage the ZYNQ, this signal is translate from 3V3 to 1V8 with a level shifter 74AVCH2T45DC,125 for example (see Figure 16).

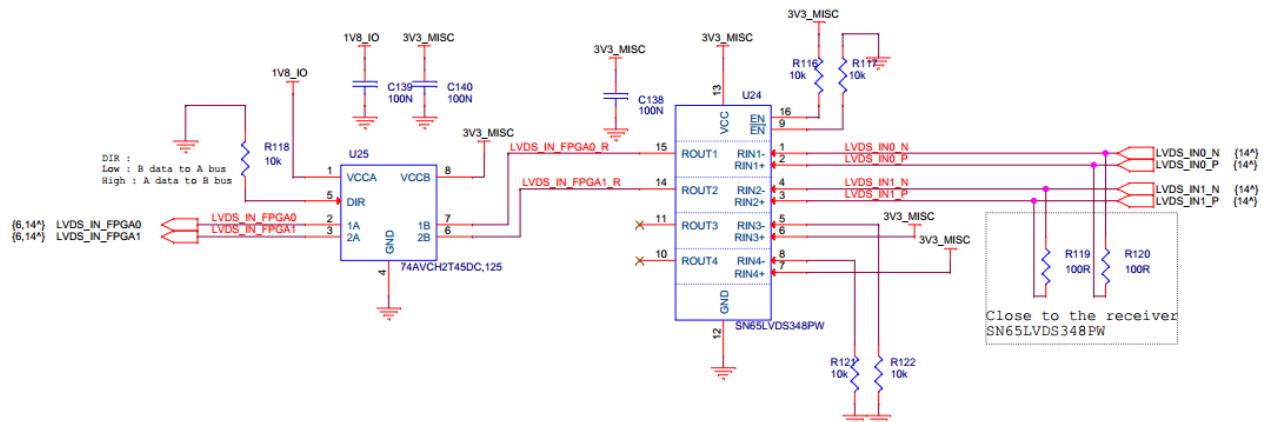


FIGURE 16 : LVDS INPUTS CARRIER BOARD SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 4: LVDS INPUT PIN ASSIGNMENT ON PICOZED

JX2 Pin #	Net Name JX2	Zync 7030 FPGA	Carrier board name	Function
41	34_LVDS_8_P	BANK34 - M2	LVDS_IN_FPGA0	LVDS_IN1
42	34_LVDS_9_P	BANK34 - N1	LVDS_IN_FPGA1	LVDS_IN2

2.2.3.3.2. LVDS Outputs

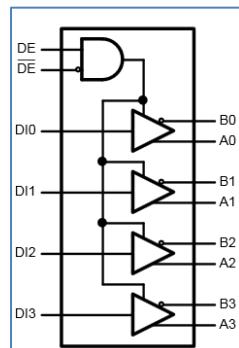


FIGURE 17 : DS91M047 DRIVER LOGIC DIAGRAM

Each LVDS differential outputs are driving by the DS91M047 Line Driver and are translate from 1V8 to 3V3 with a level shifter 74AVCH2T45DC,125 for example (see Figure 18).

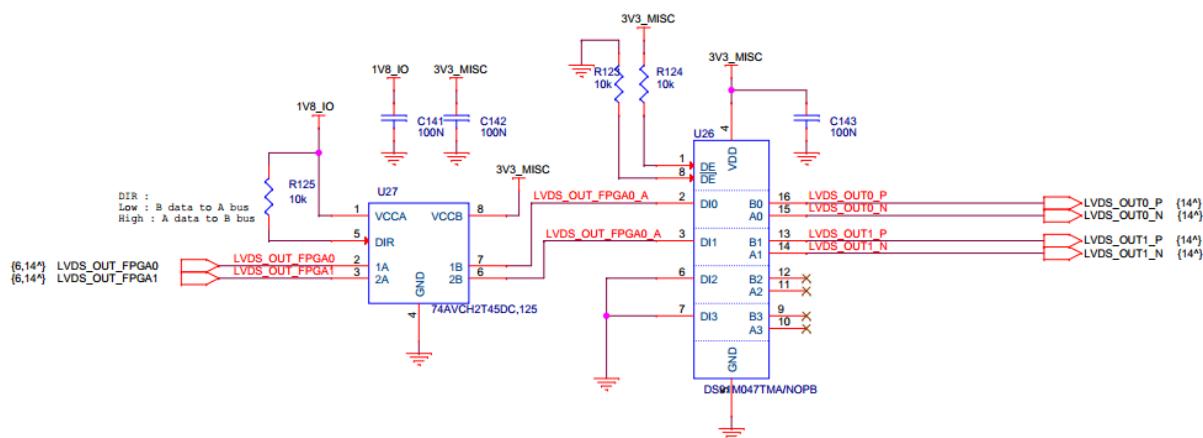


FIGURE 18 : LVDS OUPUTS

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 5: LVDS OUTPUT PIN ASSIGNMENT ON PICOZED

JX2 Pin #	Net Name JX2	Zync 7030 FPGA	Carrier board name	Function
43	34_LVDS_8_N	BANK34 - M1	LVDS_OUT_FPGA0	LVDS_OUT1
44	34_LVDS_9_N	BANK34 - P1	LVDS_OUT_FPGA1	LVDS_OUT2

2.2.4. LPC - FMC CONNECTOR (OPTIONAL BOARD)

FMC (FPGA mezzanine card) respecting LPC (Low Pin Count) standard connector is implemented. This implementation respects the ANSI/VITA 57.1 FMC Standard.

This connector is directly connected to Avnet picoZed xcZ7030

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNTR_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA21_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	I2POV	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	I2POV	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

FIGURE 19 : SIGNAL DEFINITIONS FOR LOW-PIN COUNT CONNECTOR

2.2.4.1.1. User defined signals

CLK[0..1]_M2C_P, CLK[0..1]_M2C_N .- Differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card.

LA[00..33]_P, LA[00..33]_N .- User defined signals on Bank A located on the LPC.

All signals are routed differentially and connected to the ZYNQ 7030.

2.2.4.1.2. Gigabit Data Signals

GBTCLK0_M2C_P, GBTCLK0_M2C_N - A differential pair shall be used as a reference clock for the DP data signals.

DP0_M2C_P, DP0_M2C_N, DP0_C2M_P, DP0_C2M_N - A multi-gigabit transceiver data pairs.

All signals are routed differentially and connected to the ZYNQ 7030.

2.2.4.1.3. Power supplies

VREF_A_M2C .- This is the reference voltage associated with the signaling standard used by the bank A data pins, LAxx and HAxx. If the signaling standard on Bank A does not require a reference voltage then this pin can be left unconnected.

3P3VAUX - A 3.3V auxiliary power supply.

VADJ .- These pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module. To be compliant with the Zynq 7030, VADJ should be 1,8V.

3P3V .- These pins carry 3.3V power from the carrier to the IO Mezzanine module.

12P0V .- These pins carry 12V power from the carrier to the IO Mezzanine module.

GND .- This is signal ground.

2.2.4.1.4. I²C Interface

GA[0..1] - These signals provide geographical addressed of the module and are used for I²C channel select.

SCL .- System Management I²C serial clock. This signal provides a clock reference to the IO Mezzanine module from the carrier card for a two-wire serial management bus.

SDA - System Management I²C serial data. This signal provides a data line for a two-wire serial management bus.

On Panda Carrier V02R01 the FMC I²C is connected to Picozed PS dedicated pin ZYNQ_MIO14 and ZYNQ_MIO15 using R333 and R335.

But FMC I²C could be connected to the previous slow FPGA pins by using R332 and R334 (as in Panda Carrier board version older than V02R01).

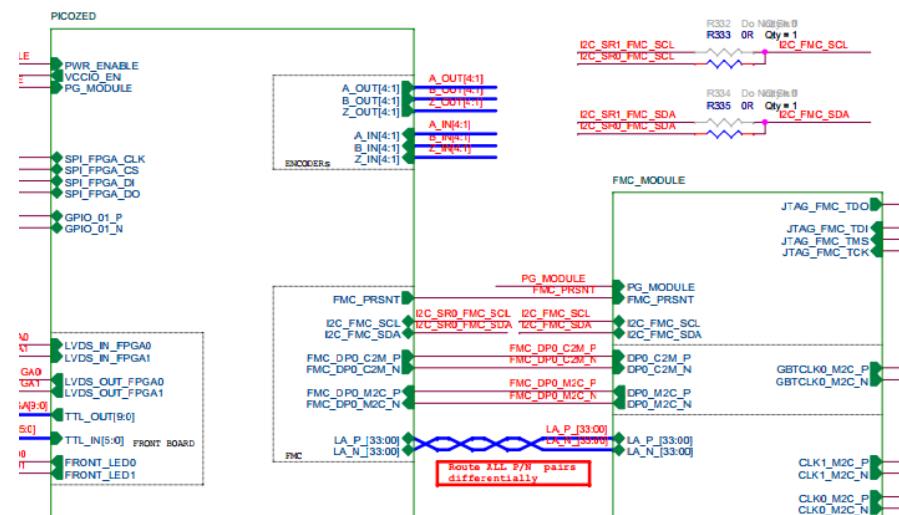


FIGURE 20: I²C CONTROL SELECTION SCHEMATIC

2.2.4.1.5. JTAG Interface

TRST_L - JTAG Reset. This signal provides asynchronous initialization of the TAP controller on the IO Mezzanine module. (Test Reset input to IO mezzanine module)

TCK - JTAG Clock. This signal provides an independent clock reference for TAP controller operation. (Test Clock input to IO mezzanine module)

TMS - JTAG Mode Select. This signal shall provide state control of the TAP controller on the IO Mezzanine module. (Test Mode Select input to IO mezzanine module)

TDI - JTAG Data In. This signal provides for serial writes of test data and instructions into the IO Mezzanine module. (Test Data Input to IO mezzanine module)

TDO - JTAG Data Out. This signal provides for serial writes of test data and instructions out of the IO Mezzanine module. (Test Data Output from IO mezzanine module)

The JTAG for FMC should have his own connector. A set of 0-Ohm Resistors should be implemented to allow the JTAG to be on the Daisy chain with the ZYNQ and the Slow FPGA

All signals on the JTAG communication should have 4,7kOhms pull-up

2.2.4.1.6. Power GOOD/PRESENT signals

PRSNT_M2C_L - Module present signal. This signal allows the carrier to determine whether an IO Mezzanine module is present.

This signal should be connected to the ZYNQ 7030 on a 3V3 BANK. Otherwise a translation should be done with VADJ (1.8V).

PG_C2M .- Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance.

This signal should be connected to power supplies distribution's power good.

2.2.4.1.7. Other specifications

More details, see AV57DOT1.pdf.

2.2.5. 3 SFP

The Carrier Card design should carefully examine desired performance requirements of the transceivers and provide adequate signaling and transceiver power on the associated pins of the JX3 connector.

NOTE: The transceivers differ between the 7015 and the 7030 in power requirements and care should be taken depending on which platform is desired in your system. Review 7

series FPGAs GTX/GTH Transceivers User guide for details surrounding the difference between designs using the 7015 versus the 7030.

PicoZed 7030 has four gigabit full-duplex transceiver lanes that reside on Bank 112 of the Zync device. 3 of these high speed transceivers will be used to interface 3 SFP cages.

Ether clock input, FMC GBTCLK or generated clock can be used as the clock reference for anyone or more of the GTX lanes in bank 112 (see Figure 22).

Gigabit transceiver lanes and their associated reference clocks are connected to the carrier board via the JX3 Micro Header (see Table 6 and Figure 22).

TABLE 6: SFP PINOUT

Pin # JX3	Net Name JX3	Pin # PicoZed 7030	Function
1	MGTRREFCLK0_P	U9	Clock 0
3	MGTRREFCLK0_N	V9	
2	MGTRREFCLK1_P	U5	Clock 1
4	MGTRREFCLK1_N	V5	
14	MGTRX1_P	W8	SFP1 RX/TX
16	MGTRX1_N	Y8	
19	MGTTX1_P	W4	
21	MGTTX1_N	Y4	
20	MGTRX2_P	AA9	SFP2 RX/TX
22	MGTRX2_N	AB9	
25	MGTTX2_P	AA5	
27	MGTTX2_N	AB5	
26	MGTRX3_P	W6	SFP3 RX/TX
28	MGTRX3_N	Y6	
31	MGTTX3_P	W2	
33	MGTTX3_N	Y2	

Control of the 3 SFP modules are done from Slow-FPGA and transmitted to individual SFP port through TCA9545A I2C SMBUS Switch.

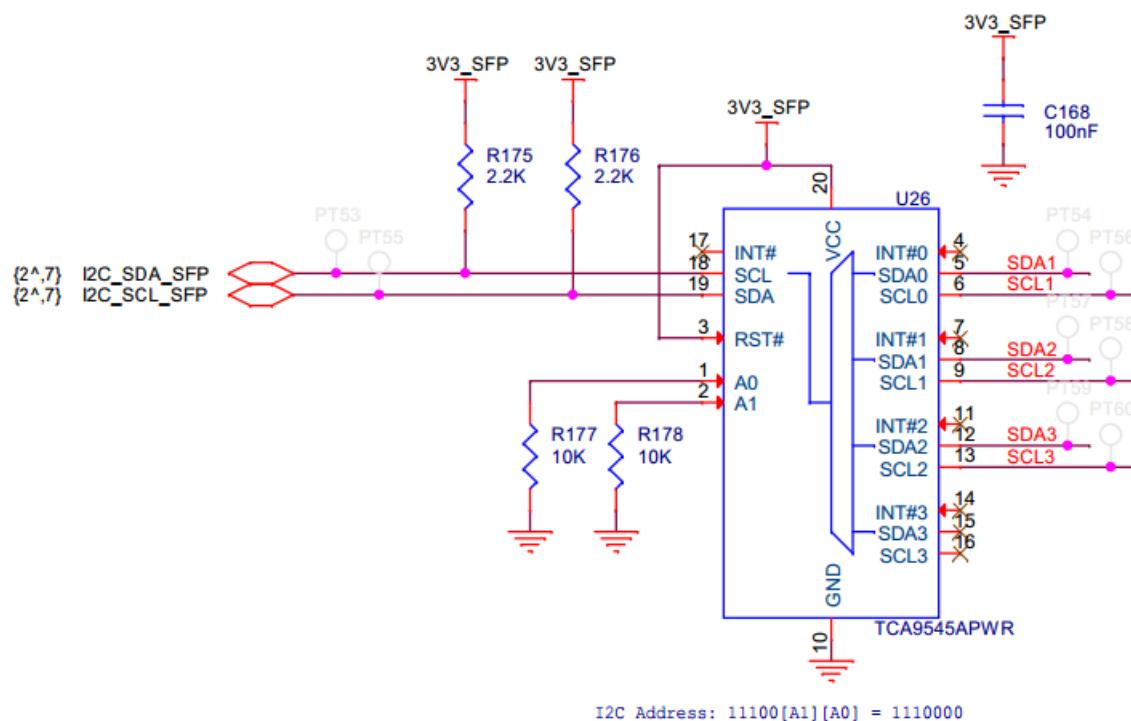


FIGURE 21: CARRIER BOARD I2C SFP SWITCH

For complete description of SFP I2C switch IC(TCA9545a) used on Carrier board see:
<http://www.ti.com/lit/ds/symlink/tca9545a.pdf>

The control of SFPs I2C are currently not implemented in Panda Firmware.

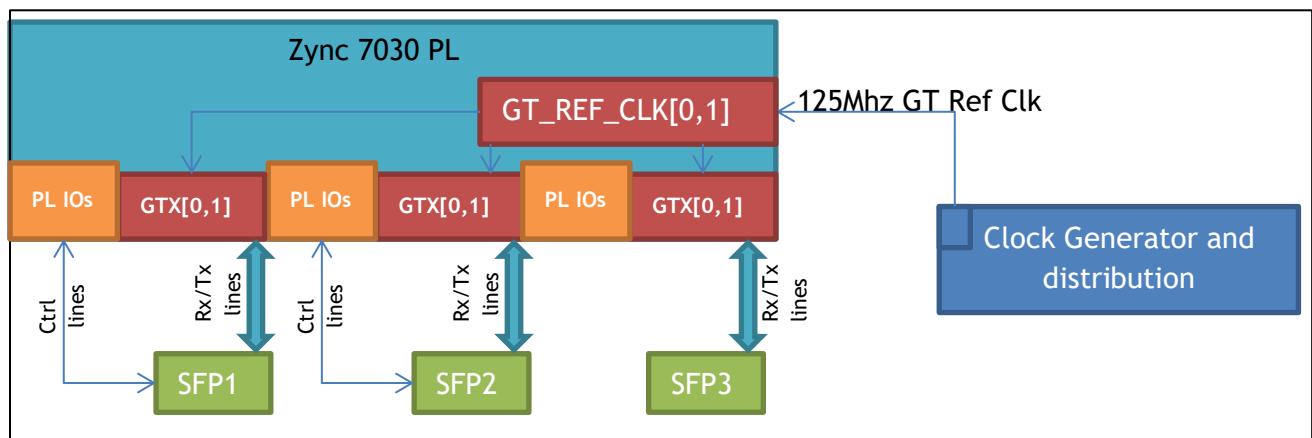


FIGURE 22 : BLOCK DIAGRAM PL SFP TO GTX LINK

2.2.5.1. SFP Jumper configuration

For configuration jumpers see §3.2.2 Carrier Board SFP configuration Jumpers

2.2.6. 1 GIGABIT ETHERNET FOR CONTROL AND DAQ

On PicoZed, 2 Ethernet ports are available, for PandA only one is currently identified to be usefull.

It will respect the following interface.

TABLE 7: ETHERNET PINOUT

Net Name	JX3 Pin#	JX3 Pin#	Net Name
ETH_PHY_LED0	47	48	ETH_PHY_LED1
ETH_MD1_P	51	52	ETH_MD2_P
ETH_MD1_N	53	54	ETH_MD2_N
ETH_MD3_P	57	58	ETH_MD4_P
ETH_MD3_N	59	60	ETH_MD4_N

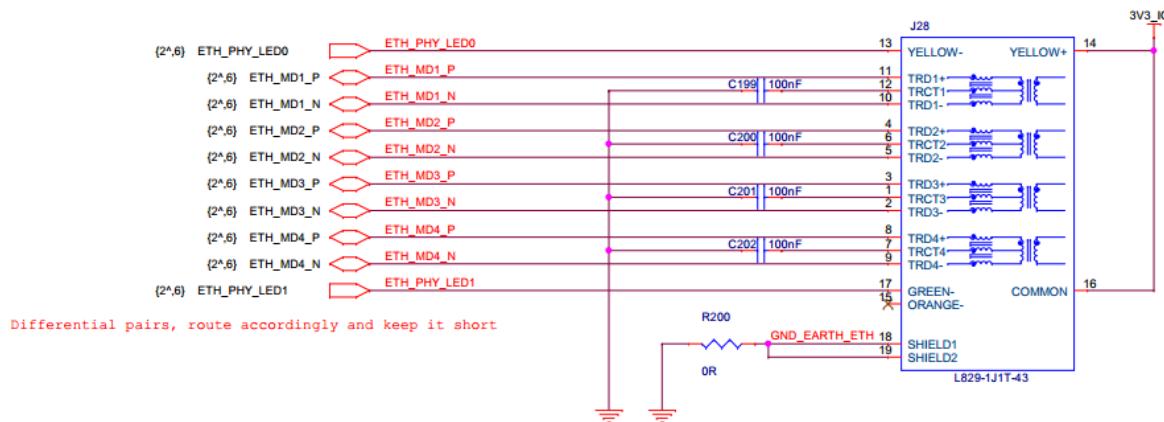


FIGURE 23 : ETHERNET SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

2.2.7. SLOW CONTROL VIA SPARTAN-6 WITH PROM

2.2.7.1.1. SPARTAN-6

The slow control FPGA aims at controlling function or peripheral which configuration is static or process is asynchronous. It will mainly control LED, FAN, buffer configurations....
The functions identified on the slow FPGA are listed below:

TABLE 8 :SLOW CONTROL FPGA PIN COUNT

Function	Pins	Units	Total	Functionality
Encoder Control				
Loss detection interface CTRL_D[0..1]	2	4	8	Control buffer on Loss detection interface
Incremental encoder interface control CTRL_D[2..5]	4	4	16	Control RS422 buffer
Incremental to SSI encoder interface control CTRL_D[6..9]	4	4	16	Select RS422 or SSI buffer
Termination switching interface control CTRL_D[10..11]	2	4	8	Select 120 Ω Termination for SSI interface
Spare interface control CTRL_D[12..15]	4	4	16	Spare control line for new board
CLOCK				
CLK_125MHz	1	1	1	Additional 125MHz clock
I2C to control SI57X	3	1	3	I2C to configure I2C Multiplexer to setup 2 SI57X
CLK_MUX control between FMC and SI57X	1	1	1	Multiplexer control, to select clock from FMC or SI57X
FAN				
Fan Control	1	2	2	Read fan speed to diagnose fan state
FMC				
I2C FMC	2	1	2	I2C control for the FMC board
SFP				
I2C SFP	2	1	2	I2C control for the SFP Interface
LED				
Shift register control [TTL LED;TTL Termination; STATUS; POWER;]	4	1	4	Control for Front panel LED, 50Ω TTL; Status LED; Power Led
Encoder LED	1	4	4	Control back panel LED for encoder
SPI-ZYNQ_To_FPGA				
SPI_Interface_4Wire	4	1	4	SPI interface to control and communicate with the Slow control FPGA from the Zynq
		TOTAL	88	

In order to carry out this function we will use a SPARTAN 6 FPGA. Diamond use XC6SLX9 part number on Zebra component

2.2.7.1.2. PROM

In order to store the large STARTAN-6 Xilinx FPGA configuration, XCF04S PROM is present on the Carrier Board.

2.2.7.1.1. Slow FPGA BOOT architecture

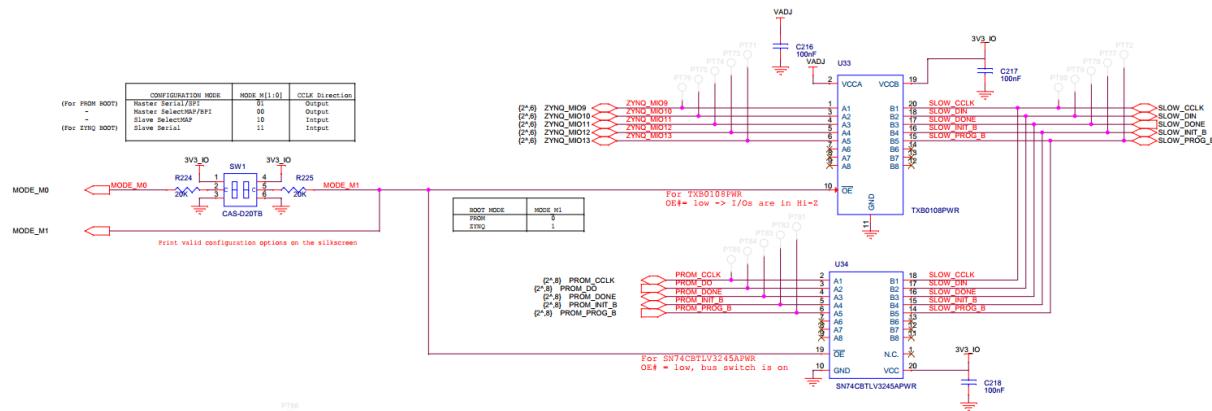


FIGURE 24: SLOW FPGA BOOT SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

The slow FPGA Spartan-6 is configured in “SLAVE Serial” mode. The configuration master will be either PROM or ZYNQ controlled by SW1 carrier board DIP switches.

Default boot should be ZYNQ (For complete description, see §3.2.3Carrier Board Slow FPGA Boot mode configuration Switch).

When loading Slow FPGA configuration from Zynq the signals are generated from the following Table 9 Picozed board pin assignment

TABLE 9: SLOW FPGA BOOT SIGNALS PIN ASSIGNMENT ON PICOZED

JX2 Pin #	Net Name JX1	PicoZed 7015/7030	Function
8	PS_MIO09	BANK500 - C19	CCLK
1	PS_MIO10	BANK500 - G16	DIN
6	PS_MIO11	BANK500 - B19	DONE
5	PS_MIO12	BANK500 - C18	INIT_B
2	PS_MIO13	BANK500 - A17	PROG_B

2.2.8. RS232 UART ARM TERMINAL

Usefully for monitoring Linux boot logs and access Linux terminal, PandA include a UART Interface.

PandA UART Interface is without CTS and RTS signals. It respects the following interface with Picozed daughter card.

TABLE 10: UART ARM TERMINAL PIN ASSIGNMENT PICOZED

JX3 Pin#	JX3 logic name	Net Name
42	PS_MIO48	UART_TXD
44	PS_MIO49	UART_RXD

Pins UART RXD and TXD are on the 1.8V BANK from the ZYNQ.

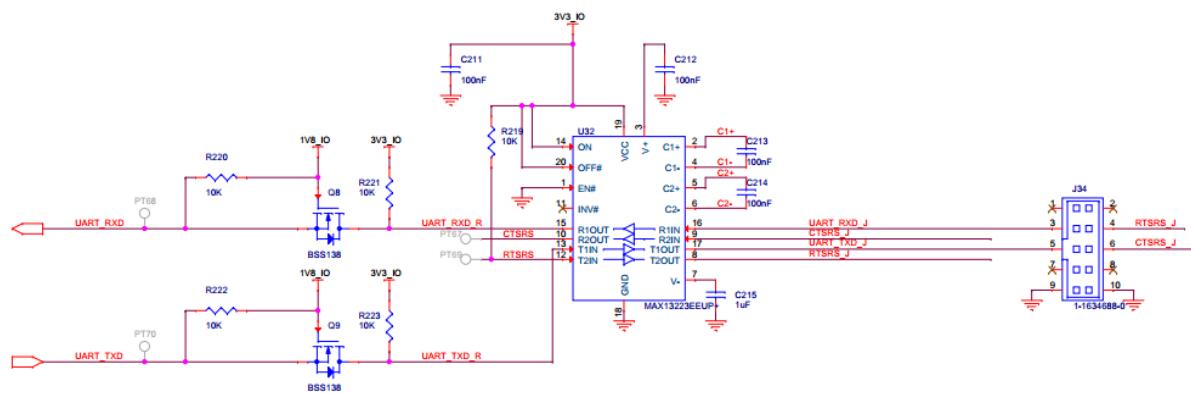


FIGURE 25 : UART SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

2.2.8.1. RS232 UART PandaBox interface

UART interface J34 is linked on D-sub9 connector labed RS232 of the rear panel (see §3.1 PandaBox Rear and front Panels).

2.2.9. USB HOST

PandA include a USB Interface with USB_ID, USB_OTG_P and USB_OTG_N signals. It respects the following interface with Picozed daughter card.

TABLE 11: USB PIN ASSIGNMENT ON PICOZED

JX3 Pin#	JX3 logic name	Net Name
63	USB_ID	USB_OTG_ID
67	USB_OTG_P	USB_OTG_P
69	USB_OTG_N	USB_OTG_N
70	USB_OTG_OPEN	USB_OTG_OPEN
68	USB_VBUS_OTG	USB_VBUS_OTG

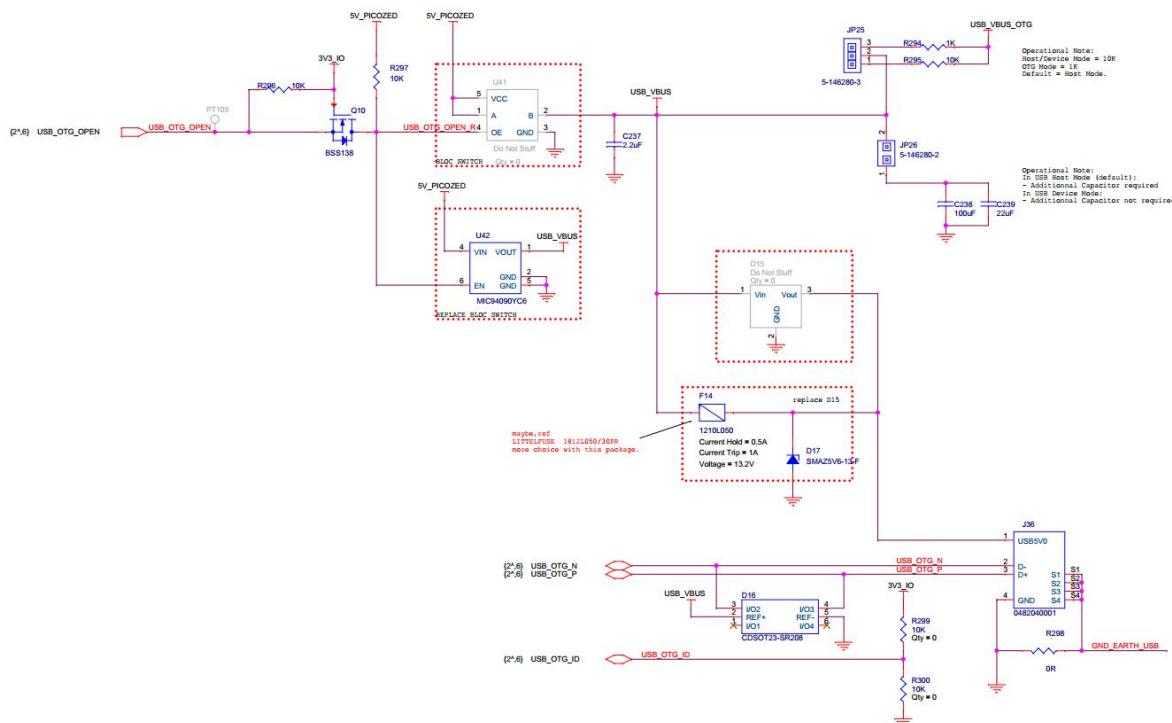


FIGURE 26: USB SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

2.2.9.1. USB jumper Configuration

USB mode can be selected with jumpers see §3.2.4 Carrier Board USB configuration
Jumpers for decription

2.2.9.2. USB PandaBox interface

USB interface J36, Mounted on the Carrier Board, shows as connector labed USB of the rear panel (see §3.1 PandaBox Rear and front Panels).

2.2.10. JTAG

PandA uses one main chain for JTAG to program Zynq SOC, Slow control FPGA and its PROM. For debug purpose, we should add 0-Ohm resistor to disconnect one device on the chain.

The following functional block presents the implementation.

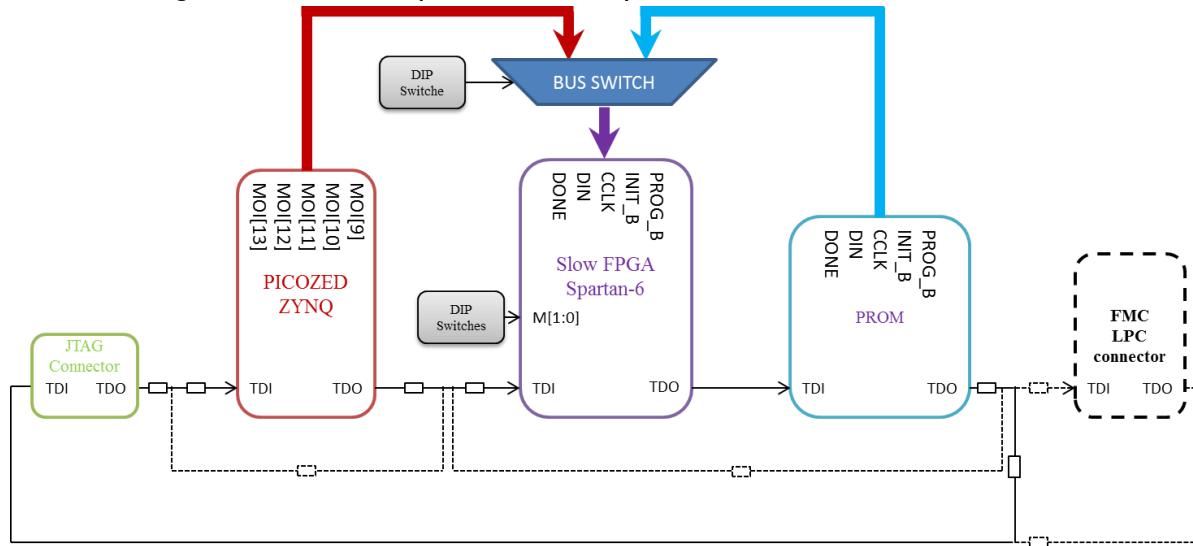


FIGURE 27 : JTAG/BOOT FUNCTIONAL BLOCK

2.2.10.1. JTAG architecture

The FMC JTAG have his own connector and an option with 0-Ohm resistors is implemented on all signals to add FMC JTAG on the daisy chain (see Figure 27 : JTAG/BOOT functional block).

TABLE 12: JTAG PIN ASSIGNMENT ON PICOZED

JX1 Pin #	Net Name JX1	Zync 7030 FPGA	Function
1	JTAG_TCK	BANK0 - H11	JTAG_TCK
2	JTAG_TMS	BANK0 - H10	JTAG_TMS
3	JTAG_TDO	BANK0 - G9	JTAG_TDO
4	JTAG_TDI	BANK0 - H9	JTAG_TDI

2.2.10.2. JTAG PandaBox interface

JTAG interface J22, Mounted on the Carrier Board, shows as connector labed JTAG of the rear panel (see §3.1 PandaBox Rear and front Panels).

2.2.11. STATUS LED

PandA handles 4 status led for visual information on PANDABOX front right end side (see §3.1 PandaBox Rear and front Panels). These leds are controlled by PICOZED pins or by slow FPGA thow the shift register signals communication to the front board.

TABLE 13: STATUS LED DESCRIPTION

Led Colour	Name	Function
GREEN	STA	Power status
GREEN	RDY	*application specific
RED	ERR	*application specific
YELLOW	ACQ	ACQ status

(*)RDY and ERR status leds are controlled from PicoZED broard pin (see Table 14)

TABLE 14: STATUS LED PIN ASSIGNMENT PICOZED ON PANDA_FRONT_BOARD

JX3 Pin#	JX2 logic name	Zync SOC pin #	Carrier board Net Name	Controlled Led on front Board
66	PS_MIO50	501-D10	FRONT_LED0	ERR led status
64	PS_MIO51	501-C13	FRONT_LED1	RDY led status

STA and ACQ status leds, together with TTL Led and TTL Inputs 50 Ω Termination of §2.2.3.2, are controlled from Slow FPGA Shift registers signals

See appendix §3.4Front Board SHIFT Registers

2.2.12. EXTERNAL CLOCK

PandA include a External clock Interface. It respects the following interface with Picozed daughter card.

TABLE 15: EXTERNAL CLOCK PIN ASSIGNMENT PICOZED

JX3 Pin#	JX3 logic name	Net Name
73	13_LVDS_7_P	EXTCLK+
75	13_LVDS_7_N	EXTCLK-

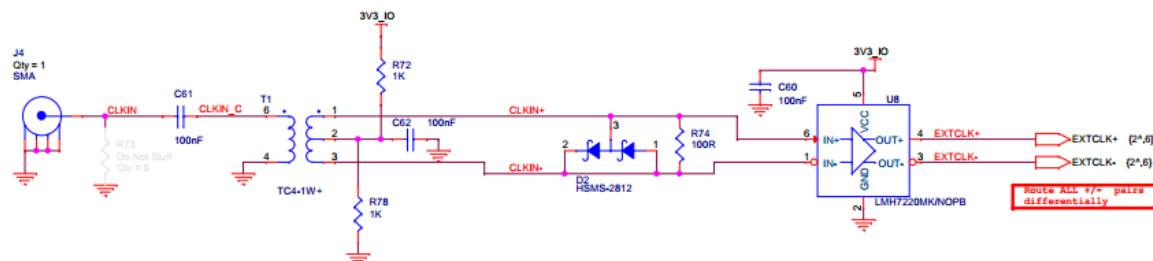


FIGURE 28 : EXTERNAL CLOCK SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

2.2.12.1. External clock PandaBox interface

External clock interface J4 is linked on SMA connector labed CLK of the rear panel (see §3.1 PandaBox Rear and front Panels).

2.2.13. ON BOARD CLOCK TREE

The following Clocking circuitry is implemented on PandABox:

2 on board programmable clock (Si570 component for example) for IPBus

1 External input from SMA connector to received Diamond Timing clock

3 on board clock from FMC connector

Internal Zynq 125MHz coming from processor part used to clock FPGA part

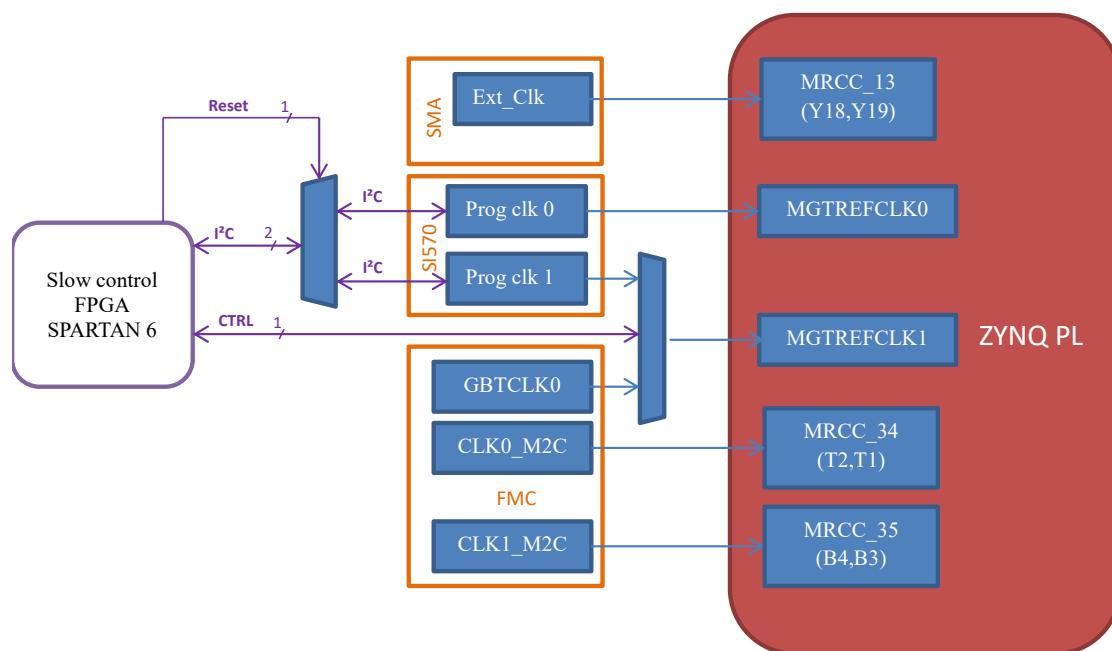


FIGURE 29: CLOCKING CIRCUITRY

The clocking circuitry architecture uses two SI570 (part Number: 570CAC000121DG) to generate on board clock up to 280MHz.

To program both SI570, a dual bidirectional translating switch is controlled by the slow FPGA using one I²C bus.

For MGTREFCLK1, we have the choice between FMC clocks or programmable clock using a differential 2:1 LVDS multiplexer (SY89543LMG component for example).

All clocks must be connected to MGTREFCLK for transceivers or MRCC pins for Multi-Region Clock Capable.

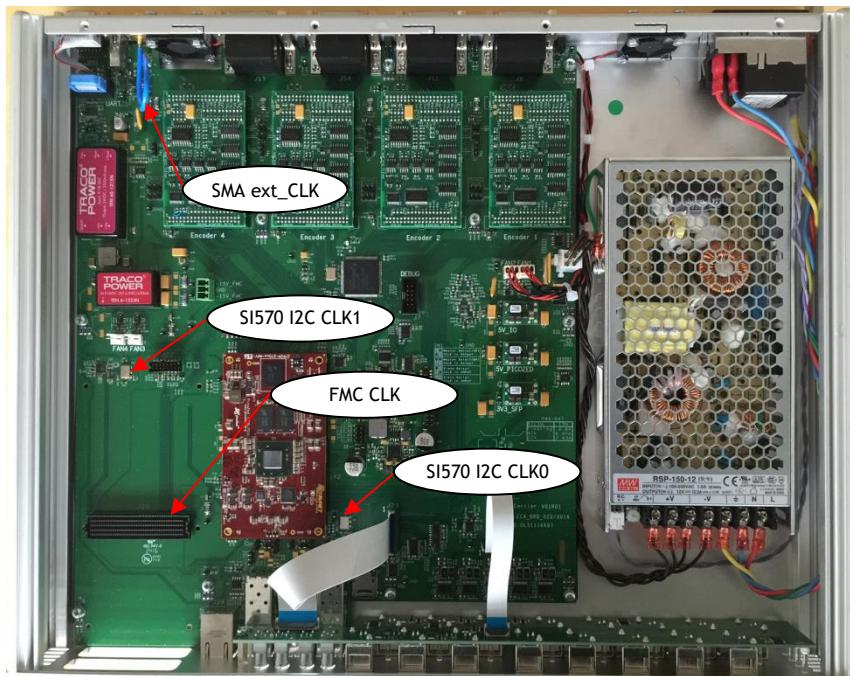


FIGURE 30: ONBOARD CLOCK TREE IN PANDABOX

Control of the clocks selection are done from Slow-FPGA I2C_CLOCK signals and transmitted to through TCA9543A I2C SMBUS Switch to the two SI570 programmable clock generators.

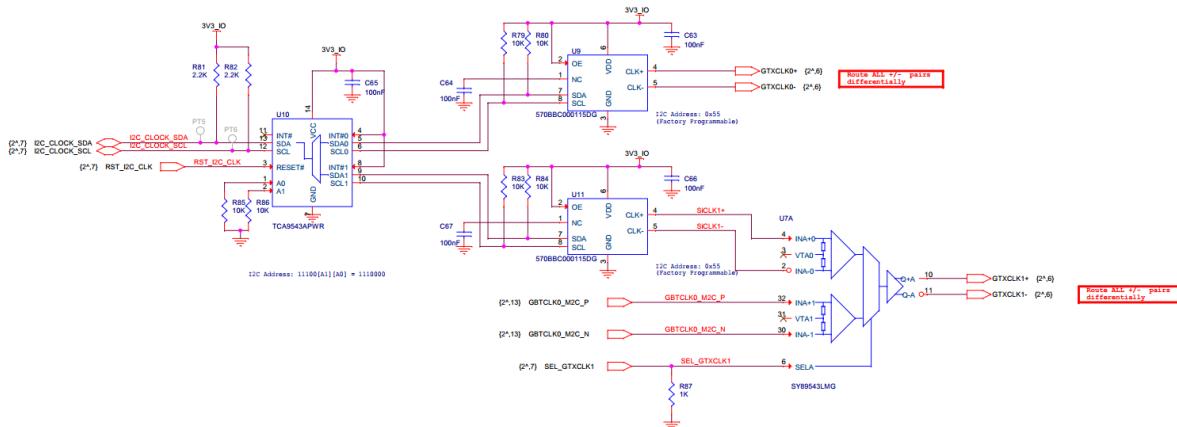


FIGURE 31: CARRIER BOARD CLOCK SWITCH SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 16: CLOCK TREE CONTROL PIN ASSIGNMENT ON SLOW FPGA

Slow FPGA Pin#	Slow FPGA Pin Name	Function (LM75AIM/NOPB)
141	IO_L2N_0	I2C_CLOCK_SDA
142	IO_L2P_0	I2C_CLOCK_SCL
143	IO_L1N_VREF_0	RST_I2C_CLK
144	IO_L1P_HSWAPEN_0	SEL_GTXCLK1

For complete description of Si570 IC(570BBC000115DG) used on Carrier board see:
<https://www.silabs.com/documents/public/data-sheets/si570.pdf>

For complete description of SFP I2C switch IC(TCA9543a) used on Carrier board see:
<http://www.ti.com/lit/ds/scps206a/scps206a.pdf>

2.2.14. ON-BOARD TEMPERATURE SENSORS

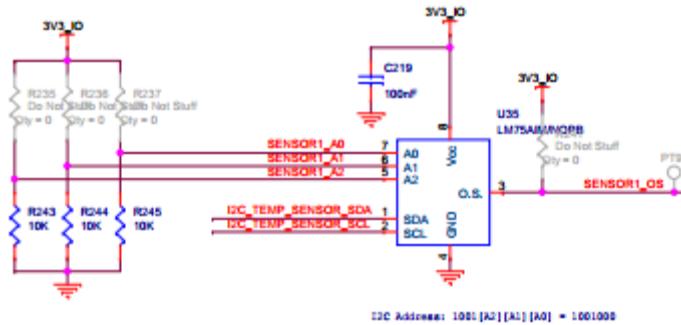


FIGURE 32: TEMPERATURE SENSOR SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 17: I2C VOLTAGE MONITOR PIN ASSIGNMENT ON SLOW FPGA

Slow FPGA Pin#	Slow FPGA Pin Name	Function (LM75AIM/NOPB)
61	IO_L12N_D2_MIS03_2	I2C_TEMP_SENSOR_SDA
62	IO_L12P_D1_MIS02_2	I2C_TEMP_SENSOR_SCL

TABLE 18: I2C VOLTAGE MONITOR ADDRESS

SPI Address	Function	Board physical placement
1001000	SENSOR1	near power supply component
1001001	SENSOR2	near SFPs connector
1001010	SENSOR3	close to ENCODER on the left
1001011	SENSOR4	under picozed board
1001100	SENSOR5	some quiet place on ENCODER right

(See Figure 33 for Temperature sensors placement in PandA BOX)

For complete description of the temperatures monitors IC(LM75AIM/NOPB) used on Carrier board see: <http://www.ti.com/lit/ds/symlink/lm75a.pdf>

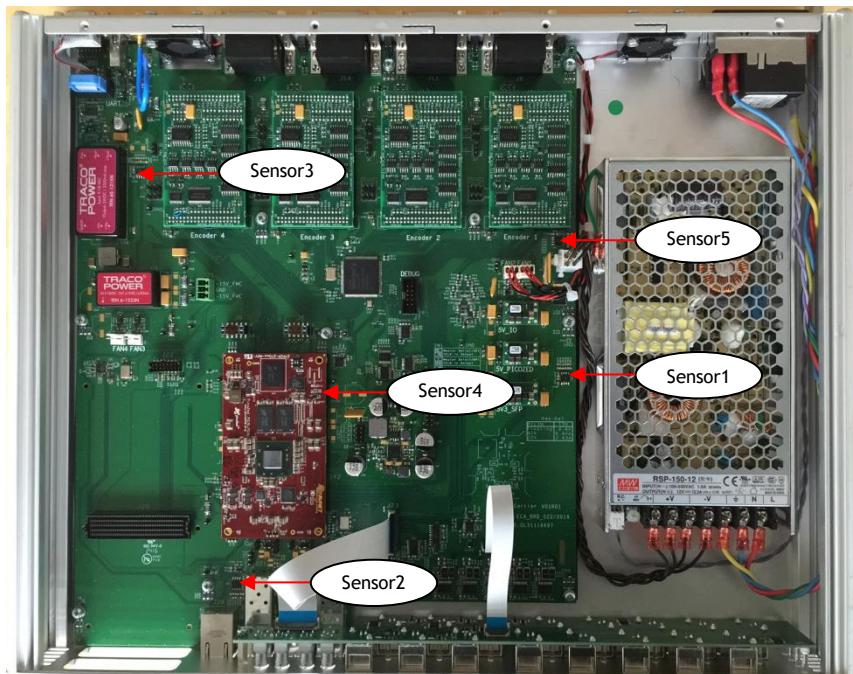


FIGURE 33: TEMPERATURE SENSORS PLACEMENT IN PANDA BOX

2.2.15. ON-BOARD VOLTAGE MONITORING

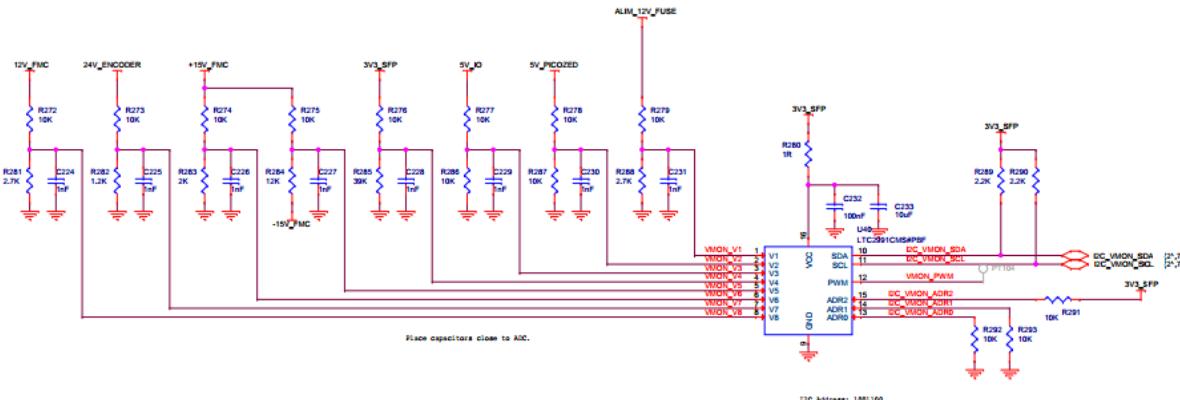


FIGURE 34: VOLTAGE MONITOR SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

TABLE 19: I2C VOLTAGE MONITOR PIN ASSIGNMENT ON SLOW FPGA

Slow FPGA Pin#	Slow FPGA Pin Name	Function
84	IO_L43N_GCLK4_1	I2C_VMON_SDA
85	IO_L43P_GCLK5_1	I2C_VMON_SCL

TABLE 20: I2C VOLTAGE MONITOR ADDRESS

SPI Address	Function
1001100	Voltage monitor (LTC2991CMS#PBF)

TABLE 21: I2C VOLTAGE MONITOR INPUT VOLTAGES ASSIGMENT

input voltages name	Voltage net name
V1	ALIM_12V_FUSE
V2	5V_PICOZED
V3	5V_IO
V4	3V3_SFP
V5	+15V_FMC/-15V_FMC
V6	+15V_FMC (to Ground)
V7	24V_ENCODER
V8	12V_FMC

For complete description of the Voltage monitor IC (LTC2991CMS#PBF) used on Carrier board see : <http://cds.linear.com/docs/en/datasheet/2991ff.pdf>

2.2.15.1. Power distribution block

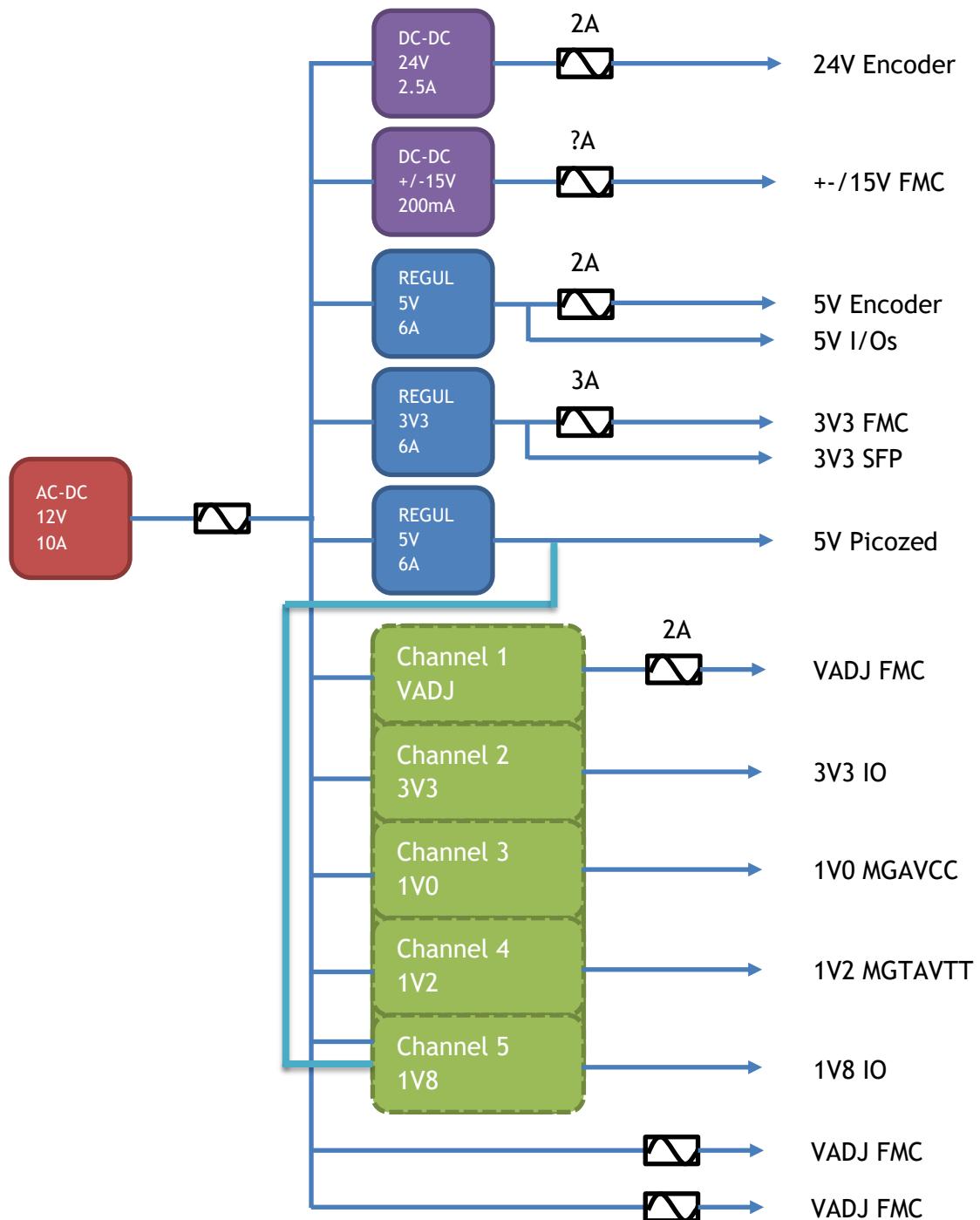


FIGURE 35 : POWER DISTRIBUTION ARCHITECTURE

2.2.16. ON-BOARD FAN TACHYMETRER

PandA handles 2 fans on the rear panel to improve airflow on the rack. Tachymeter will be used to know if fans are still alive.

TABLE 22: FAN PINOUT CONNECTOR

J29, J30, J31, J32 Pin#	Function
1	GND
2	+12V
3	FAN Tachymeter

The Tachymeter information is powered by +12V. An adaptation is used to protect the slow FPGA.

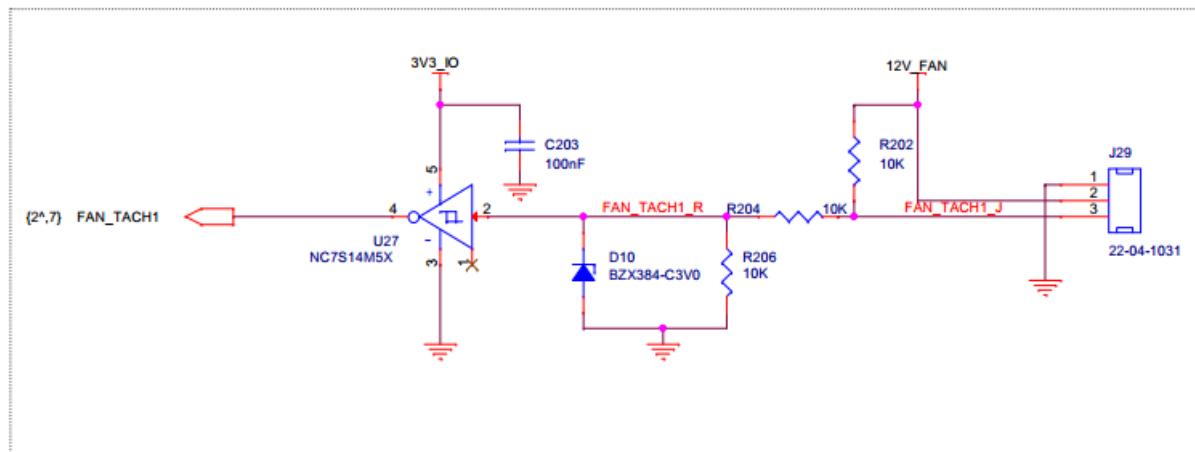


FIGURE 36 : FAN TACHYMETRER PROTECTION SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

Pin assignment on Slow FPGA of the four Tachymeters information can be found on following Table 23.

TABLE 23: TACHYMETRER PIN ASSIGNMENT ON SLOW FPGA

Slow FPGA Pin#	Slow FPGA Pin Name	Function
1	IO_L83N_VREF_3	Fan_TACH1
2	IO_L83P_3	Fan_TACH2
95	IO_L40P_GCLK11_1	Fan_TACH3
94	IO_L40N_GCLK10_1	Fan_TACH4

For complete description of the fans used in Pandabox see:

<https://www.sepa-europe.com/sites/sepa-europe.com/content/pdfs/en/mfb30gxx.pdf>

or <http://www.nidec-copal-electronics.com/e/catalog/dc-fan/f310r.pdf>

2.2.17. ON BOARD COMPACT FLASH

PandA includes a microSD card socket with four lines for data transfer. It respects the following interface.

TABLE 24: MICROSD PINOUT ON PICOZED

Net Name	JX3 Pin#	JX3 Pin#	Net Name
SD_D0	37	34	SD_CMD
SD_D2	39	36	SD_D1
SD_CD	41	38	SD_D3
SD_CLK	43	-	-

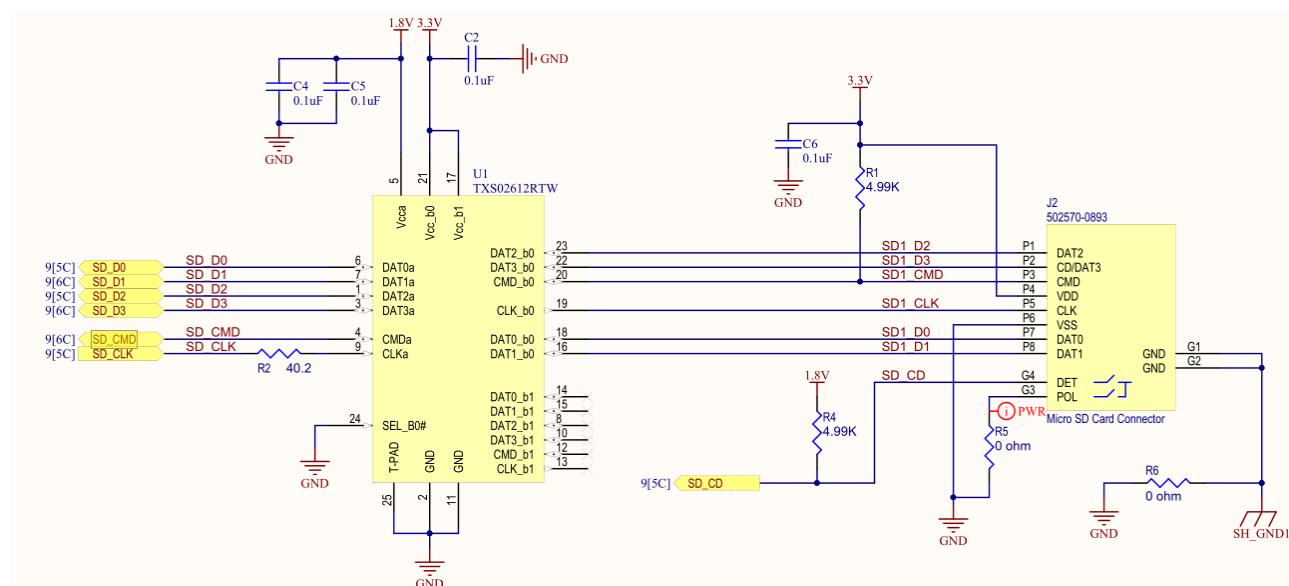


FIGURE 37 : MICROSD SCHEMATIC

(Note: The source of this schematic can be found in §1.2.1 Panda CARRIER board schematic)

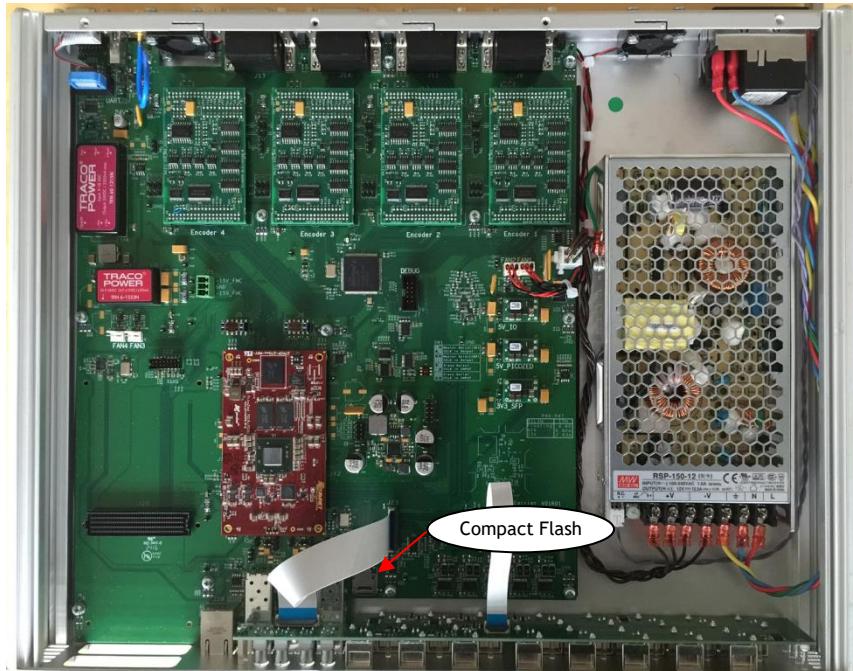


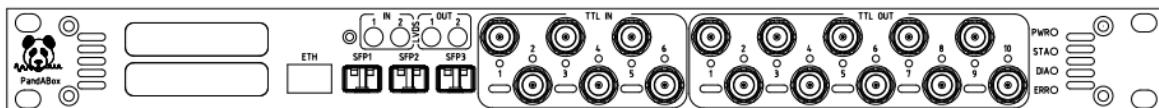
FIGURE 38: ONBOARD COMPACT FLASH IN PANDABOX

3. APPENDIX

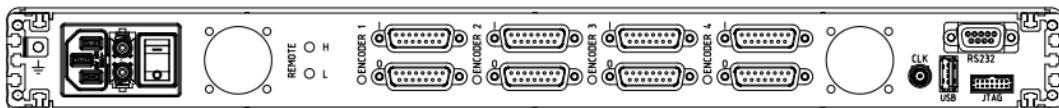
3.1. PANDABOX REAR AND FRONT PANELS

TABLE 25: PANDABOX REAR AND FRONT PANELS

FRONT VIEW



REAR VIEW



PandABox V01R02

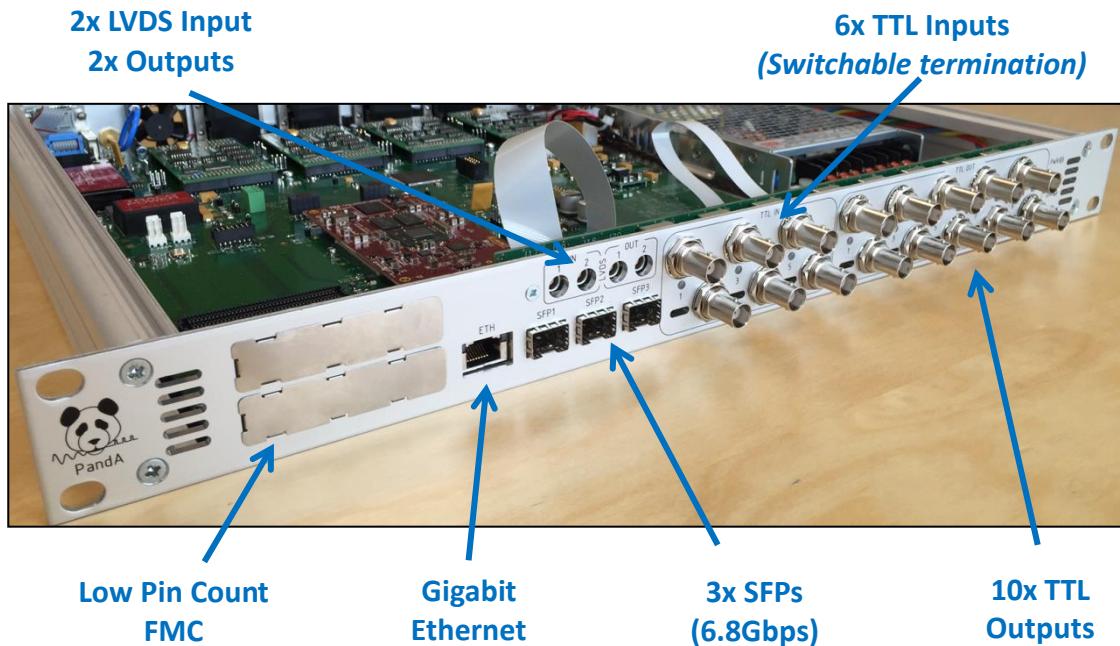


FIGURE 39 : PANDABOX FRONT SIDE PHOTO

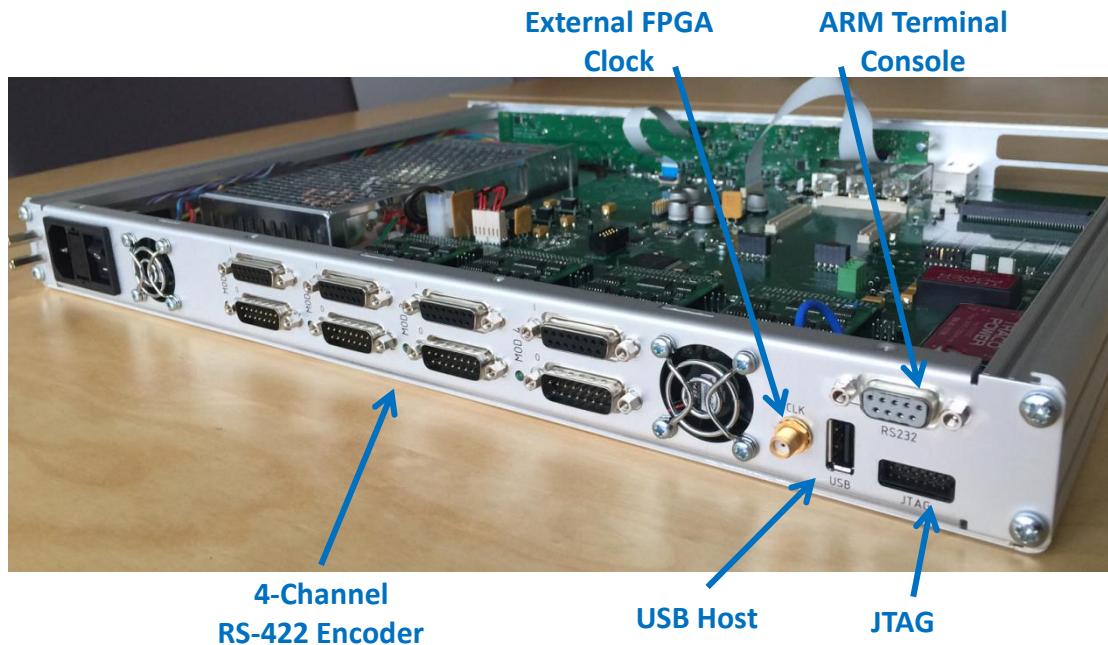


FIGURE 40 : PANDA BOX BACK SIDE PHOTO

3.2. PANDA BOX DEFAULT SWITCH AND JUMPER SETTINGS

3.2.1. CARRIER BOARD ENCODER CONFIGURATION JUMPERS

Ref	Function/type		default
JP7	Encoder 1 5V source selection :		Jump 1-2
	short 1-2	5V from PandaBox	
	short 2-3	5V from encoder	
JP4	Encoder 1 to Encoder 2 5V link :		No Jumper
	No Jumper	encoders 5V isolated	
	short 1-2	encoders 5V linked	
JP11 & JP12	Encoder 1 V_ENC_MEZ source selection :		Jump 1-2
	short 1-2	+24V/0V	
	short 2-3	+15V/-15V	
JP1	Encoder 1 to Encoder 2 V_ENC_MEZ link :		No Jumper
	No Jumper	encoders V_ENC_MEZ isolated	
	short 1-2	encoders V_ENC_MEZ linked	
JP8	Encoder 2 5V source selection :		Jump 1-2
	short 1-2	5V from PandaBox	
	short 2-3	5V from encoder	
JP5	Encoder 2 to Encoder 3 5V link :		No Jumper
	No Jumper	encoders 5V isolated	
	short 1-2	encoders 5V linked	
JP13 & JP14	Encoder 2 V_ENC_MEZ source selection :		Jump 1-2
	short 1-2	+24V/0V	
	short 2-3	+15V/-15V	
JP2	Encoder 2 to Encoder 3 V_ENC_MEZ link :		No Jumper
	No Jumper	encoders V_ENC_MEZ isolated	
	short 1-2	encoders V_ENC_MEZ linked	
JP9	Encoder 3 5V source selection :		Jump 1-2
	short 1-2	5V from PandaBox	
	short 2-3	5V from encoder	
JP6	Encoder 3 to Encoder 4 5V link :		No Jumper
	No Jumper	encoders 5V isolated	
	short 1-2	encoders 5V linked	
JP15 & JP16	Encoder 3 V_ENC_MEZ source selection :		Jump 1-2
	short 1-2	+24V/0V	
	short 2-3	+15V/-15V	
JP3	Encoder 3 to Encoder 4 V_ENC_MEZ link :		No Jumper
	No Jumper	encoders V_ENC_MEZ isolated	
	short 1-2	encoders V_ENC_MEZ linked	
JP10	Encoder 4 5V source selection :		Jump 1-2
	short 1-2	5V from PandaBox	
	short 2-3	5V from encoder	
JP17 & JP18	Encoder 4 V_ENC_MEZ source selection :		Jump 1-2
	short 1-2	+24V/0V	
	short 2-3	+15V/-15V	

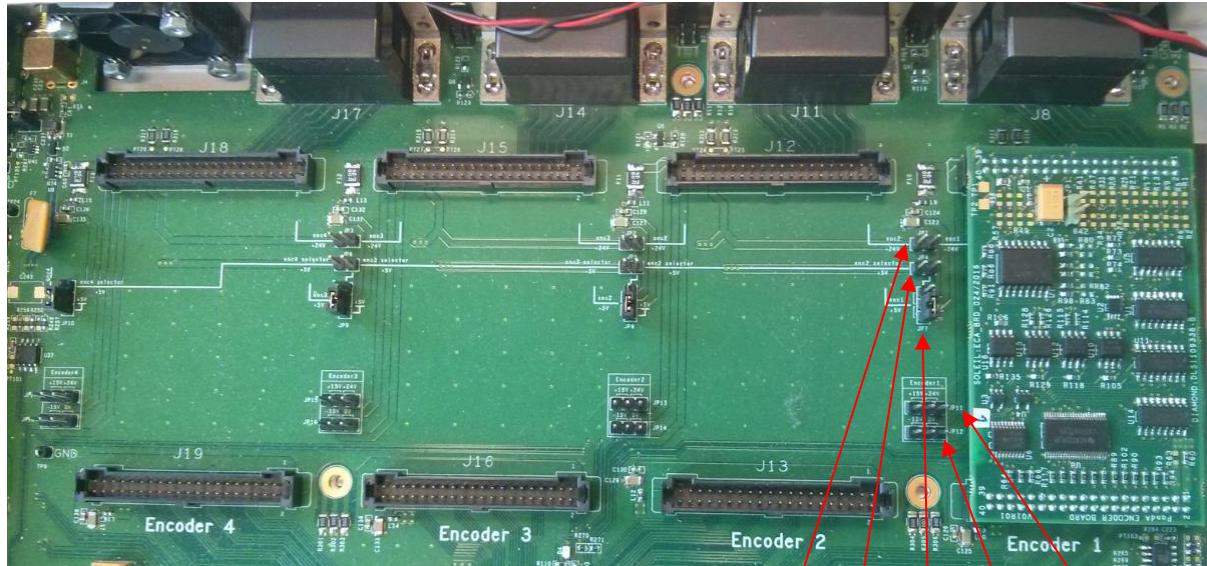


FIGURE 41: CARRIER BOARD ENCODER 1 JUMPERS JP1, JP7, JP4, JP12, JP11

3.2.2. CARRIER BOARD SFP CONFIGURATION JUMPERS

Ref	Function/type		default
JP19	SFP 3 Tx enable Selection :		Jump 1-2
	short 1-2	Optical output enabled	
	No Jumper	Optical output disabled	
JP20	SFP 3 Rate selection :		No Jumper
	No Jumper	LOW Rate	
	short 1-2	FULL Rate	
	short 2-3	LOW Rate	
JP21	SFP 2 Tx enable Selection :		Jump 1-2
	short 1-2	Optical output enabled	
	No Jumper	Optical output disabled	
JP22	SFP 2 Rate selection :		No Jumper
	No Jumper	LOW Rate	
	short 1-2	FULL Rate	
	short 2-3	LOW Rate	
JP23	SFP 1 Tx enable Selection :		Jump 1-2
	short 1-2	Optical output enabled	
	No Jumper	Optical output disabled	
JP24	SFP 1 Rate selection :		No Jumper
	No Jumper	LOW Rate	
	short 1-2	FULL Rate	
	short 2-3	LOW Rate	

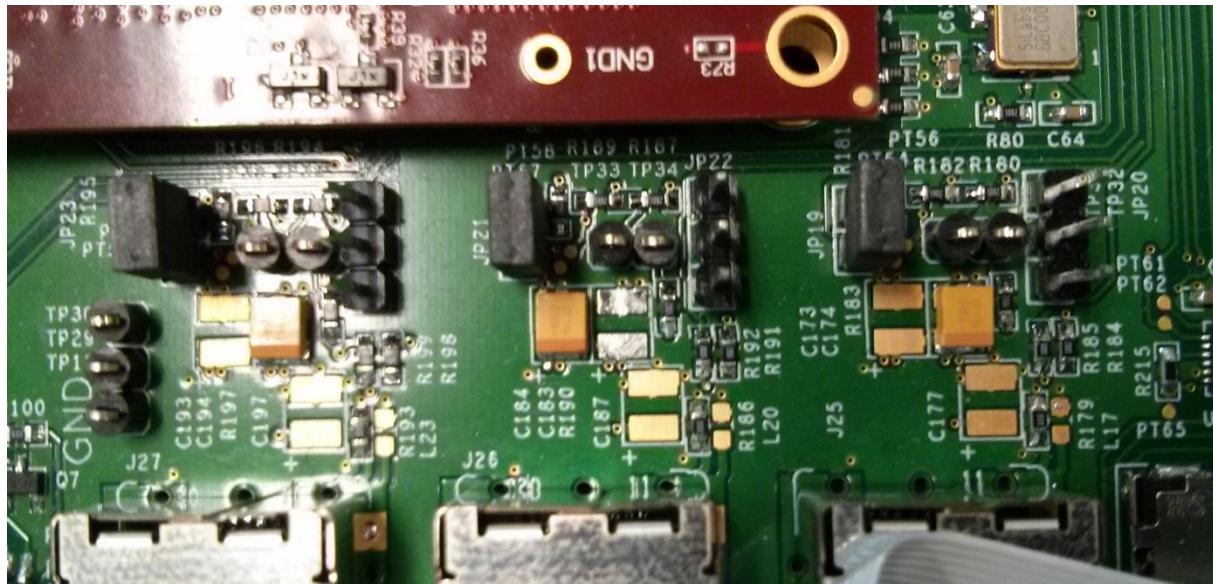


FIGURE 42: CARRIER BOARD SFP DEFAULT JUMPERS JP19, JP21, JP23=JUMPER 1-2

3.2.3. CARRIER BOARD SLOW FPGA BOOT MODE CONFIGURATION SWITCH

Ref	Function/type	default
SW1	Boot mode Selection :	
	00 Master SelectMAP/BPI CCLK as output (from PROM)*	
	10 Master Serial/SPI CCLK as output(from PROM)	
	01 Slave SelectMAP CCLK as input (from ZYNQ)*	
	11 Slave Serial CCLK as input (from ZYNQ)	

*: Parallel mode is not supported (additionnal data input should be used in slow fpga)



FIGURE 43: CARRIER BOARD SW1 = 10 (FROM PROM)



FIGURE 44: CARRIER BOARD SW1 = 11 (FROM ZYNC)

3.2.4. CARRIER BOARD USB CONFIGURATION JUMPERS

Ref	Function/type		default
JP25	USB mode :		Jump 1-2
	short 1-2	Host/Device Mode	
	short 2-3	OTG Mode	
JP26	Host or Device mode selection :		Jump 1-2
	short 1-2	Additional capacitor (Host Mode)	
	No Jumper	NO additional capacitor (Device Mode)	



FIGURE 45: CARRIER BOARD USB DEFAULT JUMPERS JP25 AND JP26= JUMPER 1-2

3.2.5. CARRIER BOARD PICOZED POWER CONFIGURATION JUMPERS

Ref	Function/type		default
J2	VADJ voltage selection for picoZ VCCO_35, VCCO_34 and FMC module VADJ:		No Jumper
	No Jumper	VADJ=1.8V	
	short 1-2	VADJ=1.8V	
	short 3-4	VADJ=1.8V	
	short 5-6	VADJ=2.5V	
	short 7-8	VADJ=3.3V	
J3	Voltage monitor (monitor only no jumper allowed):		No Jumper
	Pin 1	Vadj	
	Pin 3	VCC3V3 slow_fpga 3V3_IO and encoder 3V3 front led 3V3	
	Pin 5	VCC1V0 1V0_MGTAVCC for picozed gigabit transceivers	
	Pin 9	VCC1V8 1V8_IO uart led microSD level shifter 1.8V<>3.3V VCCO_13 picozed VCCO_13	
	Pin 2, 4, 6, 8	Ground	

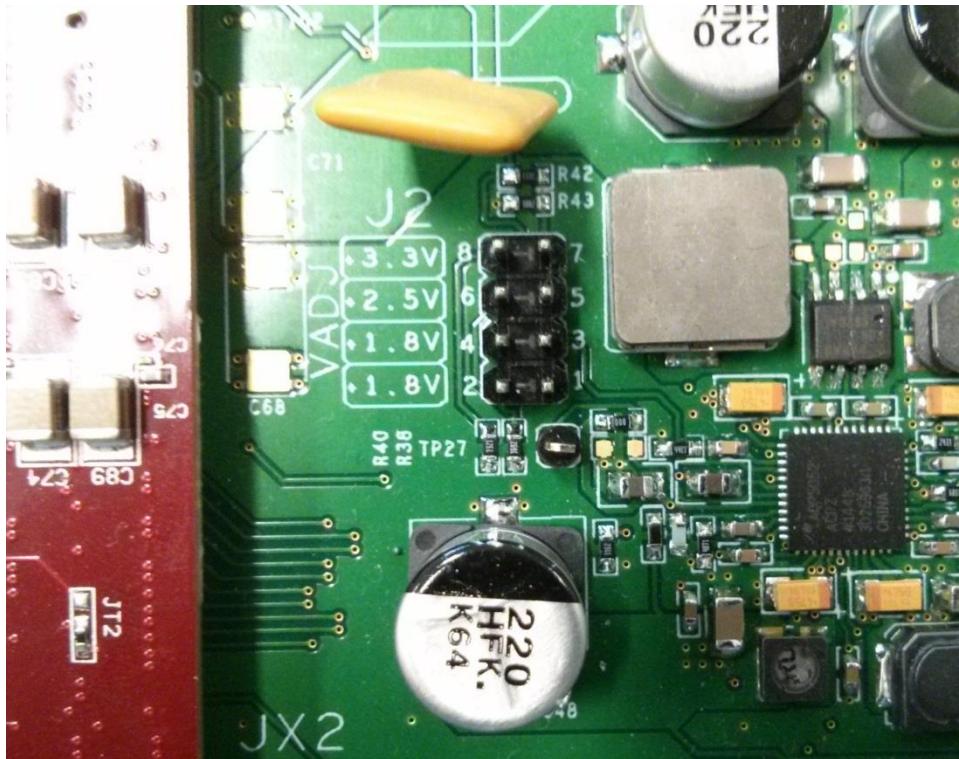


FIGURE 46: CARRIER BOARD VADJ DEFAULT JUMPERS J2 = NO JUMPER

3.3. PANDA-PICOZED PINS ASSIGNEMENT

3.3.1. PICOZED JX1 CONNECTOR

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME_pico carrier	IO	SFP	J5 Pin/Name
JX1	1	JTAG_TCK	0-H11						
JX1	2	JTAG_TMS	0-H10						
JX1	3	JTAG_TDO	0-G9						
JX1	4	JTAG_TDI	0-H9						
JX1	5	PWR_ENABLE	N/A						
JX1	6	CARRIER_SRST#	N/A						
JX1	7	FPGA_VBATT	N/A						
JX1	8	FPGA_DONE	500-T10						
JX1	9	JX1_SE_0	35-H6						2/JX1_35_SE_0
JX1	10	JX1_SE_1	35-H5						1/JX1_35_SE_1
JX1	11	JX1_LVDS_0_P	35-H4		g9	LA03_P			
JX1	12	JX1_LVDS_1_P	35-F5		h7	LA02_P			
JX1	13	JX1_LVDS_0_N	35-H3		g10	LA03_N			
JX1	14	JX1_LVDS_1_N	35-E5		h8	LA02_N			
JX1	15	GND	N/A						
JX1	16	GND	N/A						
JX1	17	JX1_LVDS_2_P	35-G3		g12	LA08_P			
JX1	18	JX1_LVDS_3_P	35-F2		h10	LA04_P			
JX1	19	JX1_LVDS_2_N	35-G2		g13	LA08_N			
JX1	20	JX1_LVDS_3_N	35-F1		h11	LA04_N			
JX1	21	GND	N/A						
JX1	22	GND	N/A						
JX1	23	JX1_LVDS_4_P	35-G4		g15	LA12_P			

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME_pico carrier	IO	SFP	J5 Pin/Name
JX1	24	JX1_LVDS_5_P	35-E4		h13	LA07_P			
JX1	25	JX1_LVDS_4_N	35-F4		g16	LA12_N			
JX1	26	JX1_LVDS_5_N	35-E3		h14	LA07_N			
JX1	27	GND	N/A						
JX1	28	GND	N/A						
JX1	29	JX1_LVDS_6_P	35-G6		g18	LA16_P			
JX1	30	JX1_LVDS_7_P	35-B2		H16	LA11_P			
JX1	31	JX1_LVDS_6_N	35-F6		g19	LA16_N			
JX1	32	JX1_LVDS_7_N	35-B1		H17	LA11_N			
JX1	33	GND	N/A						
JX1	34	GND	N/A						
JX1	35	JX1_LVDS_8_P	35-E8		g21	LA20_P			
JX1	36	JX1_LVDS_9_P	35-H1		h19	LA15_P			
JX1	37	JX1_LVDS_8_N	35-D8		g22	LA20_N			
JX1	38	JX1_LVDS_9_N	35-G1		h20	LA15_N			
JX1	39	GND	N/A						
JX1	40	GND	N/A						
JX1	41	JX1_LVDS_10_P	35-C6		g24	LA22_P			
JX1	42	JX1_LVDS_11_P	35-D5		h22	LA19_P			
JX1	43	JX1_LVDS_10_N	35-C5		g25	LA22_N			
JX1	44	JX1_LVDS_11_N	35-C4		h23	LA19_N			
JX1	45	GND	N/A						
JX1	46	GND	N/A						
JX1	47	JX1_LVDS_12_P	35-B4		g2	CLK1_M2C_P			
JX1	48	JX1_LVDS_13_P	35-D3		g6	LA00_CC_P			
JX1	49	JX1_LVDS_12_N	35-B3		g3	CLK1_M2C_N			
JX1	50	JX1_LVDS_13_N	35-C3		g7	LA00_CC_N			
JX1	51	GND	N/A						
JX1	52	GND	N/A						

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME_pico carrier	IO	SFP	J5 Pin/Name
JX1	53	JX1_LVDS_14_P	35-D1		d8	LA01_CC_P			
JX1	54	JX1_LVDS_15_P	35-A2		h25	LA21_P			
JX1	55	JX1_LVDS_14_N	35-C1		d9	LA01_CC_N			
JX1	56	JX1_LVDS_15_N	35-A1		h26	LA21_N			
JX1	57	VIN	N/A						
JX1	58	VIN	N/A						
JX1	59	VIN	N/A						
JX1	60	VIN	N/A						
JX1	61	JX1_LVDS_16_P	35-E2		g27	LA25_P			
JX1	62	JX1_LVDS_17_P	35-D7		h28	LA24_P			
JX1	63	JX1_LVDS_16_N	35-D2		g28	LA25_N			
JX1	64	JX1_LVDS_17_N	35-D6		h29	LA24_N			
JX1	65	GND	N/A						
JX1	66	GND	N/A						
JX1	67	JX1_LVDS_18_P	35-F7		g30	LA29_P			
JX1	68	JX1_LVDS_19_P	35-A5		h31	LA28_P			
JX1	69	JX1_LVDS_18_N	35-E7		g31	LA29_N			
JX1	70	JX1_LVDS_19_N	35-A4		h32	LA28_N			
JX1	71	GND	N/A						
JX1	72	GND	N/A						
JX1	73	JX1_LVDS_20_P	35-G8		g33	LA31_P			
JX1	74	JX1_LVDS_21_P	35-A7		h34	LA30_P			
JX1	75	JX1_LVDS_20_N	35-G7		g34	LA31_N			
JX1	76	JX1_LVDS_21_N	35-A6		h35	LA30_N			
JX1	77	GND	N/A						
JX1	78	VCCO_34	N/A						
JX1	79	VCCO_34	N/A						
JX1	80	VCCO_34	N/A						
JX1	81	JX1_LVDS_22_P	35-B7		g36	LA33_P			

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME_pico carrier	IO	SFP	J5 Pin/Name
JX1	82	JX1_LVDS_23_P	35-C8		h37	LA32_P			
JX1	83	JX1_LVDS_22_N	35-B6		g37	LA33_N			
JX1	84	JX1_LVDS_23_N	35-B8		h38	LA32_N			
JX1	85	GND	N/A						
JX1	86	GND	N/A						
JX1	87	BANK13_LVDS_0_P	13-AA14	Z-in1					
JX1	88	BANK13_LVDS_1_P	13-Y14	Z-in2					
JX1	89	BANK13_LVDS_0_N	13-AA15	Z-in3					
JX1	90	BANK13_LVDS_1_N	13-Y15	Z-in4					
JX1	91	BANK13_LVDS_2_P	13-U19	Z-out1					
JX1	92	BANK13_LVDS_3_P	13-V18	Z-out2					
JX1	93	BANK13_LVDS_2_N	13-V19	Z-out3					
JX1	94	BANK13_LVDS_3_N	13-W18	Z-out4					
JX1	95	GND	N/A						
JX1	96	GND	N/A						
JX1	97	VP_0_P	0-L12						4/JX1_V_0_P
JX1	98	DXP_0_P	0-N12						3/JX1_DX_0_P
JX1	99	VN_0_N	0-M11						6/JX1_V_0_N
JX1	100	DXN_0_N	0-N11						5/JX1_DX_0_N

3.3.2. PICOZED JX2 CONNECTOR

JX	Pin #	Net Name JX	B-pin	FMC Pin	FMC_NAME pico carrier	IO	SFP	Spartan	J5 Pin/Name
JX2	1	MIO10	500-G16						
JX2	2	MIO13	500-A17						
JX2	3	MIO14	500-B17						
JX2	4	MIO15	500-E17						
JX2	5	MIO12	500-C18						
JX2	6	MIO11	500-B19						
JX2	7	MIO0	500-G17						
JX2	8	MIO9	500-C19						
JX2	9	INIT#	0-T8						
JX2	10	PG_1V8	N/A						
JX2	11	PG_MODULE	N/A	d1	PG_C2M/ PG_MODULE				
JX2	12	VIN	N/A						
JX2	13	JX2_SE_0	34-H8					9/JX2_34_SE_0	
JX2	14	JX2_SE_1	34-R8	h2	FMC_PRSNT (via transistor)				
JX2	15	GND	N/A						
JX2	16	GND	N/A						
JX2	17	JX2_LVDS_0_P	34-M4			TTL_IN0			
JX2	18	JX2_LVDS_1_P	34-J2			TTL_IN1			
JX2	19	JX2_LVDS_0_N	34-M3			TTL_IN2			
JX2	20	JX2_LVDS_1_N	34-J1			TTL_IN3			
JX2	21	GND	N/A						
JX2	22	GND	N/A						
JX2	23	JX2_LVDS_2_P	34-K7			TTL_IN4			
JX2	24	JX2_LVDS_3_P	34-J3			TTL_IN5			
JX2	25	JX2_LVDS_2_N	34-L7			TTL_OUT8			
JX2	26	JX2_LVDS_3_N	34-K2			TTL_OUT9			

JX	Pin #	Net Name JX	B-pin	FMC Pin	FMC_NAME pico carrier	IO	SFP	Spartan	J5 Pin/Name
JX2	27	GND	N/A						
JX2	28	GND	N/A						
JX2	29	JX2_LVDS_4_P	34-P7			TTL_OUT0			
JX2	30	JX2_LVDS_5_P	34-L2			TTL_OUT1			
JX2	31	JX2_LVDS_4_N	34-R7			TTL_OUT2			
JX2	32	JX2_LVDS_5_N	34-L1			TTL_OUT3			
JX2	33	GND	N/A						
JX2	34	GND	N/A						
JX2	35	JX2_LVDS_6_P	34-N4			TTL_OUT4			
JX2	36	JX2_LVDS_7_P	34-P3			TTL_OUT5			
JX2	37	JX2_LVDS_6_N	34-N3			TTL_OUT6			
JX2	38	JX2_LVDS_7_N	34-P2			TTL_OUT7			
JX2	39	GND	N/A						
JX2	40	GND	N/A						
JX2	41	JX2_LVDS_8_P	34-M2			LVDS_IN0			
JX2	42	JX2_LVDS_9_P	34-N1			LVDS_IN1			
JX2	43	JX2_LVDS_8_N	34-M1			LVDS_OUT0			
JX2	44	JX2_LVDS_9_N	34-P1			LVDS_OUT1			
JX2	45	GND	N/A						
JX2	46	GND	N/A						
JX2	47	JX2_LVDS_10_P	34-K4				sclk		
JX2	48	JX2_LVDS_11_P	34-L5	d20	LA17_CC_P				
JX2	49	JX2_LVDS_10_N	34-K3				sdci		
JX2	50	JX2_LVDS_11_N	34-L4	d21	LA17_CC_N				
JX2	51	GND	N/A						
JX2	52	GND	N/A						
JX2	53	JX2_LVDS_12_P	34-T2	h4	CLK0_M2C_P				
JX2	54	JX2_LVDS_13_P	34-U2	c22	LA18_CC_P				
JX2	55	JX2_LVDS_12_N	34-T1	h5	CLK0_M2C_N				

JX	Pin #	Net Name JX	B-pin	FMC Pin	FMC_NAME pico carrier	IO	SFP	Spartan	J5 Pin/Name
JX2	56	JX2_LVDS_13_N	34-U1	c23	LA18_CC_N				
JX2	57	VIN	N/A						
JX2	58	VIN	N/A						
JX2	59	VIN	N/A						
JX2	60	VIN	N/A						
JX2	61	JX2_LVDS_14_P	34-R3	d11	LA05_P				
JX2	62	JX2_LVDS_15_P	34-L6	c10	LA06_P				
JX2	63	JX2_LVDS_14_N	34-R2	d12	LA05_N				
JX2	64	JX2_LVDS_15_N	34-M6	c11	LA06_N				
JX2	65	GND	N/A						
JX2	66	GND	N/A						
JX2	67	JX2_LVDS_16_P	34-J5	d14	LA09_P				
JX2	68	JX2_LVDS_17_P	34-R5	c14	LA10_P				
JX2	69	JX2_LVDS_16_N	34-K5	d15	LA09_N				
JX2	70	JX2_LVDS_17_N	34-R4	c15	LA10_N				
JX2	71	GND	N/A						
JX2	72	GND	N/A						
JX2	73	JX2_LVDS_18_P	34-J7	d17	LA13_P				
JX2	74	JX2_LVDS_19_P	34-P6	c18	LA14_P				
JX2	75	JX2_LVDS_18_N	34-J6	d18	LA13_N				
JX2	76	JX2_LVDS_19_N	34-P5	c19	LA14_N				
JX2	77	GND	N/A						
JX2	78	VCCO_35	N/A						
JX2	79	VCCO_35	N/A						
JX2	80	VCCO_35	N/A						
JX2	81	JX2_LVDS_20_P	34-J8	d23	LA23_P				
JX2	82	JX2_LVDS_21_P	34-N6	c26	LA27_P				
JX2	83	JX2_LVDS_20_N	34-K8	d24	LA23_N				
JX2	84	JX2_LVDS_21_N	34-N5	c27	LA27_N				

JX	Pin #	Net Name JX	B-pin	FMC Pin	FMC_NAME pico carrier	IO	SFP	Spartan	J5 Pin/Name
JX2	85	GND	N/A						
JX2	86	GND	N/A						
JX2	87	JX2_LVDS_22_P	34-M8	d26	LA26_P				
JX2	88	JX2_LVDS_23_P	34-N8						SCS
JX2	89	JX2_LVDS_22_N	34-M7	d27	LA26_N				
JX2	90	JX2_LVDS_23_N	34-P8						sdo
JX2	91	GND	N/A						
JX2	92	GND	N/A						
JX2	93	BANK13_LVDS_4_P	13-AB21						SFP1_IO1
JX2	94	BANK13_LVDS_5_P	13-AB18						SFP1_IO2
JX2	95	BANK13_LVDS_4_N	13-AB22						SFP2_IO1
JX2	96	BANK13_LVDS_5_N	13-AB19						SFP2_IO2
JX2	97	BANK13_LVDS_6_P	13-AA19						GPIO_01_P
JX2	98	VCCO_13	N/A						
JX2	99	BANK13_LVDS_6_N	13-AA20						GPIO_01_N
JX2	100	BANK13_SE_0	13-T16						7/JX2_13_SE_0

3.3.3. PICOZED JX3 CONNECTOR

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME pico carrier	IO	spartan	SFP	CLOCK
JX3	1	MGTREFCLK0_P	112-U9							GTXCLK0+
JX3	2	MGTREFCLK1_P	112-U5							GTXCLK1+
JX3	3	MGTREFCLK0_N	112-V9							GTXCLK0-
JX3	4	MGTREFCLK1_N	112-V5							GTXCLK1-
JX3	5	MGTAVCC	N/A							
JX3	6	GND	N/A							
JX3	7	MGTAVCC	N/A							
JX3	8	MGTRX0_P	112-AA7		C6	FMC_DP0_M2C_P				
JX3	9	MGTAVCC	N/A							
JX3	10	MGTRX0_N	112-AB7		C7	FMC_DP0_M2C_N				
JX3	11	MGTAVCC	N/A							
JX3	12	GND	N/A							
JX3	13	MGTTX0_P	112-AA3		C2	FMC_DP0_C2M_P				
JX3	14	MGTRX1_P	112-W8							SFP1_RX_P
JX3	15	MGTTX0_N	112-AB3		C3	FMC_DP0_C2M_N				
JX3	16	MGTRX1_N	112-Y8							SFP1_RX_N
JX3	17	GND	N/A							
JX3	18	GND	N/A							
JX3	19	MGTTX1_P	112-W4							SFP1_TX_P
JX3	20	MGTRX2_P	112-AA9							SFP2_RX_P
JX3	21	MGTTX1_N	112-Y4							SFP1_TX_N
JX3	22	MGTRX2_N	112-AB9							SFP2_RX_N
JX3	23	GND	N/A							
JX3	24	GND	N/A							
JX3	25	MGTTX2_P	112-AA5							SFP2_TX_P
JX3	26	MGTRX3_P	112-W6							SFP3_RX_P
JX3	27	MGTTX2_N	112-AB5							SFP2_TX_N

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME pico carrier	IO	spartan	SFP	CLOCK
JX3	28	MGTRX3_N	112-Y6						SFP3_RX_N	
JX3	29	GND	N/A							
JX3	30	MGTAVTT	N/A							
JX3	31	MGTTX3_P	112-W2						SFP3_TX_P	
JX3	32	MGTAVTT	N/A							
JX3	33	MGTTX3_N	112-Y2						SFP3_TX_N	
JX3	34	PS_MIO41	501-C15							
JX3	35	GND	N/A							
JX3	36	PS_MIO43	501-B12							
JX3	37	PS_MIO42	501-D15							
JX3	38	PS_MIO45	501-B14							
JX3	39	PS_MIO44	501-E10							
JX3	40	PS_MIO47	501-B13							
JX3	41	PS_MIO46	501-D11							
JX3	42	PS_MIO48	501-D12							
JX3	43	PS_MIO40	501-E9							
JX3	44	PS_MIO49	501-C9							
JX3	45	VCCO_13	N/A							
JX3	46	VCCO_13	N/A							
JX3	47	ETH_PHY_LED0	N/A							
JX3	48	ETH_PHY_LED1	N/A							
JX3	49	GND	N/A							
JX3	50	GND	N/A							
JX3	51	ETH_MD1_P	N/A							
JX3	52	ETH_MD2_P	N/A							
JX3	53	ETH_MD1_N	N/A							
JX3	54	ETH_MD2_N	N/A							
JX3	55	GND	N/A							
JX3	56	GND	N/A							

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME pico carrier	IO	spartan	SFP	CLOCK
JX3	57	ETH_MD3_P	N/A							
JX3	58	ETH_MD4_P	N/A							
JX3	59	ETH_MD3_N	N/A							
JX3	60	ETH_MD4_N	N/A							
JX3	61	GND	N/A							
JX3	62	GND	N/A							
JX3	63	USB_ID	N/A							
JX3	64	PS_MIO51	501-C13							
JX3	65	GND	N/A							
JX3	66	PS_MIO50	501-D10							
JX3	67	USB_OTG_P	N/A							
JX3	68	USB_VBUS_OTG	N/A							
JX3	69	USB_OTG_N	N/A							
JX3	70	USB_OTG_COPEN	N/A							
JX3	71	GND	N/A							
JX3	72	GND	N/A							
JX3	73	BANK13_LVDS_7_P	13-Y18							EXTCLK+
JX3	74	BANK13_LVDS_8_P	13-AA16							
JX3	75	BANK13_LVDS_7_N	13-Y19							EXTCLK-
JX3	76	BANK13_LVDS_8_N	13-AA17							
JX3	77	GND	N/A							
JX3	78	GND	N/A							
JX3	79	BANK13_LVDS_9_P	13-AA11	B-in1						
JX3	80	BANK13_LVDS_10_P	13-Y12	B-in2						
JX3	81	BANK13_LVDS_9_N	13-AB11	B-in3						
JX3	82	BANK13_LVDS_10_N	13-Y13	B-in4						
JX3	83	GND	N/A							
JX3	84	GND	N/A							
JX3	85	BANK13_LVDS_11_P	13-V11	A-in1						

JX	Pin #	Net Name JX	B-pin	encoder	FMC Pin	FMC_NAME pico carrier	IO	spartan	SFP	CLOCK
JX3	86	BANK13_LVDS_12_P	13-V13	A-in2						
JX3	87	BANK13_LVDS_11_N	13-W11	A-in3						
JX3	88	BANK13_LVDS_12_N	13-V14	A-in4						
JX3	89	GND		N/A						
JX3	90	GND		N/A						
JX3	91	BANK13_LVDS_13_P	13-W12	B-o1						
JX3	92	BANK13_LVDS_14_P	13-R17	B-o2						
JX3	93	BANK13_LVDS_13_N	13-W13	B-o3						
JX3	94	BANK13_LVDS_14_N	13-T17	B-o4						
JX3	95	GND		N/A						
JX3	96	GND		N/A						
JX3	97	BANK13_LVDS_15_P	13-V15	A-o1						
JX3	98	BANK13_LVDS_16_P	13-V16	A-o2						
JX3	99	BANK13_LVDS_15_N	13-W15	A-o3						
JX3	100	BANK13_LVDS_16_N	13-W16	A-o4						

3.3.4. PICOZED CONNECTORS DESCRIPTION

MicroHeader #1 (JX1)			MicroHeader #2 (JX2)			
	Signal Name	Source	Signal Name	Source	Pin Count	
PL	Bank 34 I/Os (except for PUDC_B)	Zynq Bank 34 or Zynq Bank 35	49 ##	Bank 35 I/Os	Zynq Bank 35 or Zynq Bank 34	50 ##
	Bank 13 I/Os	Zynq Bank 13	8 **		Bank 13 I/Os	7 **
JTAG	TMS_0	Zynq Bank 0			PS MIO [0,9-15]	8
	TDI_0	Zynq Bank 0			Init_B_0	1
	TCK_0	Zynq Bank 0			VCCIO_EN	1
	TDO_0	Zynq Bank 0			PG_MODULE	1
	Carrier_SRST#	Carrier			Vin	5
Analog	VP_0	Zynq Bank 0			GND	23
	VN_0	Zynq Bank 0			VCCO_13	1
	DXP_0	Zynq Bank 0			VCCO_35	3
	DXN_0	Zynq Bank 0				
C	PUDC_B / IO	Zynq Bank 34				
	DONE	Zynq Bank 0				
Power	PWR_Enable	Carrier	1			
	Vin	Carrier	4			
	GND	Carrier	23			
	VCCO_34	Carrier	3			
	VBATT	Carrier	1			
TOTAL		100	TOTAL			100

** PicoZed 7015/7020/7030

PicoZed 7010/7020 Bank 34 and PicoZed 7015/7030 Bank 35

** PicoZed 7015/7020/7030

PicoZed 7010/7020 Bank 35 and PicoZed 7015/7030 Bank 34

MicroHeader #3 (JX3)			
	Signal Name	Source	Pin Count
PL	Bank 13 I/Os	Zynq Bank 13	20 **
	MGTTX I/Os	Zynq Bank 112	20 ##
XCV/R	MGTRX I/Os	Zynq Bank 112	
	MGTREFCLK I/Os	Zynq Bank 112	
	MIO[40-51]	Zynq Bank 501	25 @@
PS	ETHERNET	Zynq Bank 501	
	USB 2.0	Zynq Bank 500	
	USB_VBUS_OTG	Carrier	1
Power	VCCO_13	Carrier	2
	MGTAVCC	Carrier	4
	MGTAVTT	Carrier	2
	GND	Carrier	26
TOTAL		100	

** PicoZed 7020 has 10 I/O and PicoZed 7015/7030 adds 20 I/O

PicoZed 7015/7030 only

@@ MIO[47] not on JX3

FIGURE 47 PICOZED MICROHEADERS PINOUT

3.4. FRONT BOARD SHIFT REGISTERS

PWR led status and ERROR led status, together with TTL Led and TTL Inputs 50 Ω Termination of §2.2.3.2, are controlled from Slow FPGA Shift registers signals to four 8bit shift registers IC (SN74HC595PW) mounted serially on Front Board.

For complete description of the shift registers ICs (SN74HC595PW) used on Carrier board see : <http://www.ti.com/lit/ds/symlink/sn74hc595.pdf>

TABLE 26: SHIFT REGISTERS SIGNALS PIN ASSIGNMENT ON SLOW FPGA

Slow FPGA Pin#	Slow FPGA Pin Name	Function
7	IO_L51N_3	SHIFT_REG_SDATA
8	IO_L51P_3	SHIFT_REG_SCLK
9	IO_L50N_3	SHIFT_REG_LATCH
10	IO_L50P_3	SHIFT_REG_OE#

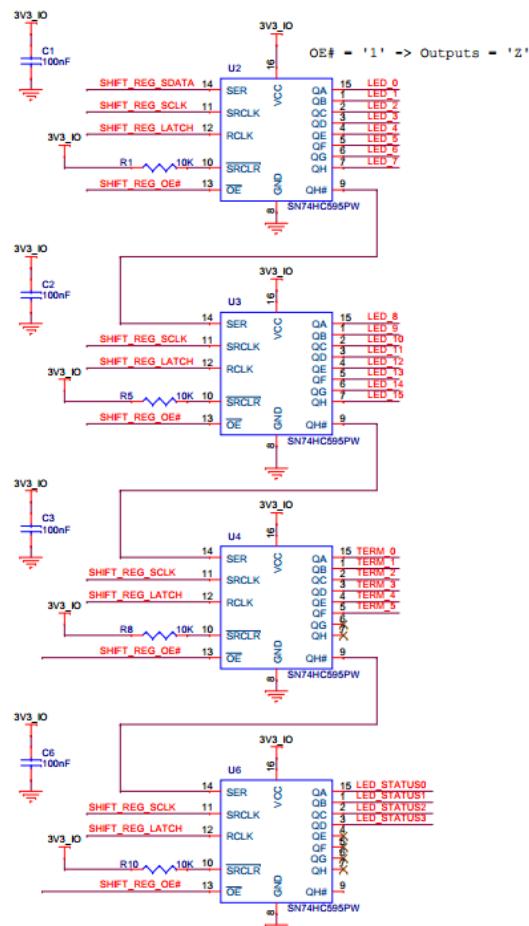


FIGURE 48: LED SHIFT REGISTERS FRONT BOARD SCHEMATIC

TABLE 27: SHIFT REGISTERS 32 BIT ASSIGMENT ON FRONT BOARD

Shift Registers bit#	Front Board Name	Function
0	LED_0	TTL OUT led 1
1	LED_1	TTL OUT led 2
2	LED_2	TTL OUT led 3
3	LED_3	TTL OUT led 4
4	LED_4	TTL OUT led 5
5	LED_5	TTL OUT led 6
6	LED_6	TTL OUT led 7
7	LED_7	TTL OUT led 8
8	LED_8	TTL OUT led 9
9	LED_9	TTL OUT led 10
10	LED_10	TTL IN led 1
11	LED_11	TTL IN led 2
12	LED_12	TTL IN led 3
13	LED_13	TTL IN led 4
14	LED_14	TTL IN led 5
15	LED_15	TTL IN led 6
16	TERM_0	Control 50 Ω Termination of TTL IN 1
17	TERM_1	Control 50 Ω Termination of TTL IN 2
18	TERM_2	Control 50 Ω Termination of TTL IN 3
19	TERM_3	Control 50 Ω Termination of TTL IN 4
20	TERM_4	Control 50 Ω Termination of TTL IN 5
21	TERM_5	Control 50 Ω Termination of TTL IN 6
22	*NONAME	*UNUSED
23	*NONAME	*UNUSED
24	LED_STATUS0	STA STATUS LED
25	LED_STATUS1	*UNUSED
26	LED_STATUS2	*UNUSED
27	LED_STATUS3	ACQ STATUS LED
28	*NONAME	*UNUSED
29	*NONAME	*UNUSED
30	*NONAME	*UNUSED
31	*NONAME	*UNUSED